Multilevel Coding/Modulation Using LDPC Convolutional Codes


Department of Electrical Engineering
University of Notre Dame
Notre Dame, IN 46556, U.S.A.
E-mail: {Pusane.1, Lentmaier.1, Fuja.1, Zigangirov.1, Costello.2}@nd.edu

Abstract

In this paper, we propose a novel multilevel coding scheme that employs low-density parity-check convolutional (LDPC) codes. A combined decoding/demodulation scheme is also considered. Unlike previous work on multilevel coding, the proposed scheme employs a single code with some structure that allows it to benefit from the use of multilevel mapping. The proposed scheme can be seen as a form of bit-interleaved coded-modulation (BICM) that employs multilevel mapping and iterative demodulation and a code with structure.

1. Introduction

Low-density parity-check convolutional (LDPC) codes, the convolutional counterpart of Gallager’s LDPC block codes [1], were introduced by Jiménez Feltström and Zigangirov in [2]. Decoding of these codes can be done by a pipeline decoder that employs $I$ independent processors, simultaneously performing the $I$ iterations. In order to develop power efficient schemes without sacrificing bandwidth efficiency, LDPC codes can be combined with known coded modulation schemes.

In this paper, we investigate the bit error rate performance of bandwidth efficient LDPC coding schemes. In particular, we propose a novel way of employing multilevel coding/demodulation for LDPC codes. While based on the set-partitioning idea of multilevel coding, the proposed scheme employs a single code and can be seen as a form of bit interleaved coded modulation (BICM) with combined decoding/demodulation. We also consider LDPC codes with conventional Gray mapped BICM. Computer simulation results show that bandwidth efficient schemes with LDPC coding outperform corresponding low-density parity-check block (LDPCB) coded systems with the same processor complexity.

2. Low-density parity-check convolutional codes

LDPC codes can be defined by a sparse syndrome former (transposed parity-check) matrix. An $(m, J, K)$ time-varying LDPC code is the set of sequences $v$ satisfying the equation $vH^T = 0$, where

$$H^T = \begin{bmatrix} H^T_0(0) & \cdots & H^T_{m_s}(m_s) \\ \vdots & \ddots & \vdots \\ H^T_{J-1}(t) & \cdots & H^T_{m_s}(t+m_s) \end{bmatrix}$$

(1)

Here, $H^T$ is an infinite syndrome former matrix with $J$ ones in each row and $K$ ones in each column. For a rate $R = b/c$ LDPC code, the elements $H^T_i(t)$, $i = 0, 1, \cdots, m_s$, are binary $c \times (c - b)$ submatrices

$$H^T_i(t) = \begin{bmatrix} h_i^{(1,1)}(t) & \cdots & h_i^{(1,c-b)}(t) \\ \vdots & \ddots & \vdots \\ h_i^{(c-1,1)}(t) & \cdots & h_i^{(c-1,c-b)}(t) \end{bmatrix}$$

(2)

The value $m_s$, called the syndrome former memory, is determined by the maximum width of the nonzero area in the matrix $H^T$ and is uniquely defined by demanding that $H^T_{m_s}(t) \neq 0$ for at least one time instant $t \in Z$. The pipeline decoder consists of $(J+1)$ shift registers of size $I \cdot (m_s+1) \cdot c$ plus $I$ processors that perform the decoding iterations simultaneously.
3. Multilevel coding with iterative decoding

Multilevel coding was introduced by Imai and Hirakawa in [3], and the set-partitioning idea was invented by Ungerboeck [4]. The goal of multilevel mapping is to increase the intra-subset minimum Euclidean distances of a signal constellation of size $2^l$ via set-partitioning. The resulting $l$ levels have different intra-subset minimum Euclidean distances. The idea of multilevel coding is to protect the $l$ levels with codes of different strengths. The higher levels, which have lower minimum Euclidean distances, should be protected by stronger (lower rate) codes, while the lower levels can be protected by weaker codes, since they already benefit from higher minimum Euclidean distance. The conventional multistage decoder for these codes starts from the highest level and, as soon as a decision about the bit corresponding to this level is made, this information is passed on and decoding of the next level starts. This continues until all $l$ bits are decoded. Thus, provided that the higher levels have been successfully decoded at every level, from the receiver perspective, sequential transmission of $l$ bits over the physical channel is equivalent to parallel transmission of the bits over $l$ separate channels.

In the area of error control coding, codes based on iterative decoding have been the most exciting development in the past decade. These codes can perform well at signal-to-noise ratios (SNRs) close to channel capacity while only requiring a decoding complexity that grows linearly with block (constraint) length. This makes them very good candidates to be used as component codes in a multilevel coding system designed to increase bandwidth efficiency while maintaining power efficiency. Coded modulation schemes combining turbo codes and multilevel coding have been previously studied in [5]. Since turbo codes perform well close to capacity, in [5] Wachsmann, Fischer, and Huber discussed the problem of optimal rate allocation among the levels. They concluded that multistage decoding suffices to achieve capacity as long as the rates of the levels are chosen equal to the capacities of the corresponding equivalent channels. However, in practice, when codes of finite length are used, the underlying assumption of perfect decoding at the higher levels is no longer valid, and multistage decoding is not necessarily optimal.

With the use of iterative decoding, we have not only hard decisions but also reliability information about the decoded bits. This suggests that we can use this reliability information in the decoding of the higher levels (see [6, 7, 8]). Another nice property of iterative decoding is that reliability information about a bit is available after each iteration. This suggests exchanging information between decoding iterations. This information exchange is performed by the demodulator.

A modification of the pipeline decoder for LDPC codes employing this combined demodulation/decoding principle was introduced in [9, 10]. The proposed system employed two regular LDPC codes of rates $R_1 = b_1/c = 1/4$ and $R_2 = b_2/c = 3/4$. The higher level code was chosen as an ($m_s$, 3, 4) code having a syndrome former row weight of 3 and a column weight of 4. The lower level code had a row weight of 3 and a column weight of 12. 4PSK multilevel mapping was used as the signal constellation. The Tanner graph of this scheme for a small syndrome former memory $m_s$ is presented in Figure 1. The consecutive columns of variable and check nodes in the Tanner graph of an LDPC code correspond to time instances. There are $c = 4$ variable nodes per time instant in both codes, and $c - b_1 = 3$ and $c - b_2 = 1$ check nodes per time instant in higher and lower level codes, respectively.

The difference between the traditional multistage decoder and the one proposed in [9] lies in the message-passing schedule on the Tanner graph. When a multistage decoder is employed to decode the scheme in Figure 1, the decoding is completed on the higher level of the Tanner graph and information is passed to the lower level decoder. Instead, [9] uses a symmetric message-passing schedule in which all nodes in the graph are activated at the same time during the iterative decoding procedure. A continuous information exchange between the levels is achieved by such an arrangement.

4. Multilevel mapping with a single code

As a class of LDPC codes, LDPC codes can be decoded using belief-propagation on a bipartite Tanner graph [11]. Messages are exchanged between the variable nodes and the check nodes in the graph representation. In traditional multistage decoding, each code has its own graph. As soon as decoding of a higher level code is finished, the decisions are fed to the decoders at the lower levels. When information is exchanged after every decoding iteration, the decoding operations at the different levels are no longer independent. This can be represented by introducing additional demodulation nodes (as indicated in Figure 1), by means of which the variable nodes of the graph at one level pass a priori information to the variable nodes of the graphs at other levels.

Instead of separate graphs, we can now consider a single graph representing the overall multilevel coding scheme that incorporates the codes at the individual levels and the demodulation. We can construct a single semi-regular LDPC code whose decoding is represented by this graph. The syndrome former matrix has
Figure 1: Tanner graphs of the codes corresponding to the multilevel scheme of [9] and their connection through the demodulation.

rows of weight 3 and columns of weights 4 and 12, so that the column weight ratio of 3 to 1 matches the rate combination given in [9]. The resulting overall code has a rate of $R = b/c = 1/2$, giving a bandwidth efficiency of 1 bit/sec/Hz. The Tanner graph corresponding to this scheme for a small syndrome former memory $m_s$ is shown in Figure 2. It should also be noted that the slight irregularity of the code allows different message probability densities to flow along different edges of the Tanner graph.

The system proposed in [9] used two codes with rates $R_1 = b_1/c = 1/4$ and $R_2 = b_2/c = 3/4$. The corresponding submatrices used in the syndrome former matrices (given by (2)) were of size $4 \times 3$ and $4 \times 1$, respectively. At every time interval, both encoders produced four bits, and the resulting four pairs of bits were used to choose a sequence of four signal points from the 4PSK multilevel mapped signal constellation. The proposed coding scheme using only one code follows a much simpler procedure. Since the rate of the code is 1/2, the submatrix has size $2 \times 1$ and every encoded 2-tuple is mapped directly into the 4PSK signal constellation.

Another popular approach to achieving high bandwidth efficiencies for iterative decoding schemes is to use Gray mapping. In this approach, the code symbols are directly mapped to the signal constellation without requiring any special structure. In the literature, this system is often referred to as bit interleaved coded modulation (BICM) [12, 13]. However, when used in conjunction with turbo or LDPC codes, an interleaver is not needed due to the inherent diversity of the codes. Note that, in this case, performing iterative demodulation does not improve the bit error rate performance of Gray mapped coded modulation schemes. Since Gray mapping is designed to minimize the dependency between mapped bits, the messages exchanged among the levels do not carry significant information.

The combined decoding/demodulation scheme proposed in this paper illustrates an analogy between multilevel coded systems and BICM systems. The proposed scheme can be seen as a BICM system that employs multilevel mapping and iterative demodulation and uses an irregular (semi-regular) code that has some structure, allowing it to benefit from the use of multilevel mapping. Therefore, the strength of set-partitioning is combined with the simplicity of BICM. We can apply this same idea to any multilevel coding system.
5. Simulation results

A processor’s complexity is determined by the total number of variable nodes that must be accessible at the same time. For a length $N$ LDPCB code, all $N$ variable nodes are within the processor’s operating region at all times. Correspondingly, this number is equal to $(ms+1) * c$ for an $(ms, J, K)$ LDPCC code. Therefore, in our comparisons with LDPCB codes, we set the block length to $N = (ms + 1) * c$.

A regular (1199,3,6) LDPCC code was used to construct a coded modulation scheme using Gray mapped 4PSK. The corresponding LDPCB code is a regular (2400,3,6) code. Also, a 4PSK multilevel coding scheme has been constructed using the method proposed in the previous section. This code’s syndrome former has 3 ones in each row and the column weights are 4 and 12. Every decoder was allowed a total of 100 iterations and the LDPCC pipeline decoders employed the on-demand variable node update schedule recently proposed in [14]. The simulation results for the bit error rate (BER) performance of these schemes are presented in Figure 3.

Similar constructions for an 8PSK constellation have been used to achieve 2 bits/sec/Hz bandwidth efficiency. The Gray mapped 8PSK scheme employs a rate $R = 2/3$ regular (1199,3,9) LDPCC code, and the corresponding LDPCB code is a regular (3600,3,9) code. The multilevel mapped code has been designed according to the rate distribution 0.25/0.85/0.90. The rows of the syndrome former matrix still have weight 3, and the column weights are 4, 20, and 30 corresponding to the first, second, and third mapping levels, respectively. Simulation results for these schemes are presented in Figure 4. It should be mentioned that the semi-regular codes which are designed specifically for multilevel mapping do perform bad when used with Gray mapping. This suggests that it is not only the code structure, but the correct combination of code structure and mapping that determines the performance.

It can be seen from the simulation results that the LDPCC codes outperform the corresponding LDPCB codes that have the same processor complexity, by nearly 1dB at a $10^{-5}$ BER. To compare the Gray mapped and multilevel mapped LDPCC codes, we must consider the optimal rate allocation problem. In [9], the codes were independently optimized to find the best rate combination. In the proposed scheme, the decoding graph includes all individual level graphs and the modulation, so it must be optimized as a whole.

Although the multilevel mapped scheme outperformed Gray mapping for the 4PSK signal constellation, the Gray mapped scheme outperformed the multilevel scheme in the 8PSK case. The flexibility of rate selection is limited when regular codes are used. Employing irregular codes can considerably increase the de-
gree of freedom in choosing the appropriate protection for the individual levels, however. Also, particularly for higher order signal constellations, the advantage of employing set-partitioning (multilevel mapping) becomes more apparent. As the signal constellation size increases, the minimum Euclidean distance becomes smaller and therefore set-partitioning becomes more effective. Thus, for larger constellation sizes, particularly if irregular code designs are employed, LDPCC codes in combination with multilevel mapping represent an attractive solution for achieving both power and bandwidth efficiency.

References


