Curriculum Vitae
Michael Niemier
August 31, 2012

Education

B.S. in Computer Engineering, University of Notre Dame, 1998
M.S. in Computer Engineering, University of Notre Dame, 2000
Ph.D. in Computer Engineering, University of Notre Dame, 2004

Appointments

Title	Organization	Duration
Assistant Professor	University of Notre Dame	July 2008 – present
Assistant Research Professor	University of Notre Dame	July 2007 – July 2008
Visiting Assistant Research Professor	University of Notre Dame	May 2005 – July 2007
Assistant Professor	Georgia Institute of Technology	Sept. 2003 – July 2007
Research Fellow	University of Notre Dame	Aug. 1998 – Aug. 2003

Scholarships and Fellowships

1. National Science Foundation Graduate Research Fellowship
2. Arthur J. Schmidt University of Notre Dame Presidential Fellowship

Distinctions, Honors, and Awards

1. Best paper award at International Symposium on Nanoscale Architectures (2009)
2. IBM Faculty Award (2008)

Professional Memberships

- IEEE (Senior Member), ACM

(Note: given the interdisciplinary nature of my work, my specific contributions to journal and conference publications are noted below each paper from 2010-2012, as well as for other select papers.)

Refereed Journal Articles – under review (JR)

1. Shiliang Liu, X. Sharon Hu, **Michael T. Niemier**, Joseph J. Nahas, Gary H. Bernstein, and Wolfgang Porod, "A Design Space Exploration of the Magnetic-Electrical Interfaces for Nanomagnet Logic," under review in *IEEE Transactions on Nanotechnology*.
    - Niemier, Hu, and Nahas advised Liu with this work
    - Niemier wrote/edited bulk of paper with Liu
    - Niemier, Hu advised Liu with respect to what structures should be designed and tested
2. Xueming Ju, **Michael Niemier**, Markus Becherer, Wolfgang Porod, Paolo Lugli, and György Csaba, "Systolic Pattern Matching Hardware with Out-of-Plane Nanomagnet Logic Devices," under review in *IEEE Transactions on Nanotechnology*.
    - Niemier wrote part of and edited all of paper
    - Niemier proposed systolic architecture designs (and initial NML mappings) presented in paper, and did benchmarking work
    - Ju and Csaba performed physical-level simulations (of Niemier's designs)

3. Mohammad Abu Jafar Siddiq, **M.T. Niemier**, G.H. Bernstein, W. Porod, X.S. Hu, "A Field Coupled Electrical Input for Nanomagnet Logic," under review in *IEEE Transactions on Nanotechnology*.
    - Siddiq is co-advised by Niemier and Bernstein
    - Niemier wrote paper with Siddiq
    - Niemier did simulation work with Siddiq to determine what structures should be fabricated (and how they should be controlled in the accompanying experiments) to successfully facilitate a field-coupled electrical input
    - Bernstein advised Siddiq with respect to fabrication-related aspects of electrical input structures

Refereed Journal Articles (J)

1. Peng Li, Vijay K. Sankar, Gyorgy Csaba, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, "Magnetic Properties of Enhanced Permeability Dielectrics for NML Circuits," accepted in *IEEE Transactions on Magnetics.*
    - Niemier initially proposed idea of using enhanced permeability dielectric-like materials for lowering clock energy in NML circuits
    - Niemier helped to design experiments presented in paper (to provide best insight with respect to how materials considered might improve energy associated with application-level hardware)
2. Peng Li, Gyorgy Csaba, Vijay K. Sankar, Xueming Ju, Edit Varga, Paolo Lugli, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, and Gary Bernstein, "Direct Measurement of Magnetic Coupling between Nanomagnets for NML Applications," accepted in *IEEE Transactions on Magnetics*.
    - Niemier assisted with analysis of experimental results
3. M. Tanvir Alam, Steven Kurtz, M. Jafar Siddiq, **Michael T. Niemier**, Gary H. Bernstein, Xiaobo Sharon Hu, and Wolfgang Porod, "On-chip Clocking of Nanomagnet Logic Lines and Gates," in *IEEE Transactions on Nanotechnology*, 11(2), p. 273-286, 2012.
    - Alam should be considered the sole lead author. He is primarily responsible for the design and implementation of the experiments presented in this work
    - Siddiq assisted with experiments and performed finite element simulations
    - Niemier and Bernstein co-advised Alam and Siddiq
    - Niemier designed and advised Alam as to what NML patterns should be placed on clock lines, helped to interpret results, designed and directed simulation efforts, and wrote the manuscript with Alam and Kurtz
    - Bernstein advised Alam on clock wire fabrication and helped to edit the manuscript
    - Kurtz performed all of the micromagnetic simulation work reported in this manuscript and supporting online texts. He is co-advised by Niemier
4. **M. Niemier**, E. Varga, G. H. Bernstein, W. Porod, M. T. Alam, A. Dingler, A. Orlov, and X. Sharon Hu, "Shape Engineering for non-majority Boolean gate designs with nanomagnet logic," in *IEEE Transactions on Nanotechnology*, 11(2), p. 220-230, 2012. **(#3 most downloaded paper in March, 2012)**.
    - Alam and Dingler are advised by Niemier
    - Niemier designed and developed gate and experiments presented here, as well as the shape-based logic idea
    - Niemier wrote paper
5. Peng Li, Gyorgy Csaba, Vijay K. Sankar, Xueming Ju, Paolo Lugli, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, "Switching Behavior of Lithographically Fabricated Nanomagnets for Logic Applications," *Journal of Applied Physics,* 111, 07B911, April 2012.
    - Niemier assisted with analysis of experimental results
6. M. Crocker, **M.T. Niemier**, and X.S. Hu "A Reconfigurable PLA Architecture for Nanomagnet Logic," *ACM Journal of Emerging Technology and Computing Systems, ACM Journal on Emerging Technologies in Computing*, Vol. 8, No. 1, p. 1-25, February, 2012.
    - Hu originally derived implementation independent PLA design; Niemier worked with Crocker to port to magnetic implementation
    - Niemier directed physical-level simulations
    - Niemier worked with Crocker and Hu to write paper and did much of the technical editing
7. **M.T. Niemier**, G.H. Bernstein, A. Dingler, X.S. Hu, S. Kurtz, S. Liu, J. Nahas, W. Porod, M.

Siddiq, and E. Varga, "Nanomagnet Logic: Progress Toward System-Level Integration," in *Journal of Physics: Condensed Matter*, 23, 493202, 2011.

- Niemier organized, compiled material for, did additional simulation work for, and wrote paper (~4-5 pages of ~ 25 page paper were written by co-authors under Niemier's coordination and guidance).

8. Shiliang Liu, X. Sharon Hu, Joseph J. Nahas, **Michael Niemier**, Wolfgang Porod, and Gary H. Bernstein, "Magnetic-Electrical Interface for Nanomagnet Logic," in *IEEE Transactions on Nanotechnology*, 10(4), p. 757-763, 2011 **(Featured on cover)**.

- Liu is officially advised by Hu, but meets with Niemier and Hu each week
- Niemier helped to design simulated interface and guided Liu in simulation efforts
- Niemier helped to write introduction and background of paper, and worked with Hu and Bernstein to write and edit text describing specific technical contributions

9. Aaron Dingler, **Michael T. Niemier**, Xiaobo Sharon Hu, and Evan Lent, "Performance and Energy Impact on Locally Controlled NML Circuits," in *ACM Journal on Emerging Technologies in Computing*, 7(1), p. 1-24, 2011.
   - Dingler is advised by Niemier
   - Niemier directed simulation efforts for this paper
   - Niemier and Hu worked together with Dingler to devise clocking schemes
   - Niemier and Dingler wrote paper
10. Steven Kurtz, Edit Varga, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, and X. Sharon Hu, "Two Input, Non-Majority Magnetic Logic Gates: Experimental Demonstration and Future Prospects," in *Journal of Physics: Condensed Matter*, 23(5), p. 053202, 2011.
    - Varga performed experiments
    - Kurtz performed simulations
    - Niemier designed experiments and simulation set
11. Mohmmad Tanvir Alam, Mohammad Jafar Siddiq, Gary H. Bernstein, **Michael Niemier**, Wolfgang Porod, and X. Sharon Hu, "On-chip Clocking for Nanomagnet Logic Devices," *IEEE Transactions on Nanotechnology*, p. 348-351, Volume 9(3), 2010.
    - Alam and Siddiq are co-advised by Niemier
    - Niemier designed switching experiments and either did or guided simulation efforts
    - Bernstein guided fabrication efforts
    - Niemier/Bernstein/Porod/Hu developed clock structure that was implemented
    - Niemier wrote paper with Alam
12. Edit Varga, Alexei Orlov, **Michael T. Niemier**, X. Sharon Hu, Gary H. Bernstein, Wolfgang Porod, "Experimental Demonstration of Fanout for Nanomagnet Logic," in *IEEE Transactions on Nanotechnology*, 9(6), p. 668-670, 2010.
    - Niemier personally did simulation work included in paper
13. M. Crocker, X.S. Hu, and **M.T. Niemier**, "Defects and Faults in QCA-Based PLAs," *ACM Journal of Emerging Technology and Computing Systems*, Vol. 5, No. 2, p. 1-27, 2009.
14. M. Crocker, X. Sharon Hu, **M. Niemier**, M. Yan, and G. Bernstein, "PLAs in Quantum-Dot Cellular Automata," *IEEE Transactions on Nanotechnology*, Vol.7, no.3, pp.376-386, May 2008.
15. M. Crocker, **M. Niemier**, X. Sharon Hu, and M. Lieberman, "Molecular QCA design with chemically reasonable constraints," *ACM Journal of Emerging Technology and Computing Systems*, Vol. 4, No. 2, p. 1-21, 2008.
16. A. Chaudhary, D. Z. Chen, X.S. Hu, **M. T. Niemier**, R. Ravichandran, and K. Whitton, "Easing Fabricatable Interconnect in Molecular QCA Circuits," in *IEEE Transactions on CAD (TCAD)*, p. 1978-1991, Vol. 26(11), November 2007.
17. S.K. Lim, R. Ravichandran, and **M.T. Niemier**, "Partitioning and Placement for Buildable QCA Circuits," in *ACM Journal on Emerging Technologies in Computing Systems (JETC)*,

Vol. 1, No. 1, p.50-72, 2005.

18. R. Ravichandran, S.K. Lim, and **M.T. Niemier**, "Automatic Cell Placement for Quantum-dot Cellular Automata," in *Integration: The VLSI Journal*, Vol. 38, No. 3, p.541-548, 2005.
19. **M.T. Niemier** and P.M. Kogge, "Problems in Designing with QCAs: Layout = Timing," in *International Journal of Circuit Theory and Applications*, 29: 49-62, 2001.

Refereed Conference and Workshop Papers – under review (CR)

1. A. Papp, **M. Niemier**, A. Csurgay, M. Becherer, S. Brietkreutz, J. Kiermaier, I. Eichwald, X. Ju, W. Porod, and G. Csaba, "Design of a Threshold-Gate Based Full Adder from Out-of-Plane Nanomagnet Logic," under review at Joint MMM/Intermag Conference, Chicago, IL, 2013.
    - Niemier devised gate design with Csaba
2. Peng Li, György Csaba, Vijay K. Sankar, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, "Paths to Clock Power Reduction via High Permeability Dielectrics for Nanomagnet Logic Circuits," under review at Joint MMM/Intermag Conference, Chicago, IL, 2013.
    - Niemier initially proposed idea of using enhanced permeability dielectric-like materials for lowering clock energy in NML circuits
    - Niemier helped to design experiments presented in paper (to provide best insight with respect to how materials considered might improve energy associated with application-level hardware)
3. Mohammad A Siddiq, Gary H. Bernstein, **Michael T. Niemier**, Xiaobo S. Hu, Gyorgy Csaba, Wolfgang Porod, "Demonstration of Field-Coupled Input Scheme on Line of Nanomagnets," under review at Joint MMM/Intermag Conference, Chicago, IL, 2013.
    - Siddiq is co-advised by Niemier and Bernstein
    - Niemier wrote paper with Siddiq
    - Niemier did simulation work with Siddiq to determine what structures should be fabricated (and how they should be controlled in the accompanying experiments) to successfully facilitate a field-coupled electrical input
    - Bernstein advised Siddiq with respect to fabrication-related aspects of electrical input structures
4. E. Varga, **M.T. Niemier**, G. Csaba, G.H. Bernstein, and W. Porod, "Experimental Realization of a Nanomagnet Full Adder Using Slanted-Edge Input Magnets," under review at Joint MMM/Intermag Conference, Chicago, IL, 2013.
    - Niemier devised compact adder design used in experiments
5. S. C. Karthik, P. Li, S. Liu, F. Shah, D. Himadri, G. Csaba, **M. Niemier**, S. Hu, W. Porod, and G.H. Bernstein, "Psuedo-Spin-Valve Giant Magnetoresistance Strutures for Electronic Readout in Nanomagnet Logic," under review at Joint MMM/Intermag Conference, Chicago, IL, 2013.
    - Niemier assisted with analysis of experimental results

Refereed Conference and Workshop Papers (C)

1. Steve Kurtz, Aaron Dingler, Michael Niemier, Xiaobo Sharon Hu, György Csaba, Joseph Nahas, Wolfgang Porod, and Gary Bernstein, "Preserving Steady State Non-Volatility in Nanomagnet Logic Circuits," in the SRC's TECHCON: Technology and Talent for the 21st Century, September 10-11, 2012.
    - Kurtz and Dingler are solely advised by Niemier
    - Niemier directed the work presented in this paper
2. Peng Li, Gyorgy Csaba, Vijay Karthik Sankar, Xueming Ju, Edit Varga, Paolo Lugli, Xiaobo Sharon Hu, **Michael T. Niemier**, Wolfgang Porod, Gary H. Bernstein, "Direct Measurement of Magnetic Coupling Between Nanomagnets for Nanomagnet Logic Applications," in the SRC's TECHCON: Technology and Talent for the 21st Century, September 10-11, 2012.

- Niemier assisted with analysis of experimental results

3. Mohammad Siddiq, Gary H. Bernstein, **Michael T. Niemier**, Wolfgang Porod, Xiaobo Sharon Hu, "Experimental Demonstration of Field-Coupled Input Scheme for Nanomagnet Logic (NML)," in the SRC's TECHCON: Technology and Talent for the 21st Century, September 10-11, 2012.
   - Siddiq is co-advised by Niemier and Bernstein
   - Niemier wrote paper with Siddiq
   - Niemier did simulation work with Siddiq to determine what structures should be fabricated (and how they should be controlled in the accompanying experiments) to successfully facilitate a field-coupled electrical input
   - Bernstein advised Siddiq with respect to fabrication-related aspects of electrical input structures
4. **M. Niemier**, X. Ju, M. Becherer, G. Csaba, A Dingler, X.S. Hu, D. Schmitt-Landsiedel, P. Lugli, and W. Porod, "Boolean and Non-Boolean Architectures for Out-of-Plane Nanomagnet Logic," to appear in the Proceedings of the International Workshop on Cellular Nanoscale Networks and their Applications, August 29-31, 2012.
   - Niemier wrote paper
   - Niemier proposed systolic architecture designs (and initial NML mappings) presented in paper and did benchmarking work
   - Ju and Csaba performed physical-level simulations (of Niemier's designs)
   - Niemier also developed non-Boolean aspects of this work
5. Wolfgang Porod, Peng Li, Faisal Shah, Mohammad Siddiq, Edit Varga, Gyorgy Csaba, Vijay Sankar, Gary H. Bernstein, X. Sharon Hu, **Michael Niemier**, Joseph Nahas, and Alexei Orlov, "NanoMagnet Logic," Proceedings of the Device Research Conference, p. 213-14, June 18-20, 2012.
   - Review paper / talk
6. Peng Li, Gyorgy Csaba, Vijay K. Sankar, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, and Gary H. Bernstein, "Power Reduction in Nanomagnet Logic Clocking through High Permeability Dielectrics," Proceedings of the Device Research Conference, p. 129-130, June 18-20, 2012.
   - Niemier initially proposed idea of using enhanced permeability dielectric-like materials for lowering clock energy in NML circuits
   - Niemier helped to design experiments presented in paper (to provide best insight with respect to how materials considered might improve energy associated with application-level hardware)
7. **M. Niemier**, X. Ju, M. Becherer, G. Csaba, X.S. Hu, D. Schmitt-Landsiedel, P. Lugli, and W. Porod, "Systolic Architectures and Applications for Nanomagnet Logic," Proceedings of the Silicon Nanoelectronics Workshop, June 10-11, 2012.
   - Niemier wrote paper using simulation data from Ju
   - Niemier performed architectural-level analysis presented in paper
8. Xueming Ju, Markus Becherer, Paolo Lugli, **Michael T. Niemier**, Wolfgang Porod, and György Csaba, "Design of a Systolic Pattern Matcher for Nanomagnet Logic," at the International Workshop on Computational Electronics, p. 1-3, May 22-25, 2012.
   - Niemier proposed systolic architecture designs (and initial NML mappings) presented in paper and did benchmarking work
   - Ju and Csaba performed physical-level simulations (of Niemier's designs)
9. Aaron Dingler, Steve Kurtz, **Michael Niemier**, X Sharon Hu, Gyorgy Csaba, Joesph Nahas, Wolfgang Porod, Gary Bernstein, Peng Li, Vijay Karthik Sankar, "Making Non-Volatile Nanomagnet Logic Non-Volatile," Proceedings of the Design Automation Conference (DAC), p. 476-485, 2012 (22% acceptance rate).
   - Kurtz and Dingler are solely advised by Niemier
   - Niemier directed the work presented in this paper and the analysis techniques used (in support of a DARPA project deliverable)
   - Niemier identified how an NML-clock architecture could impact non-volatility
   - Niemier proposed materials-based solutions presented in paper
   - Niemier wrote paper with Dingler and Kurtz
10. Peng Li, Gyorgy Csaba, Vijay K. Sankar, Xueming Ju, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, "Direct Measurement of Magnetic Coupling between Nanomagnets for NML Applications," Proceedings of INTERMAG, May 7-11, 2012. (Best

student paper nominee, oral presentation).

- Niemier assisted with analysis of experimental results

11. Peng Li, Vijay K. Sankar, Gyorgy Csaba, Faisal Shah, X. Sharon Hu, **Michael Niemier**, Wolfgang Porod, Gary H. Bernstein, "Enhanced Permeability Dielectrics for Power Reduction in NML Circuits," Proceedings of Intermag, May 7-11, 2012 (oral presentation).
    - Niemier initially proposed idea of using enhanced permeability dielectric-like materials for lowering clock energy in NML circuits
    - Niemier helped to design experiments presented in paper (to provide best insight with respect to how materials considered might improve energy associated with application-level hardware)
12. Peng Li, Gyorgy Csaba, Vijay K. Sankar, X. Sharon Hu, **Michael Niemier**, Wolfang Porod, Gary H. Bernstein, "Switching Behavior of Lithographically Fabricated Nanomagnets for Logic Applications," Magnetism and Magnetic Materials (MMM), October, 2011, Scottsdale, AZ .
    - Niemier assisted with analysis of experimental results
13. Shiliang Liu, X. Sharon Hu, Joseph J. Nahas, **Michael Niemier**, Gary H. Bernstein, and Wolfgang Porod, "Magnetic-Electrical Interface for Nanomagnet Logic" in the SRC's TECHCON 2011: Technology and Talent for the 21st Century".
    - Liu is officially advised by Hu, but meets with Niemier and Hu each week
    - Niemier helped to design simulated interface and guided Liu in simulation efforts
14. Shiliang (Shawn) Liu, Xiaobo S. Hu, Joseph J. Nahas, **Michael T. Niemier**, Work in Progress session at the *2011 Design Automation Conference (DAC).*
    - Niemier, Hu, and Nahas advised Liu with this work
    - Niemier wrote/edited bulk of paper with Liu
    - Niemier, Hu advised Liu with respect to what structures should be designed and tested
15. György Csaba, Paolo Lugli, **Michael Niemier** and Wolfgang Porod, "Magnetic excitations for information processing," in *12th IEEE CNNA - International Workshop on Cellular Nanoscale Networks and Applications*, p. 1-5, February 3-5, 2010.
    - Niemier developed background material for paper
16. Steve Kurtz, **Michael Niemier**, X. Sharon Hu, Wolfgang Porod, and Gary H. Bernstein, "Design Space Exploration for Nanomagnet Logic Systems", in *Proceedings of Foundations of Nanoscience (FNANO 10)* (Snowbird, UT), p. 62-63, April 27-30, 2010 (invited).
    - Invited presentation/paper for Niemier
    - Niemier directed design space exploration work performed by Kurtz; Hu assisted
17. M. Alam, G.H. Bernstein, J. Bokor, D. Carlton, X.S. Hu, S. Kurtz, B. Lambson, **M.T. Niemier**, W. Porod, M. Siddiq, and E. Varga, "Experimental Progress of and Prospects for Nanomagnet Logic (NML)," in *Proceedings of the Silicon Nanoelectronics Workshop* (Hawaii), p. 1-2, June 15-17, 2010.
    - Survey paper written by Niemier
18. Michael Crocker, X. Sharon Hu, and **Michael Niemier**, "Design and Comparison of NML Systolic Architectures", in *Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures* (Anaheim, CA), p. 29-34, June 17-18, 2010 (33% acceptance rate).
    - Crocker is officially advised by Hu, but met regularly with Hu and Niemier
    - Niemier developed paper topic/material (i.e. NML-systolic architecture mapping)
    - Editing shared evenly between Niemier and Hu
19. E. Varga, S. Liu, **M.T. Niemier**, W. Porod, X.S. Hu, G.H. Bernstein, and A. Orlov, "Experimental Demonstration of Fanout for Nanomagnet Logic," in *Proceedings of the Device Research Conference*, p. 95-96, 2010.
    - Paper written by Niemier
    - Simulation work and discussion of extensibility to CMOS compatible fabrication mechanisms performed by Niemier

20. Edit Varga, **Michael T. Niemier**, Gary H. Bernstein, Wolfgang Porod, and X. Sharon Hu, "Programmable Nanomagnet-Logic Majority Gate," in *Proceedings of the Device Research Conference*, p. 85-86, 2010.
    - Simulation work done by Niemier
21. E. Varga, M. Siddiq, **M.T. Niemier**, M.T. Alam, G.H. Bernstein, W. Porod, X.S. Hu, and A. Orlov, "Experimental Demonstration of Non-Majority, Nanomagnet Logic Gates," in *Proceedings of the Device Research Conference*, p. 87-88, 2010.
    - Paper written by Niemier
    - Idea developed by Niemier
    - Varga and Siddiq performed experiments presented
22. E. Varga, M. Siddiq, M. Niemier, G.H. Bernstein, and W. Porod, "Experimental Investigation of Slanted Supermalloy Nanomagnets and Their Application in Nanomagnet Logic", to appear in the SRC's TECHCON 2010: Technology and Talent for the 21st Century"
    - Niemier worked with Varga to write paper
    - Premise of paper developed by Niemier
23. G. H. Bernstein, J. Kulick, D. Kopp, J. Bonath, J. Brockman, W. Buckhanan, S. Dai, P. Fay, M. Khan, A. Kriman, Y. Lee, C. Liang, **M. Niemier**, M. Padberg, D. Rinzler, R. Savino, and G. Snider, "Quilt Packaging – a Quasi-Monolithic Way to Merge Heterogeneous Technologies and Scales," in *Proceedings of Foundations of Nanoscience (FNANO09)* (invited, keynote).
24. M. T. Alam, S. Kurtz, **M.T. Niemier**, S. X. Hu, G. H. Bernstein, and W. Porod, "Magnetic Logic Based on Field-Coupled Nanomagnets: Clocking Structures and Power Analysis," in *Proceedings of Foundations of Nanoscience (FNANO09)* (invited).
25. E. Varga, **M. T. Niemier**, G.H. Bernstein, W. Porod, and X. Sharon Hu, "Non-volatile and Reprogrammable MQCA-based Majority Gates," in *Proceedings of the Device Research Conference*, p.1-2, June 22, 2009.
26. A. Dingler, **M.T. Niemier**, X.S. Hu, M.T. Alam, and M. Garrison, "System-Level Energy and Performance Projections for Nanomagnet-based Logic," in *Proceedings of the IEEE Symposium on Nanoscale Architectures*, p.21-26, July 30-31, 2009 **(best paper award)**.
    - Dingler is solely advised, and Alam is co-advised by Niemier
    - Niemier devised analysis, benchmarking techniques and directed work
27. M.T. Alam, M.A. Siddiq, **M.T. Niemier**, X.S. Hu, W. Porod, and G. H. Bernstein, "Fabrication of On-Chip Clock Structure for Nanomagnet QCA (MQCA)," in TECHCON 2009: Technology and Talent for the 21st Century" **(best student presentation award)**.
    - Alam was the presenting author
    - Alam is co-advised by Niemier and Bernstein
28. A. Dingler, M.J. Siddiq, **M.T. Niemier**, X.S. Hu, M.T. Alam, G.H. Bernstein, and W. Porod, "Controlling Magnetic Circuits: How Clock Structure Implementation will Impact Logical Correctness and Power," in *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, p.94-102, October 7-9, 2009.
    - Dingler is solely advised, and Alam and Siddiq are co-advised by Niemier
29. M. Crocker, X. Sharon Hu, and **M. Niemier**, "Defect Tolerance in QCA-Based PLAs," in *Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures*, p.46-53, Anaheim, CA, June 12-13, 2008 (27% acceptance rate).
30. M. T. Alam, S. Kurtz, **M.T. Niemier**, S. X. Hu, G. H. Bernstein, and W. Porod, "Magnetic Logic Based on Field-Coupled Nanomagnets: Clocking Structures and Power Analysis," in *Proceedings of the 8th IEEE International Conference on Nanotechnology*, Arlington, TX, p. 637, August 18-21, 2008 (invited paper).
31. **M. Niemier**, A. Dingler, and X. Sharon Hu, "Design Tradeoffs for Improved Performance in

MQCA-based Systems," in the *Proceedings of the 1st IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS)*, Cambridge, MA, Sept. 29-30, 2008, p. 35-38.

32. **M. Niemier**, M. Crocker, and X. Sharon Hu, "Fabrication Variations and Defect Tolerance for Nanomagnet-based QCA," in *Proceedings of the 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cambridge, MA, Oct. 1-3, 2008, p. 534-542.
33. **M. Niemier**, A. Dingler, X. Sharon Hu, M. Tanvir Alam, G. Bernstein, and W. Porod, "Bridging the Gap between Nanomagnetic Devices and Circuits," in *Proceedings of the 26th IEEE International Conference on Computer Design*, Lake Tahoe, CA, Oct. 12-15, 2008, p. 506-513 (34% acceptance rate).
    - Dingler is solely advised, and Alam is co-advised by Niemier
    - Niemier devised ideas for wire crossings and employment of "helper islands" presented in this paper
34. X.S. Hu and **M.T. Niemier**, "Computing with nearest neighbor interactions: a nanomagnetic implementation," in the *Proceedings of the 6th IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis*, Atlanta, GA, Oct. 19-24, 2008, p. 223-330 (invited paper).
35. M. T. Alam, G. H. Bernstein, W. Porod, S. Hu, **M. Niemier**, M. Putney, and J. DeAngelis, "Power Dissipation for Clocked Magnetic QCA," in the *Proceedings of the 12th International Workshop on Computational Electronics*, October 8-10, 2007, Amherst, MA.
36. **M. Niemier**, M.T. Alam, X.S. Hu, G. Bernstein, W. Porod, M. Putney, and J. DeAngelis, "Clocking Structures and Power Analysis for Nanomagnet-based Logic Devices," in the *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 26-31, 2007 (29% acceptance rate).
    - Alam is co-advised by Niemier and Bernstein
    - Niemier wrote paper with Alam, Bernstein, and Hu
    - Niemier, Bernstein, and Alam devised clock structures
37. M. Crocker, X.S. Hu, and **M.T. Niemier**, "Fault Models and Yield Analysis for QCA-based PLAs," in the *Proceedings of 17th International Conference on Field Programmable Logic and Applications (FPL)*, p. 435-440, Amsterdam, Netherlands, August 27-29, 2007.
38. A. Chaudhary, D.Z. Chen, R. Fleischer, X.S. Hu, J. Li, **M.T. Niemier**, Z. Xie, and H. Zhu, "Approximating the Maximum Sharing Problem," in the *Proceedings of Workshop on Algorithms and Data Structures*, Halifax, Canada, p. 52-63, August 15-17, 2007.
39. G. Bernstein, M. Alam, W. Porod, S. Hu, **M. Niemier**, M. Putney, and J. DeAngelis, "Clocking Scheme for Nanomagnet QCA (NMQCA)," in the *Proceedings of the 7th IEEE International Conference on Nanotechnology*, Hong Kong, p. 403-408, August 2-5, 2007.
40. M.T. Alam, **M. Niemier**, W. Porod, S. Hu, M. Putney, J. DeAngelis, and G. Bernstein, "On-Chip Clocking Scheme for Nanomagnet QCA," in the *Proceedings of the Device Research Conference*, p.133-134, Notre Dame, IN, June 18-20, 2007.
41. **M.T. Niemier**, X.S. Hu, M. Lieberman, and M. Crocker, "Using CAD to Shape Experiments in QCA," in the *Proceedings of International Conference on Computer Aided Design (ICCAD)*, p. 907-914, November 8, 2006 (25.1% acceptance rate).
42. **M.T. Niemier**, X.S. Hu, M. Lieberman, M. Crocker, Pavan Sadarangani, Zack Capozzi, and Tim Dysart, "Using DNA as a Circuitboard for a Molecular QCA PLA," in the *Proceedings of Foundations of Nanoscience (FNANO06)*, p. 96-107, April 23 - April 27th, 2006 (invited paper).
43. X.S. Hu, M. Crocker, **M.T. Niemier**, M.Yan, and G. Bernstein, "PLAs in Quantum-dot Cellular Automata," in the *Proceedings of International Symposium on VLSI*, p. 242-247, March 2-3, 2006.

44. A. Chaudhary, D.Z. Chen, X.S. Hu, **M.T. Niemier**, R. Ravichandran, K. Whitton, "Eliminating Wire Crossings for Molecular Quantum-dot Cellular Automata Implementation," in the *Proceedings of the International Conference on Computer Aided Design (ICCAD)*, Nov. 6-10, p. 565-571, 2005 (25% acceptance rate).
45. R. Ravichandran, **M.T. Niemier**, and S.K. Lim, "Partitioning and Placement for Buildable QCA Circuits," in the *Proceedings of IEEE/ACM Asia South Pacific Design Automation Conference*, p. 424-427, 2005.
46. **M.T. Niemier**, R. Ravichandran, and P.M. Kogge, "Using Circuits and Systems Research to Drive Nanotechnology," in the *Proceedings of the International Conference on Circuit Design*, p. 302-309, October 11-13, 2004 (invited paper).
47. D.A. Antonelli, T.J. Dysart, D.Z. Chen, A.B. Kahng, P.M. Kogge, R.C. Murphy, and **M.T. Niemier**, "Quantum-Dot Cellular Automata (QCA) Circuit Partitioning: Problem Modeling and Solutions," in the *Proceedings of the 41st Design Automation Conference*, p. 363-368, June 7-11, 2004, San Diego, CA (21% acceptance rate).
48. R. Ravichandran, N. Ladiwala, J. Nguyen, **M.T. Niemier**, S.K. Lim, "Automatic Cell Placement for Quantum-dot Cellular Automata," in the *Proceedings of the 14th Great Lakes Symposium on VLSI*, Boston, MA, April 2004, p. 332-337.
49. **M.T. Niemier** and P.M. Kogge, "The 4-Diamond Circuit - A Minimally Complex Nano-scale Computational Building Block in QCA," in the *Proceedings of the IEEE Computer Society Symposium on VLSI*, p. 3-10, IEEE Computer Society Press, Lafayette, LA, February 2004.
50. **M.T. Niemier** and P.M. Kogge, "Teaching Students Computer Architecture for New Nanotechnologies," in the *Proceedings of the Workshop on Computer Architecture Education (WCAE)*, held in conjunction with the 29th International Symposium of Computer Architecture (ISCA), Anchorage, AK, May 2002.
51. **M.T. Niemier**, A.F. Rodrigues, and P.M. Kogge, "A Potentially Implementable FPGA for Quantum Dot Cellular Automata," in the *Proceedings of the 1st Workshop on Non-Silicon Computation (NSC-1)*, held in conjunction with the 8th International Symposium on High Performance Computer Architecture (HPCA-8), Boston, MA, p. 38-45, February 2002.
52. **M.T. Niemier** and P.M. Kogge, "Exploring and Exploiting Wire-Level Pipelining in Emerging Technologies," in the *Proceedings of the 28th International Symposium of Computer Architecture*, p. 166-177, IEEE Computer Society Press, Goteburg, Sweden, July 2001.
53. **M.T. Niemier**, M.J. Kontz, and P.M. Kogge, "A Design of and Design Tools for a Novel Quantum Dot Based Microprocessor," in the Proceedings of the 37th Design Automation Conference, p. 227-232, Association for Computer Machinery (ACM) Press, Los Angeles, CA, June 2000.
54. **M.T. Niemier** and P.M. Kogge, "Logic in Wire: Using Quantum Dots to Implement a Microprocessor," in the *Proceedings of the International Conference of Electronics, Circuits, and Systems*, p.1211-1215, Vol. 3 IEEE Computer Society Press, Larnaca, Cyprus, September 1999.
55. **M.T. Niemier** and P.M. Kogge, "Designing Complex Logic Systems with QCA Devices," in the *Proceedings of the 9th Great Lakes Symposium on VLSI*, p. 122-125, IEEE Computer Society Press, Ann Arbor, MI, March 2-4, 1999.
56. **M.T. Niemier** and P.M. Kogge, "Logic-in-Wire: Using Quantum Dots to Implement Really Dense Processing Logic," in the Proceedings of the Third Petaflops Workshop held in conjunction with Frontiers of Massively Parallel Processing, Annapolis, MD, February 1999.

Un-refereed Publications

1. Wayne L. Buckhanan, **Michael Niemier**, and Gary H. Bernstein, "Bridging the HPC Processor-Memory Gap with Quilt Packaging," 18th Biennial University/Government/Industry Micro/Nano Symposium (UGIM), p. 1-3, June 28, 2010.
2. **M. T. Niemier**, X. S. Hu, M. Alam, G. Bernstein, W. Porod, M. Putney, and J. DeAngelis, "TR 2007-01: Clocking Structures and Power Analysis for Nanomagnet-Based Logic Devices," (Technical Report).
3. **M.T. Niemier**, "TR 2006-11: Notes on Interconnection Networks for PIM," (Technical Report).
4. **Michael Niemier**, Peter Kogge, Richard Murphy, Arun Rodrigues, Tim Dysart, and Sarah Frost, "TR 2006-14: Dataflow in Molecular QCA: Logic Can "Sprint", but the Memory Wall Can Still be a Hurdle," (Technical Report).
5. Erik DeBenedictis, Peter Kogge, Craig Lent, **Michael Niemier**, and Thomas Sterling, "TR 2006-15: The Technology Lane on the Road to a Zettaflops," (Technical Report).
6. Sharon Hu, **Michael Niemier**, and Michael Crocker, "TR 2005-17: PLA Designs in QCA," (Technical Report).

Invited Book Chapters

1. **M.T. Niemier** and W. Porod, "Nanomagnet Logic," CRC Handbook on Nanotechnology, 2011.
2. **M.T. Niemier** and P.M. Kogge, "Origins of Design Rules for QCA," in *Nano, Quantum, and Molecular Computation*, Iris Bahar and Sandeep Shukla (Editors), p. 267-292, Kluwer Press, June 2004.
3. J. Nguyen, R. Ravichandran, S.K. Lim, and **M.T. Niemier**, "Origins of CAD tools for QCA Systems," in *Nano, Quantum, and Molecular Computation,* Iris Bahar and Sandeep Shukla (Editors), p. 295-316, Kluwer Press, June 2004.
4. C.S. Lent, G.L. Snider, G. Bernstein, W. Porod, A. Orlov, M. Lieberman, T. Fehlner, **M.T. Niemier,** and P.M. Kogge, "Quantum-Dot Cellular Automata," chapter in *Electron Transport in Quantum Dots*, p. 397-433, Johahtan P. Bird (ed.), Kluwer Academic Publishers, 2003.

Invited Lectures and Addresses

(Numerous conference and review presentations are *not* included here for sake of brevity.)

1. I was invited by G. Bourianoff of Intel to present NML to the ITRS ERD working group in Bordeaux, France, September 21, 2012. (Because this trip will coincide with the birth of my second daughter, co-PI Wolfgang Porod will likely present this work.)
2. NRI Architectural-Level Benchmarking Workshop, August 14, 2011
3. Technical University Munich, March 12, 2012.
4. NRI Architectural-Level Benchmarking Workshop, August 16, 2011
5. Sandia National Labs, March 15, 2011.
6. NASA Jet Propulsion Lab, March 14, 2011.
7. Argonne National Labs, December 10, 2010.
8. IBM Almaden, November 4, 2010.
9. IBM Spintronics working group tele-seminar, October 4, 2010.
10. I was invited by G. Bourianoff of Intel to present NML to the ITRS ERD working group in Seville, Spain, September 17, 2010 (at a workshop co-located with ESSERDC). (Because this trip coincided with the birth of my first daughter, co-PI Sharon Hu presented this work.)

11. "Circuit Design and Architectures for Nanoscale Magnetic Logic Devices", invited seminar at *Arizona State University*, October 26, 2009.
12. "Nanomagnet Logic", invited presentation at *DARPA-sponsored Spin Logic Day*, July 24, 2009.
13. "Nanomagnet Logic (NML)", invited *NRI Architecture Benchmarking Teleseminar*, June 16, 2009.
14. "MINDing the (Performance Scaling) Gap: How New Computing Technologies Could Make Your Computer Faster and Cooler", invited seminar at *Indiana University, South Bend*, April 9, 2009.
15. "Computing with Nearest Neighbor Interactions: A Nanomagnetic Implementation," invited seminar at *Hope College*, October 24, 2008.
16. "Magnetic QCA: From Devices to Circuits to Architecture (and back!)," invited seminar at *Brown University*, October 2, 2008.
17. "Architectures and Killer Applications for Quantum-dot Cellular Automata (QCA)," invited presentation at *Nano and Giga Challenges in Electronics*, Phoenix, Arizona, March 12-16, 2007.
18. "Quantum-dot Cellular Automata Systems," invited presentation at *Frontiers of Extreme Computing*, October 23-27, 2005, Santa Cruz, CA, USA.

Patents

1. G. H. Bernstein, S. Hu, M. Niemier, W. Porod, M. T. Alam, and E. Varga, "Non-Majority MQCA Magnetic Logic Gates and Arrays Based on Misaligned Magnetic Islands," UND-10-029; P1231 - L&P Ref: CU-8431. Issued 11/15/11 – 8,058,906.

Grants and Sponsored Programs

1. Active – Sandia National Labs

Title	Heterogeneous CPU-GPU architectures for high performance computing
PIs	Danny Chen, Xiaobo S. Hu (PI), **Michael T. Niemier**
Source	Sandia National Labs
Amount	$147,529
Dates	04/18/12 – 04/18/13
Location	University of Notre Dame
Effort	0.5 summer months

2. Active – NSF

Title	NEB: Physics-Inspired Non-Boolean Computation based on Spatial-Temporal Wave Excitations
PIs	Gary H. Bernstein, Gyorgy Csaba, Xiaobo S. Hu, **Michael T. Niemier**, Wolfgang Porod (PI)
Source	National Science Foundation
Amount	$1,600,000 (+$200,000 from SRC NRI)
Dates	09/01/11 – 08/31/15
Location	University of Notre Dame
Effort	1 summer months

3. **Active – Funded by DARPA**

Title	Nanomagnet Logic
PIs	**ND:** Gary Bernstein, George Csaba, Sharon Hu, Joe Nahas, **Michael Niemier**, Alexei Orlov, and Wolfgang Porod (PI) **UCB:** Jeffery Bokor, Ramamoorthy Ramesh, and Sayeef Salahuddin **IBM:** Stuart Parkin **TUM:** Markus Becherer, Paolo Lugli, Doris Schmitt-Lansiedel
Source	Defense Advanced Research Projects Agency, Department of Defense, U.S.
Amount	$4,279,367
Dates	10/01/10 – 03/01/15
Location	University of Notre Dame
Effort	2 summer months

4. **Active – Funded by IBM**

Title	Benchmarking Emerging Technologies: Looking up to Applications
PIs	**Michael Niemier (PI)**
Source	IBM (faculty award)
Amount	$30,000
Dates	No expiration
Location	University of Notre Dame
Effort	0 summer months

5. **Active – Funded by SRC NRI**

Title	Midwest Institute for Nanoelectronics Discovery (MIND) – Phase 1.5
PIs	**ND:** Gary Bernstein, Gyorgy Csaba, Patrick Fay, Sharon Hu, Depdeep Jena, Thomas Kosel, Joe Nahas, **Michael Niemier**, Wolfgang Porod, Alan Seabaugh, Grace Xing **PSU:** Suman Datta, Theresa Mayer, Vjiay Narayanan **Purdue:** Joerg Appenzeller, Gerhard Klimeck **UT Dallas:** Jiyoung Kim, R.M. Wallace
Source	Nanoelectronics Research Corporation
Amount	$2,200,986
Dates	1/1/11 – 12/31/12
Location	University of Notre Dame
Effort	1 summer month

6. **Active – Funded by ONR**

Title	Radiation-Hard Nanomagnetic Logic with Electronic Input and Output
PIs	**ND:** Gary Bernstein, Sharon Hu, **Michael Niemier**, and Wolfgang Porod **Crane:** Steve Clark, Lydell Evans, Matthew Kay **NRL**: Mark Johnson
Source	Department of the Navy, Office of Naval Research
Amount	$482,671
Dates	09/01/09 – 12/31/10 (under no cost extension)
Location	University of Notre Dame
Effort	1 summer month

7. Active – Funded by Notre Dame's Provost Initiative

Title	Center for Nanoscience and Technology
PIs	Notre Dame's Center for Nanoscience and Technology (NDNano) faculty
Source	Notre Dame Strategic Academic Planning
Amount	~$8,000,000
Dates	Awarded 2008
Location	University of Notre Dame
Effort	0 summer months

8. Completed – Funded by DARPA

Title	Critical Technologies, Architecture
PIs	Lead: Sandia National Labs; ND Faculty: P. Kogge and **M. Niemier**
Source	Defense Advanced Research Projects Agency, Department of Defense, U.S.
Amount	$280,000 to Notre Dame; $1,050,000 requested for program via Sandia
Dates	10/05/10 – 6/24/12
Location	University of Notre Dame
Effort	1 summer month

9. Completed – Sandia National Laboratories

Title	Codesign for Exascale Computing
PIs	Danny Chen, X. Sharon Hu (PI), **Michael Niemier**
Source	Sandia National Laboratories (SNL-DOE), US
Amount	$75,000
Dates	4/11/11 – 09/30/11
Location	University of Notre Dame
Effort	0 summer months

10. Completed – Funded by NSF

Title	MRI: Acquisition: Characterization of and I/O for Magnetic Logic Structures
PIs	Gary Bernstein (PI), Sharon Hu, **Michael Niemier**, and Wolfgang Porod
Source	National Science Foundation; Engineering Directorate; Electrical, Communication, and Cyber Systems
Amount	$658,070
Dates	9/12/09 – 6/30/11
Location	University of Notre Dame
Effort	0 summer months

11. Completed – Funded by NSF

Title	Design and Study of Self-Assembling QCA Circuits
PIs	Marya Lieberman and **Michael Niemier (PI)**
Source	National Science Foundation, CISE Directorate
Amount	$300,000
Dates	8/1/06 – 7/31/11

Location	University of Notre Dame
Effort	0.5 summer months

12. Completed – Sandia National Laboratories

Title	Quilt Packaging for High Performance Computing
PIs	Gary Bernstein (PI) and **Michael Niemier**
Source	Sandia National Laboratories (SNL-DOE), US
Amount	$85,000
Dates	8/01/10 – 05/31/11
Location	University of Notre Dame

13. Completed – Funded by SRC NRI

Title	Midwest Institute for Nanoelectronics Discovery (MIND)
PIs	**ND:** Gary Bernstein, Patrick Fay, Sharon Hu, Depdeep Jena, Thomas Kosel, **Michael Niemier**, Wolfgang Porod, Alan Seabaugh (PI), Grace Xing **Ga. Tech:** Y.P. Chen and Z. Jiang **PSU:** Suman Datta, Theresa Mayer, Vjiay Narayanan, Darrell Schlom **Purdue:** Michael Capano, Gerhard Klimeck, Peide Ye **UI:** Eric Pop **UM:** Pinaki Mazumder **UT Dallas:** M.J. Kim and R.M. Wallace
Source	Nanoelectronics Research Corporation
Amount	$3,100,000
Dates	4/1/08 – 3/30/11
Location	University of Notre Dame
Effort	1 summer month

14. Completed – Funded by NSF

Title	Applications, Architectures, and Circuit Design for Nanoscale Magnetic Logic Devices
PIs	Gary Bernstein, Sharon Hu, **Michael Niemier (PI)**, and Wolfgang Porod
Source	National Science Foundation, CISE Directorate; Emerging Models and Technologies
Amount	$300,000 + $100,000 from ND
Dates	9/1/06 – 8/30/10
Location	University of Notre Dame
Effort	0 summer months

15. Completed – Funded by DOD

Title	Blending Processing into Advanced Memory Technologies to Enhance Massive, Memory-critical Applications
PIs	**ND:** Gary Bernstein, Jay Brockman, X. Sharon Hu, Peter Kogge (PI), **Michael Niemier**, and Wolfgang Porod **Cal Tech:** Ed Upchurch
Source	Department of Defense

Amount	$980,153
Dates	03/04/08 – 03/03/10
Location	University of Notre Dame
Effort	1 summer month

16. Completed – Funded by Sandia National Labs

Title	Quilt Packaging for High Performance Computing
PIs	Gary Bernstein (PI) and **Michael Niemier**
Source	Sandia National Labs
Amount	$50,000
Dates	09/24/08 – 09/30/09
Location	University of Notre Dame
Effort	0 summer months

17. Completed – Funded by Sandia National Labs

Title	Quantum-dot Logic to Extend Moore's Law
PIs	**Sandia:** Erik DeBenedictis (PI) **ND:** Peter Kogge, Craig Lent, **Michael Niemier**, and Greg Snider.
Source	Sandia National Labs
Amount	$500,000
Dates	04/01/06 – 08/01/07
Location	University of Notre Dame
Effort	0 summer months

18. Completed – Funded by NSF

Title	NSF NER: Automatic Placement Algorithms for Quantum-dot Cellular Automata
PIs	Sung Kyu Lim (PI) and **Michael Niemier**
Source	National Science Foundation, CISE Directorate
Amount	$74,208
Dates	10/01/04 – 09/30/05
Location	Georgia Institute of Technology
Effort	0 summer months

Current Graduate Research Assistants

In Computer Science and Engineering:

1. Aaron Dingler (solely advised by Niemier)
    - Work accepted to present at DAC Ph.D. forum – 2012.
    - Best paper award at IEEE/ACM Symposium on Nanoscale Architectures, 2009
2. Steven Kurtz (solely advised by Niemier)
    - Awarded IBM gradate research fellowship in February 2012
    - Work accepted to present at DAC Ph.D. forum – 2012.
3. Indranil Palit (co-advised with Sharon Hu)
4. Robert Periconne (co-advised with Sharon Hu)
5. Shiliang (Shawn) Liu
    - (not an official co-advisor, but meet regularly with Shawn and write papers with him)

In Electrical Engineering

1. Wayne Buckhanan (co-advised with Gary Bernstein)
2. M. Jafar Siddiq (co-advised with Gary Bernstein)

Past Graduate Research Assistants

1. Michael Crocker
    - (not an official co-advisor, but I met regularly with Michael and wrote papers with him)
2. M. Tanvir Alam (Ph.D. in Electrical Engineering, co-advised with Gary Bernstein)
    - Co-advised with Gary Bernstein
    - Initial appointment post-graduation as a post-doctoral researcher at University of California, Berkeley
3. Michael Putney
    - (left program for Air Force)
4. Jarrett DeAngelis
    - (M.S. in Computer Engineering)

Current Undergraduate Research Assistants

1. Craig Cahilane

Past Undergraduate Research Assistants

1. Zack Capozzi
    - Fall 2006 – Spring 2007
    - M.T. Niemier, X.S. Hu, M. Lieberman, M. Crocker, Pavan Sadarangani, **Zack Capozzi**, and Tim Dysart, "Using DNA as a Circuitboard for a Molecular QCA PLA," in the *Proceedings of Foundations of Nanoscience (FNANO06)*, p. 96-107, April 23 - April 27th, 2006.
2. Michael Garrison
    - Fall 2008 – Spring 2009
    - A. Dingler**,** M.T. Niemier, X.S. Hu, M.T. Alam, and **M. Garrison**, "System-Level Energy and Performance Projections for Nanomagnet-based Logic," in *Proceedings of the IEEE Symposium on Nanoscale Architectures*, p.21-26, July 30-31, 2009 (best paper award).
3. Leonard Gianonne
    - Summer 2008 – Spring 2009
4. Michael Jewell
    - Fall 2006 – Spring 2007
5. Peter Nistler
    - Spring 2007 – Spring 2008
6. Raymond Powers
    - Fall 2006 – Spring 2007
7. Pavan Sadarangani
    - Fall 2006 – Spring 2007
    - M.T. Niemier, X.S. Hu, M. Lieberman, M. Crocker, **Pavan Sadarangani**, Zack Capozzi, and Tim Dysart, "Using DNA as a Circuitboard for a Molecular QCA PLA," in the *Proceedings of Foundations of Nanoscience (FNANO06)*, p. 96-107, April 23 - April 27th, 2006.
8. Mike Sizemore
    - Spring 2010
9. A.J. Sporinsky
    - Fall 2006 – Fall 2007
10. Marcus Tor Strickland

- Summer 2009

11. Matthew Drummond
    - Fall 2010 – Spring 2011
12. Evan Lent
    - Spring 2009 – Spring 2010
    - Aaron Dingler, Michael T. Niemier, Xiaobo Sharon Hu, and **Evan Lent**, "Performance and Energy Impact on Locally Controlled NML Circuits," in *ACM Journal on Emerging Technologies in Computing*, 7(1), p. 1-24, 2011.
13. Ryan Turner
    - Fall 2010
    - (Began research after participating in my EG 111/112 special section.)
14. Oisin Brogan
    - Summer 2012

Classes Taught

Year	Course #	Course Title	Enrollment	Overall Impression (with 5.0 as a high)				Responses
S12	CSE 40322 CSE 60321	Computer Architecture II / Advanced Computer Architecture	38	**Inst.** **4.7**	Univ. 4.2	Div. 4.0	Dept. 3.9	34 / 38
F11	CSE 30321	Computer Architecture I	57	**Inst.** **4.4**	Univ. 4.1	Div. 3.9	Dept. 3.6	46 / 57
S11	CSE 40547 CSE 60547	Computing at the Nanoscale	5	**Inst.** **4.6**	Univ. 4.1	Div. 3.9	Dept. 4.0	5/5
F10	CSE 30321	Computer Architecture I	50	**Inst.** **4.2**	Univ. 4.0	Div. 4.0	Dept. 3.6	41 / 50
S10	EG 112	Introduction to Engineering	25	**Inst.** **4.7**	Univ. 4.1	Div. 3.9	Dept. 4.2	21 / 25
F09	CSE 30321	Computer Architecture I	34	**Inst.** **4.1**	Univ. 4.1	Div. 4.0	Dept. 4.1	30 / 34
S09	CSE 40547 CSE 60547	Computing at the Nanoscale	6	**Inst.** **3.3**	Univ. 4.1	Div. 4.0	Dept. 3.7	3 / 6
F08	CSE 30321	Computer Architecture I	42	**Inst.** **4.2**	Univ. 4.0	Div. 4.0	Dept. 4.0	27 / 42

Departmental Service Activities

- Graduate Studies Committee (2008-present)
- NSF Graduate Research Fellowship Preparation (2008, 2009)
- Ad hoc committee to revise qualifying exam (2010)

External Service Activities

- Program Committees:
    - Computing Frontiers (2007)
    - DAC Ph.D. forum (2007, 2009, 2010, 2011)
    - DAC (2011, 2012)
    - DATE (2012, 2013)
    - GLSVLSI (2008, 2009, 2010, 2011)
    - IEEE Symposium on Nanoscale Architectures (2008, 2009, 2010, 2011)
    - IEEE Symposium on Nanoscale Networks (2007)
    - NDCS (2008)
- Conference External Reviewer:
    - CODES-ISSS (2008)

  - DAC (2007)
  - DSN (2007)
  - VLSI Design Conference (2007)
- Journals:
  - ACM JETC (2008, 2009, 2010, 2011, 2012)
  - IEEE T-NANO (2007, 2008, 2009, 2010, 2011, 2012)
  - IEEE T-Computer (2009, 2010)
  - IEEE T-CAD (2010)
  - IEEE T-CAS (2008)
  - IEEE T-VLSI (2010, 2012)
  - IOP Nanotechnology (2007)
  - JVST-A (2008)
  - Nanotechnology (2012)
- Proposal Review:
  - NSF EMT Panel (2007, 2008)
  - NSF Nanocomputing Panel (2009)
  - NSF PIRE External Reviewer (2008)
  - NSF CISE Panel (2011)
  - Israel Science Foundation (2011, 2012)