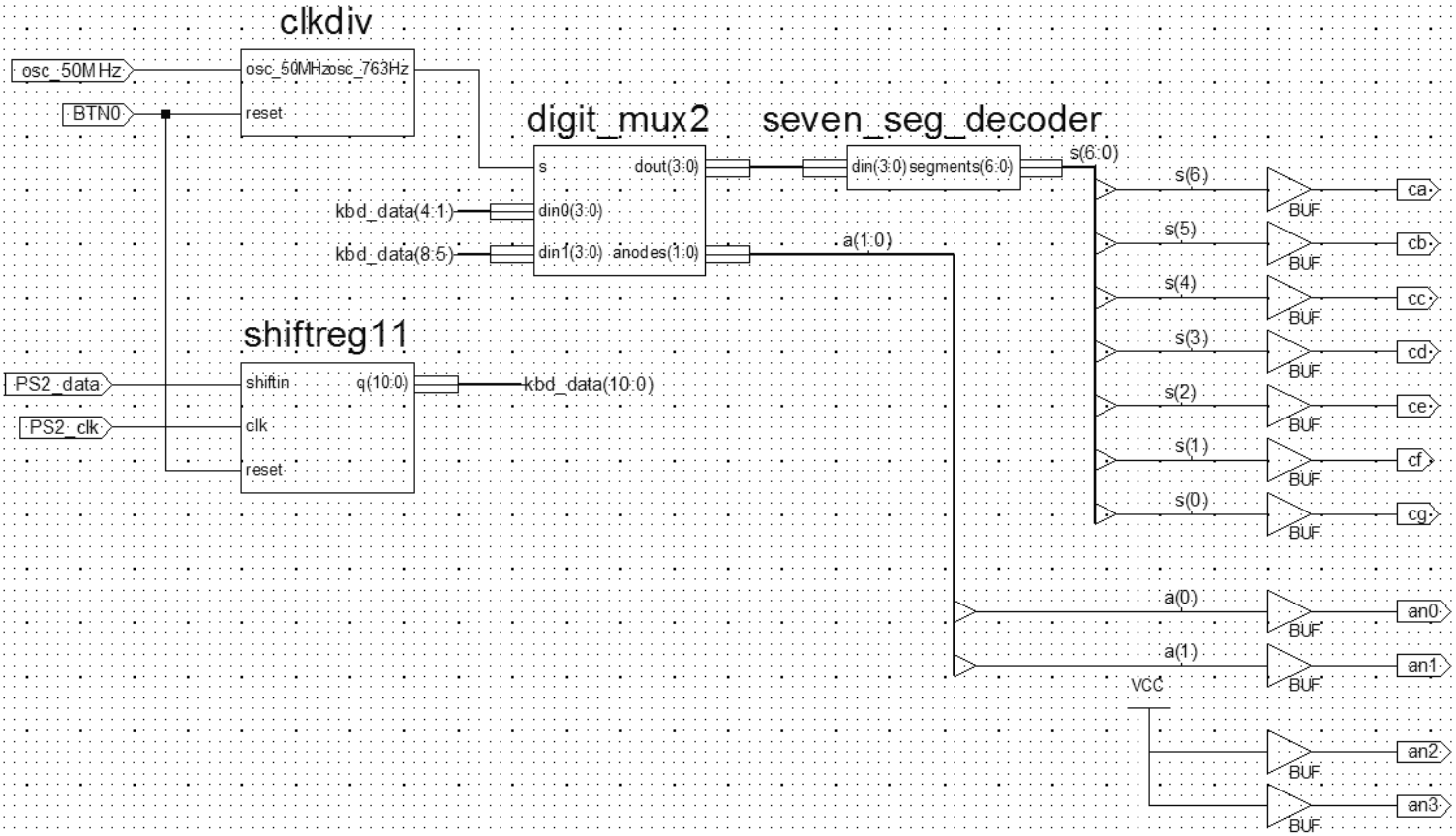
# *Interfacing to a PS/2 Keyboard and Seven-Segment Display*

### *CSE 20221 Logic Design, University of Notre Dame*
### *Due Thursday April 19, 2007*

## Description

For this assignment, you will develop a working interface to a PS/2 keyboard that displays the 8-bit key code as 2 hex digits on a seven-segment display. The first part of the assignment is to implement the design with Verilog modules wired together in a schematic using the Xilinx ISE WebPack tools. The second part of the assignment is to synthesize a bit file and download the design into a Xilinx FPGA on the Digilent Basys board and demonstrate it in the lab.

The figure below shows the top-level schematic that you should use for your design. It contains 4 modules that must each be described with Verilog.




The interface and behavior of each of these modules is as follows:

**clkdiv:** This module takes a 50 MHz clock signal (from FPGA pin P36 on the Basys board) and divides this by 65,536 ($2^{16}$) to obtain a clock frequency of 763 Hz, which is a reasonable frequency for cycling between the digits of the seven-segment display. Inside, this is basically just a 16-bit counter, where the most significant bit is the output clock. In addition to the input and output clocks, this module also has a reset input.

**shiftreg11:** This is an 11-bit shift register that captures the serial output from the keyboard when a key is pressed. It has inputs for the clock and data lines of a PS/2 keyboard as well as a reset, and has an 11 bit parallel output.

**seven_seg_decoder:** This module takes a 4-bit binary number as input and produces 7 bits of output, corresponding to the cathodes of each of the 7 segments of a display digit. The module should decode the input value and light up the appropriate segments to display a hex digit 0-F. Note: Display the hex digits A, C, E, and F as capital letters and b and d as lower case letters. Light up the top segment when displaying a "6" to distinguish it from a "b".

**digit_mux2:** This module multiplexes between the upper and lower 4 bits of the 8 bit keycode stored in the shift register, to send to the seven segment decoder. It also generates the signals for enabling the anodes of each of the two digits of the seven segment display. Its inputs are the two 4-bit values of the upper and lower hex digits of the keycode and a select signal driven by the low-frequency clock. The outputs are selected 4-bit input signal and a 2-bit signal to drive the 2 digit anodes.

## Deliverables and Due Dates

This assignment has two deliverables: (1) design and simulation using Verilog and the Xilinx ISE WebPack; (2) hardware demonstration on the Digilent Basys board.

Like you did for the mini-project, you should create a testbench for each module to verify that it works, and then create a testbench for the fully integrated design. Note that you won't be able to simulate the full 16-bit clock divider—it takes too many cycles! Instead, use a 1-bit counter for simulation purposes, which divides the input frequency in half.

Your report for this assignment should simply consist of the following:

1. 100-200 word abstract
2. List of Verilog modules and schematic(s) in the order attached to the report
3. List of testbenches for simulations with brief descriptions, in order attached
4. Attached source code for Verilog modules and schematic(s)
5. Attached simulation results

After you've completed your simulations, you can download your design to a Basys board and demonstrate it to a lab TA. You must have simulated your design before you can check out a board. Reports and demonstrations are due by **Thursday, April 19**.

## Collaboration

For this assignment, you can either work alone or with **one** partner (no more than one). If you choose to work with a partner, each of you must design one sequential module (clkdiv or shiftreg11) and one combinational module (digit_mux2 or seven_seg_decoder). You only need to turn in 1 report between you, and must have both names on the report. Also you must add a paragraph describing who did what.

## Lab Times

There will be lab times available for working with the Basys boards between Wednesday April 11 and Thursday April 19. Sign-ups for lab times are on the Wiki. Get started early and finish early—don't wait till the end!