Estimating Relative Logic Area from Xilinx Synthesis

Without doing a full VLSI chip layout for your design, there is no way to know *exactly* how much area it will take in hardware. That said, it is fairly easy to make relative comparisons between your modified design and the baseline six-instruction design using another metric that is provided by the Xilinx synthesis toolchain. As you may remember from Logic Design, the Xilinx tools map your design into macrocells on an FPGA, where each macrocell contains some configurable unit of logic: a look-up table, some flip-flops, and perhaps some other special-purpose hardware. Xilinx will report the number of look-up tables (LUTs), flip flops, and other macrocell components used for a given design after it is synthesized.

In order to synthesize the base six-instruction processor, a few changes need to be made. First, the way that we have done memories, using large Verilog arrays, is fine for a behavioral simulation but does not match what would happen in hardware – your data memory will consume one flip-flop per bit, whereas a real DRAM chip uses a dense, special-purpose array of very small components. Including the memories will throw off the estimate of logic complexity, so we will simply exclude the memories for the purpose of this estimation. A modified `processor.v` has been posted on the course website for this purpose. Essentially, the modification comments out the instantiations of $\texttt{inst}_{mem}$ and $\texttt{data}_{mem}$, and then brings their address and data lines out as external processor ports so that the logic is not optimized away. This mirrors how a real CPU core would work. After using this modified top-level source (or else modifying your own accordingly), run a synthesis on your design in Xilinx ISE. If you do not already have the Design Summary open, you can open it by selecting the toplevel (processor.v) in the design hierarchy when "Synthesis/Implementation" is selected, and then double-clicking "View Design Summary" in the Processes sidebar. The "Device Utilization Summary" section has several important statistics.

For the purposes of this comparison, we will look at the "Total equivalent gate count for design" estimate that Xilinx provides. This number is a good summary of the various detailed resource counts that the tools report. The baseline six-instruction processor, as provided on the course website, had an equivalent gate count of 8462 in Xilinx ISE 10.1. You should be able to estimate impact to circuit area that your modifications have fairly confidently by comparing to this number.