

Name: _____

CSE 30321 – Computer Architecture I – Fall 2008
Final Exam
December 18, 2008

Test Guidelines:

1. Place your name on EACH page of the test in the space provided.
2. Answer every question in the space provided. If separate sheets are needed, make sure to include your name and clearly identify the problem being solved.
3. Read each question carefully. Ask questions if anything needs to be clarified.
4. The exam is open book and open notes.
5. All other points of the ND Honor Code are in effect!
6. Upon completion, please turn in the test and any scratch paper that you used.

Suggestion:

- Whenever possible, show your work and your thought process. This will make it easier for us to give you partial credit.

Question	Possible Points	Your Points
1	10	
2	15	
3	15	
4	15	
5	20	
6	10	
7	15	
Total	100	

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Problem 1: (10 points)

Assume that you have a 4-way, *set-associative* cache with:

- 8192 *total blocks*
- 32 words per block
- 64 bits per word
- 64 bits per physical address

Question A: (7 points)

If addresses are *to the word* what bits of the address will comprise the index, tag, and offset?

Question B: (3 points)

If addresses are to the byte, how – if at all – does the above change?

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Problem 2: (15 points)

Question A: (7 points)

Assume you have space on your chip to make a cache that is direct mapped and 32 KBytes. The processor that you are designing will be used primarily for handling memory requests that occur randomly (e.g. not sequentially). In most cases, the amount of data required will only be 2-4 bytes. Given these requirements, how might you organize your cache? Why?

Question B: (8 points)

Assume that you have a direct mapped cache with 4 blocks; each block holds 4 words. It is initially empty. Addresses are to the word. Now, assume you get the following pattern of address requests (in hex):

- A B C
- A B D
- A B B
- A B F
- B B D
- A B B
- B B F
- A B C

Which requests are hits and which are misses?

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Problem 3: (15 points)

Question A: (3 points)

Is the following statement true or false?

“A miss in the TLB implies a page fault has occurred.”

Question B: (3 points)

Assume that your CPU supplies a virtual address that is 40 bits long:

F 2 5 D 3 F 0 8 0 1 (hex)

In this system:

- Physical addresses are 32 bits
- Page sizes are 4 KBytes
- The Page Table Register = 0 0 0 0 0 0 0 F (hex)

What address in the page table should contain the Virtual Page Number that we need?

Question C: (3 points)

For the address in Question B, how many bits of data should the Page Table Entry hold? (You can ignore valid bits, dirty bits, etc.)

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Question D: (3 points)

After we calculate a physical address, how many entries down in the page will we find the data we are actually looking for?

Question E: (3 points)

Assuming a clock rate of 1 GHz, which answer below best describes the number of **clock cycles** required to process a page fault (circle your answer).

1

10

1000

1,000,000

1,000,000,000,000

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Problem 4: (15 points)

This question considers the basic, MIPS, 5-stage pipeline. (For this problem, you may assume that there is full forwarding.)

Question A: (7 points)

Show how the instructions will flow through the pipeline:

	1	2	3	4	5	6	7	8	9	10	11	12
Lw \$5, 0(\$7)												
Add \$19,\$7,\$6												
Xor \$5,\$19,\$3												
Sub \$2,\$10,\$11												
Sw \$2, 0(\$1)												

Question B: (2 points)

What are the data dependencies in this instruction mix?

Question C: (2 points)

How many stall clock cycles arise due to hazards in this mix?

Question D: (4 points)

Where does the XOR instruction get its data? (Be very specific)

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Problem 5: (20 points)

This question considers the basic, MIPS, 5-stage pipeline. (For this problem, you may assume that there is full forwarding.)

Question A: (7 points)

Show how the instructions will flow through the pipeline:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Sub \$17,\$15,\$12																
Sub \$9,\$8,\$4																
Lw \$10, 0(\$5)																
Add \$1,\$10,\$2																
Add \$6,\$1,\$3																
Lw \$20, 0(\$21)																

Question B: (5 points)

What is the CPI of this instruction sequence if it is executed 1000 times?

Question C: (2 points)

How does the performance of this code compare with the ideal? Quantify your answer.

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Question D: (3 points)

How many clock cycles would 1000 iterations of the above sequence of instructions take if it were executed on a *multi-cycle* machine? (Assume loads take 5 CCs and adds take 4 CCs.)

Question E: (3 points)

If the clock cycle time of the multi-cycle machine is 80% of that of the pipelined machine, which machine is faster? By how much?

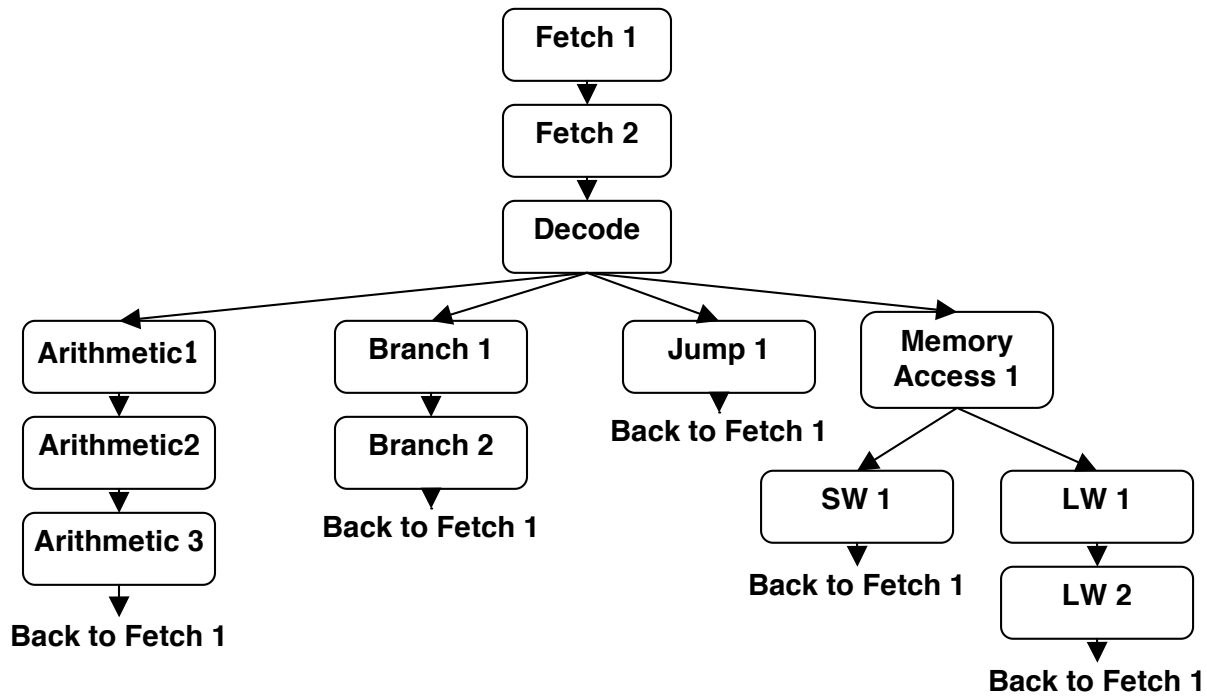
Problem 6: (10 points)

Part A: (5 points)

Assume that we have developed a datapath for a multi-cycle machine that can execute the following instructions: ADD, ADDI, AND, BEQ, BNEQ, JUMP, LW, OR, SUB and SW. The instructions are broken down into classes as follows:

Instruction Class	Instructions	Frequency of Class
Arithmetic	ADD, ADDI, AND, OR, SUB	50%
Branch	BEQ, BNEQ	20%
Jump	JUMP	10%
Memory Access	LW, SW	20% (10% loads, 10% stores)

The state machine for this particular datapath is shown below:

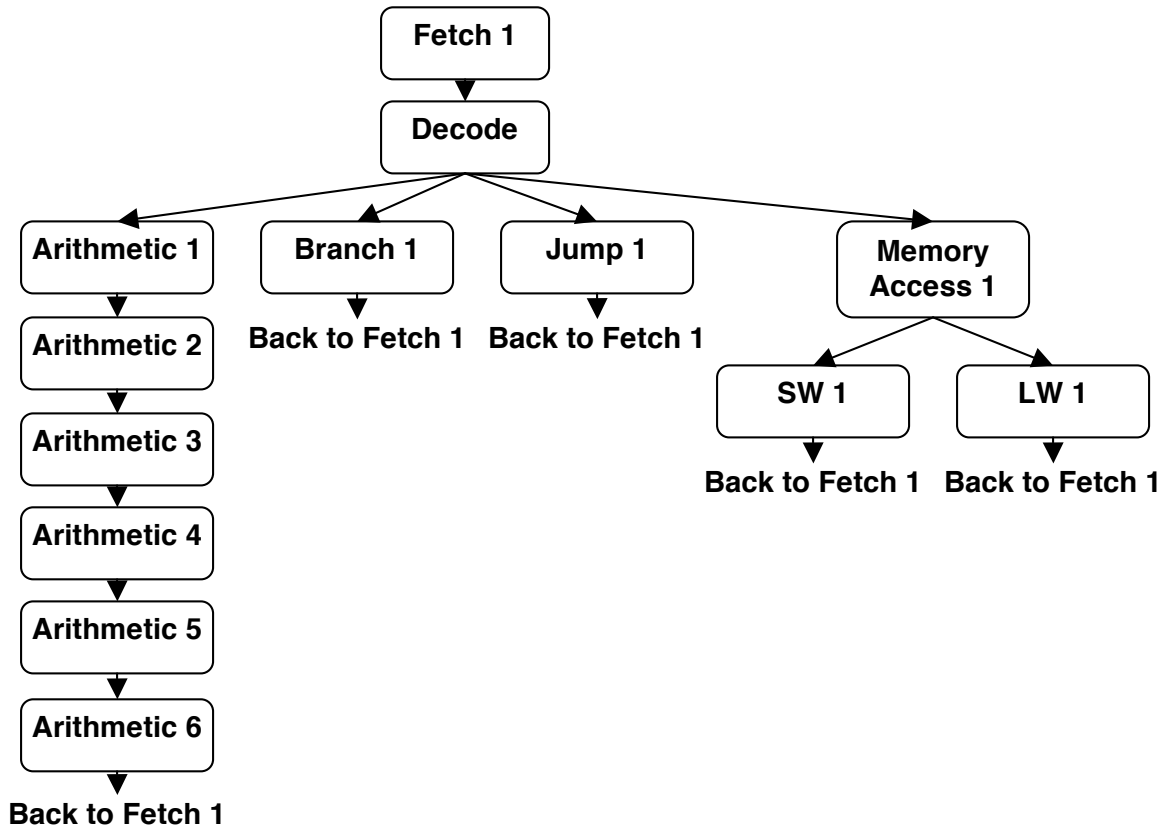


Calculate the average CPI:

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Part B: (5 points)

We have made some changes to our datapath causing some changes in the state machine. The new state machine appears below. (Note that the compiler has not changed and instruction frequencies remain the same).



Were these changes smart to make? Justify your answer (and note that a simple 'yes' or 'no' answer will earn you 0 points for this part of the problem).

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Problem 7: (15 points)

You have a dual core microprocessor that needs to execute 5 tasks. The instruction count and CPI for each task is shown in the table below. (You may assume a clock rate of 1 GHz).

Task	Instruction Count	CPI
1	400,000	1.7
2	2,100,000	2.1
3	3,000,000	1.4
4	10,000,000	1.2
5	6,000,000	1.5

Your job is to figure out which tasks should run on each core. However, there is a catch. Tasks 4 and 5 need to communicate with each other. If they are placed on separate cores, the CPI of Task 4 will rise to 2.3 and the CPI of Task 5 will rise to 3.0.

Which tasks should run on each core? Why?