Problem 1:

Assume a machine with the following characteristics:

- The CPU supplies a 64 bit virtual address.
- The 64 bit virtual address must be translated into a 64 bit physical address.
- This single core machine has 2 levels of cache.
- The clock rate is 1 GHz.

Question A:

The page table has 2^{32} entries. Determine the physical address associated with the virtual address using portions of the memory state of the machine provided below. (All addresses are in hex.)

Page Table Register: AAAA 0000 0000 0000
Virtual Address: 0000 BBBB 0000 AAAA

	Address (least significant to most significant)	Data
1	0000, 0000, 0000, 0000	FEDC, BA98, 7654, 3210
2	0000, 0000, 1111, 1111	0123, 4567, 89AB, CDEF
3	0000, 0000, AAAA, 0000	0000, 0000, 3333, 7777
4	0000, 0000, DDDD, 9988	2222, 7777, 8888, 4444
5	0000, 000F, 0000, 0000	E1E1, 0E1E, 10E1, E100
6	0000, BBBB, 0000, AAAA	0000, 0000, EEEE, FFFF
7	0000, BBBB, AAAA, AAAA	0000, 0000, 9999, 2222
8	000A, AAA0, 0000, 0000	0000, 0000, 2222, 2222
9	0BBB, AAAA, 0000, AAAA	0000, 0000, 5555, 4444
10	AAAA, 0000, 0000, 0000	0000, 0000, BBBB, CCCC
11	AAAA, 0000, 0000, BBBB	0000, 0000, FFFF, EEEE
12	AAAA, BBBB, BBBB, AAAA	1111, 0000 AAAA, 0000
13	BBBB, AAAA, 0000, 0000	0000, 0000, 9999, 1111
14	BBBB, BBBB, BBBB, AAAA	0000, 0000, 9999, 8888
15	CCCC, CCCC, DDDD, DDDD	8888, 9999, 0000, 1111
16	FFFF, CCCC, DDDD, AAAA	1111, 1111, 0000, AAAA

Goto memory location AAAA 0000 0000 0000
\+ 0000 BBBB
AAAA 0000 0000 BBBB
Get: 0000 0000 FFFF EEEE

Physical address is: FFFF EEEE 0000 AAAA

Question B:
The physical address generated above is then sent to a direct mapped, L1 cache. The L1 cache has the following characteristics:

- The cache has 4096 blocks.
- There are 256, 32-bit words in each block. Addresses are to the word.
- The cache can hold 4 MB (i.e. 4,194,304 bytes) of data.

Using the physical address found in Part A, fill in the following table:

Index	0AA
Offset	AA
Tag	FFFF EEEE 000

Physical address: FFFF EEEE 0000 AAAA

4096 Blocks → 2^{12} → 12 bits of index → 0AA

256 words/block → 2^{8} words/block → 8 bits of offset → AA

Therefore there are 64 – 12 – 8 = 44 bits of tag → FFFF EEEE 000

Question C:
Assume that you have a sequence of 3 virtual addresses that you need to convert to physical addresses. The first virtual address takes 3 nanoseconds to translate to a physical address. The second virtual address takes 300,000 nanoseconds to translate to a physical address. The third virtual address takes 100 nanoseconds to translate to a physical address. For each virtual address, *briefly* comment on the critical path of translation.

3 ns	TLB hit + cache hit
300000 ns	TLB miss + page fault
100 ns	(1) TLB Miss + Page Table Hit OR (2) TLB Hit + Cache Miss