CSE 40547/60547 – Computing at the Nanoscale– Spring 2011
Homework 02 – 3D Integration OR Emerging Device Technologies
Assigned: February 9, 2011 **– Due:** February 21, 2011

Background:

For this assignment (as well as many of the other remaining assignments) you will be asked to read a research paper whose topic runs parallel to the material that is currently being discussed in class. The core of the assignment will be to "review" the paper, as well as answer/comment on 1-2 pointed questions that I have identified.

I've specifically chosen papers that should be accessible (from a technical standpoint) to the average student taking this class. Moreover, I will allow you to pick from 1 of several papers – so that you can chose to review a paper that most closely matches your academic background *or* research interests. (Please don't be afraid to read a paper that you may be interested in, but less comfortable with. I'm happy to discuss technical points as you go through the review process.)

For each review, I will ask you to address 6 specific items / questions that are derived from Alan Jay Smith's 1999 article "The Task of the Referee" – see link on course website. These items are summarized below:

1. What is the purpose of the paper?

2. Is the goal of the work significant? Why?

3. Are the methods used to perform the research sound and valid? Why do you think so?

4. What are the conclusions of the paper?

5. In your opinion, how and / or why does the work better the state of the art?
   Comment 1: If you don't think it does, say so and explain why!
   Comment 2: If you are reading a review-type paper, please comment on whether or not you think the authors have an underlying opinion about the topic, what that opinion is, and whether or not you think the opinion is valid.

6. What are the pros and cons of the way in which the material was presented?

Finally, your review should explicitly address the 1-2 specific questions that I alluded to above. If you feel that it is easier to answer these questions in the context of the 6 questions above, that's fine, but be sure that you explicitly call out answers to these questions in the document. Alternatively, it may be better to answer the questions separately, at the end of the review.

This Assignment:

In this assignment, you will be asked to read and review 1 of 4 papers. Two of the papers review emerging device technologies (largely from an industry perspective), and two of the papers look at possible ways to leverage 3D integration technology.

The possible papers (and specific questions to address) are listed below:

Device Technologies:

Boolean Logic and Alternative Information-Processing Devices

- Authors: George Bourianoff (Intel)
  Joe E. Brewer (U. of Floriday)
  Ralph Cavin, James A. Hutchby, Victor Zhirnov (SRC)
- Link: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4519934&tag=1
- Questions:
  - Based on what you read, what do you believe are the most viable device/architecture approaches for beyond CMOS logic?
  - Why?

Device Proposals Beyond Silicon CMOS

- Authors: Paul Solomon (IBM)
- Link: http://domino.research.ibm.com/library/cyberdig.nsf/papers/C12D0D2E53FE8833852576F90055CF7E
- Questions:
  - What is Solomon's opinion as to the most viable approach for beyond CMOS computing?
  - What are Solomon's primary concerns about (all) emerging technologies?

3D Integration:

3D Stacked Memory Architectures for Multi-Core Processors

- Authors:
  - Gabriel Loh (Georgia Tech, AMD)
- Link: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4556747
- Questions:
  - Comment on the practicality of "aggressive 3D memory organizations"
  - What is the significance of thermal effects? Are the manageable?

MIRA: A Multi-Layered On-Chip Interconnect Router Architecture

- Authors:
  - Dongkook Park, Soumya Eachempati, Reetuparna Das, Asit K. Mishra, Yuan Xie, N. Vijaykrishnan, Chita R. Das (Penn State Univesity)
- Link: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=04556731
- Questions:
  - What is the impact of thermal effects if 3D integration is primarily used to support networks on chip (i.e. interconnect)?
  - Characterized the gains over the 2D based design?

As a point of reference, the review should be ~3 pages long assuming a 12 point, Helvetica font with 1" margins.