CSE 40547/60547 – Computing at the Nanoscale– Spring 2011
Homework 03 – Three Terminal Device Alternatives + Alternative Operating Modes
Assigned: March 2, 2011 **– Due:** March 11, 2011, 11:59 p.m. via email

Assignment:
Like before, for this assignment you will be asked to read research papers whose topics run parallel to the material that is currently being discussed in class. The core of the assignment will be to read **TWO** of 6 papers, and answer/comment on the pointed questions that I have identified. Essentially, there is 1 paper on each of the three terminal alternatives (or different operating modes) that we have discussed in class. The exception is the TFET – where you can choose to read one of two similar papers. (Note that you cannot read *both* TFET papers.)

Because I am asking you to read 2 papers, you do not need to do a "review" as before. You just need to answer the questions. As a point of reference, the document that you turn in should be ~3 pages long assuming a 12 point, Helvetica font with 1" margins. (Thus, about 1.5 pages per paper.) The possible papers (and specific questions to address) are listed below:

Lecture 07: CNTFETs
- *Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits*
  - Nishant Patil, Jie Deng, Subhasish Mitra, and H.-S. Philip Wong
  - IEEE Transactions on Nanotechnology
  - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4663869
- *Questions:*
  - Why are multiple carbon nanotubes used / needed to make a given logic gate?
    - (What is an "optimal" number of tubes in your opinion?)
  - Quantitatively, how does this technology compare to scaled CMOS?
    - (In your opinion, is it worth investing in?)

Lecture 08: FinFETs
- *Evaluation of Multiple Supply and Threshold Voltages for Low-Power FinFET Circuit Synthesis*
  - Prateek Mishra, Anish Muttreja, and Niraj Jha
  - IEEE International Symposium on Nanoscale Architectures, p. 77-84, 2008.
  - http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4585795
- *Questions:*
  - How was the Threshold Control through Multiple Supply (TCMS) mechanism made extensible to the design of any logic circuit?
    - (In your opinion, is this scheme practical? Why or why not?)

Lecture 09: TFETs
- *Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)*
  - Daeyeon Kim, Yoonmyung Lee, Jin Cai, Isaac Lauer, Leland Chang, Steven J. Koester, Dennis Sylvester, David Blaauw
  - ISLPED, August 19th-21st, 2009.
  - *http://portal.acm.org/citation.cfm?id=1594287*

OR

- *A Novel Si-Tunnel FET based SRAM Design for Ultra-Low Power 0.3 V VDD Applications*
  - J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta‡, N. Vijaykrishnan, D. Pradhan
  - ASP-DAC, January 18-21, 2010, p. 181-186
  - *http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5419897*
- *Questions (for either paper):*
  - Explain why (with TFETs) an SRAM cell must be redesigned.
  - Explain how and why a re-designed TFET SRAM cell works.
  - Quantitatively, how does a TFET SRAM compare to a CMOS SRAM? Be sure to note metrics used.

Lecture 10: Subthreshold CMOS

- *Energy Optimization of Subthreshold-Voltage Sensor Network Processors*
  - Leyla Nazhandali, Bo Zhai, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Sanjay Pant, Todd Austin and David Blaauw
  - Proceedings of the 25th International Symposium on Computer Architecture, p. 197-207, June 4-8, 2005.
  - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1431557
- *Questions:*
  - What architectural-level tradeoffs must be considered in the design of a subthreshold *processor*?
    - (Don't just make a list – briefly discuss.)
  - Briefly describe the characteristics of the designs on the pareto-optimal curve. (In other words, what characteristics do they have?)
    - In your opinion, why do you think that these designs have proven to be optimal?

Lecture 11: NEMS Relays

- *Integrated Circuit Design with NEM Relays*
  - Fred Chen, Hei Kam, Dejan Markovic, Tsu-Jae King Liu, Vladimir Stojanovic, Elad Alon
  - Proceedings of International Conference on Computer Aided Design, San Jose, CA, p. 750-757, November 10-13, 2008.
  - *http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4681660*
- *Questions:*
  - What is the impact on load capacitance on the benchmarks simulated in this paper?
    - Why were multiple loads considered?
  - What would an optimal relay-based circuit design look like?
    - In your opinion what are the challenges in designing such a circuit (use the adder as context).
  - From the standpoint of throughput, how do NEMS relay-based adders compare to CMOS equivalents?