CSE 40547/60547 – Computing at the Nanoscale– Spring 2011
Homework 04 – Nanowire crossbar architectures and devices
Assigned: March 21, 2011 **– Due:** March 30, 2011, 11:59 p.m. via email

Assignment:

Like before, for this assignment you will be asked to read research papers whose topics run parallel to the material that is currently being discussed in class. The core of the assignment will be to read a subset of papers, and answer/comment on the pointed questions that I have identified.

Like the last assignment, you do not need to do a "review. You just need to answer the questions. As a point of reference, the document that you turn in should be ~3 pages long assuming a 12 point, Helvetica font with 1" margins. (Thus, about 1.5 pages per paper.)

Below, I have specified four documents that you may want to / will need to review to complete this assignment. Two papers address memristor technology, and two papers address nanowire crossbar processors. (You may not need to read every last word of each paper, but I have included them all for your reference.)

Memristors

- *Papers:*
  - *The missing memristor found*
    - Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart, and R. Stanley Williams
    - *Nature*, Vol 453, May 1, 2008, p. 80-83.
    - http://www.nature.com/nature/journal/v453/n7191/abs/nature06932.html
  - *How we found the missing memristor*
    - R. Stanley Williams
    - IEEE Spectrum, December, 2008, p. 29-35
    - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4687366
- *Questions:*
  - Explain how a memristor can be programmed and then used to perform logic and/or memory operations. Your answer should make reference to the "bow tie" curves discussed in both of the papers listed above.
  - In your opinion, is it possible to "wreck" a device during programming? (i.e. is there a way that one could render a device unusable?)
  - In your opinion, what is the ultimate viability of this device technology? (While supporting your answer with references from the literature is good, I am in essence interested in your opinion. A short paragraph will suffice as an answer to this question.)

Nanowire Crossbar Processors

- *Papers:*
  - *Programmable nanowire circuits for nanoprocessors (paper)*
    - Hao Yan, Hwan Sung Choe, SungWoo Nam, Yongjie Hu, Shamik Das, James F. Klemic, James C. Ellenbogen, Charles M. Lieber
    - *Nature*, Vol. 240, February 10, 2011, p. 240-244.
    - *http://www.nature.com/nature/journal/v470/n7333/full/nature09749.html*
  - *Programmable nanowire circuits for nanoprocessors (supplement)*
    - Hao Yan, Hwan Sung Choe, SungWoo Nam, Yongjie Hu, Shamik Das, James F. Klemic, James C. Ellenbogen, Charles M. Lieber
    - *Nature*, Vol. 240, February 10, 2011, p. 240-244.
    - *http://www.nature.com/nature/journal/v470/n7333/extref/nature09749-s1.pdf*
- *Questions:*
  - How does the fabricated processor differ from the nanowire crossbar architectures discussed in class (the basic crossbar design with stochastic restoration, CMOL/FPNI)? (For example, you might discuss/explain how a logical operation is performed, how programmability is achieved, etc.)
  - Using just the technology and approach described in this paper, could this technology better the state of the art for CMOS (for any applications)? If not, what advances are required, what fabrication technology is required, etc.