CSE 40547/60547 – Computing at the Nanoscale– Spring 2011
Homework 06 –Memory Technology OR Memory Technologies Impact on Architecture
Assigned: April 25, 2011 **– Due:** May 4, 2011, 11:59 p.m. via email
Note: Assignments turned in by May 6, 2011, 11:59 p.m. via email will not be considered late.

Assignment:
In this assignment, you will study the viability and impact of emerging memory technologies. You need to investigate one of two topics: **(1)** racetrack memory (where the assignment will be more technology/architecture-based) OR **(2)** phase change memory (PCM) (where the assignment will be more focused on how emerging memory technologies can affect systems-level performance.)

More specifically, for a given technology, you will need to address the items and questions listed below. Your final write up should be ~2.5 to 3 pages.

Like before, for each topic, I have included a list of suggested papers to look at / read. Also, like previous assignments, I do not expect you to read and completely understand every last word of every last paper, but I have included multiple references such that you can address all of the items below. Note that the order in which the papers are listed represents how useful I found each paper to be (i.e. the first paper listed was probably the most useful – and also served as a good introductory overview of a given topic).

Racetrack
- *Papers:*
  - Data in the Fastlane of Racetrack Memory
    - Stuart S. P. Parkin
    - Scientific American
    - http://www.cs.virginia.edu/~robins/Racetrack_Memory.pdf
  - Magnetic Domain-Wall Racetrack Memory (supporting online material)
    - Stuart S. P. Parkin
    - *Science* 320, 190 (2008)
    - http://www.sciencemag.org/cgi/content/full/320/5873/190/DC1
  - Magnetic Domain-Wall Racetrack Memory
    - Stuart S. P. Parkin
    - *Science* 320, 190 (2008)
    - http://www.sciencemag.org/content/320/5873/190.short
  - Dynamics of Magnetic Domain Walls Under Their Own Inertia
    - Luc Thomas, et al.
    - Science 330, 1810 (2010);
    - http://www.sciencemag.org/content/330/6012/1810.abstract
- *Questions:*
  - Explain how racetrack memory works.
  - Explain what obstacles exist to implementable racetrack memory. For example, are there energy concerns? Are there concerns about defects? Please be somewhat specific as to how potential obstacles could inhibit large-scale implementations. (In other words, don't just say "energy.")
  - In your opinion, are the proposed 3D racetracks feasible? Why or why not?
  - When compared to other memory technologies, how does racetrack compare in terms of energy, performance, and density?
  - In your opinion, is the memory architecture presented in the 2008 Science paper (specifically the supplement) sufficiently developed to make detailed comparisons to other memory technologies?

PCM

- *Papers:*
  - A Content-Aware Block Placement Algorithm for Reducing PRAM Storage Bit Writes
    - Brian Wongchaowart, et al.
    - Proceedings of the 26th Symposium on Mass Storage and Systems and Technologies
    - http://portal.acm.org/citation.cfm?id=1914443
  - Analyzing the Impact of Useless Write-Backs on the Endurance and Energy Consumption of PCM Main Memory
    - Santiago Bock, et al.
    - IEEE International Symposium on Performance Analysis of Systems and Software
    - http://www.cs.pitt.edu/~childers/papers/ispass2011.pdf
  - Flip-N-Write: A Simple Deterministic Technique to Improve PRAM Write Performance, Energy and Endurance
    - Cho, et al.
    - IEEE/ACM International Symposium on Microarchitecture
    - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5375405
  - Increasing PCM Main Memory Lifetime
    - Alexandre P. Ferreira, et al.
    - Design Automation and Test in Europe (DATE) 2010
    - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5456923
- *Other:*
  - Fine-Grained QoS Scheduling for PCM-based Main Memory Systems
    - Zhou, et al.
    - IEEE International Symposium on Parallel and Distributed Systems
    - http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5470451
  - A Durable and Energy Efficient Main Memory Using Phase Change Memory Technology
    - Zhou, et al.
    - International Symposium on Computer Architecture, 2009
    - http://portal.acm.org/citation.cfm?id=1555759
  - Website:
    - http://www.cs.pitt.edu/PCM/
- *Questions:*
  - Explain how phase change memory works.
  - Explain what obstacles exist to implementable phase change memory. For example, are there energy concerns? Are there concerns about defects? Please be somewhat specific as to how potential obstacles could inhibit large-scale implementations. (In other words, don't just say "energy.")
  - Why would phase change memory be useful in storage class systems?
    - (consider the scale of something like a server farm)
  - Explain what obstacles exist for using PCM in storage class data systems? What are some possible solutions to said obstacles?
  - If you had to bet on phase change memory or STT-RAM as the next dominant memory technology, which would you bet on? Why?