

# Challenges and Innovations in Nano-CMOS Transistor Scaling

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October, 2009



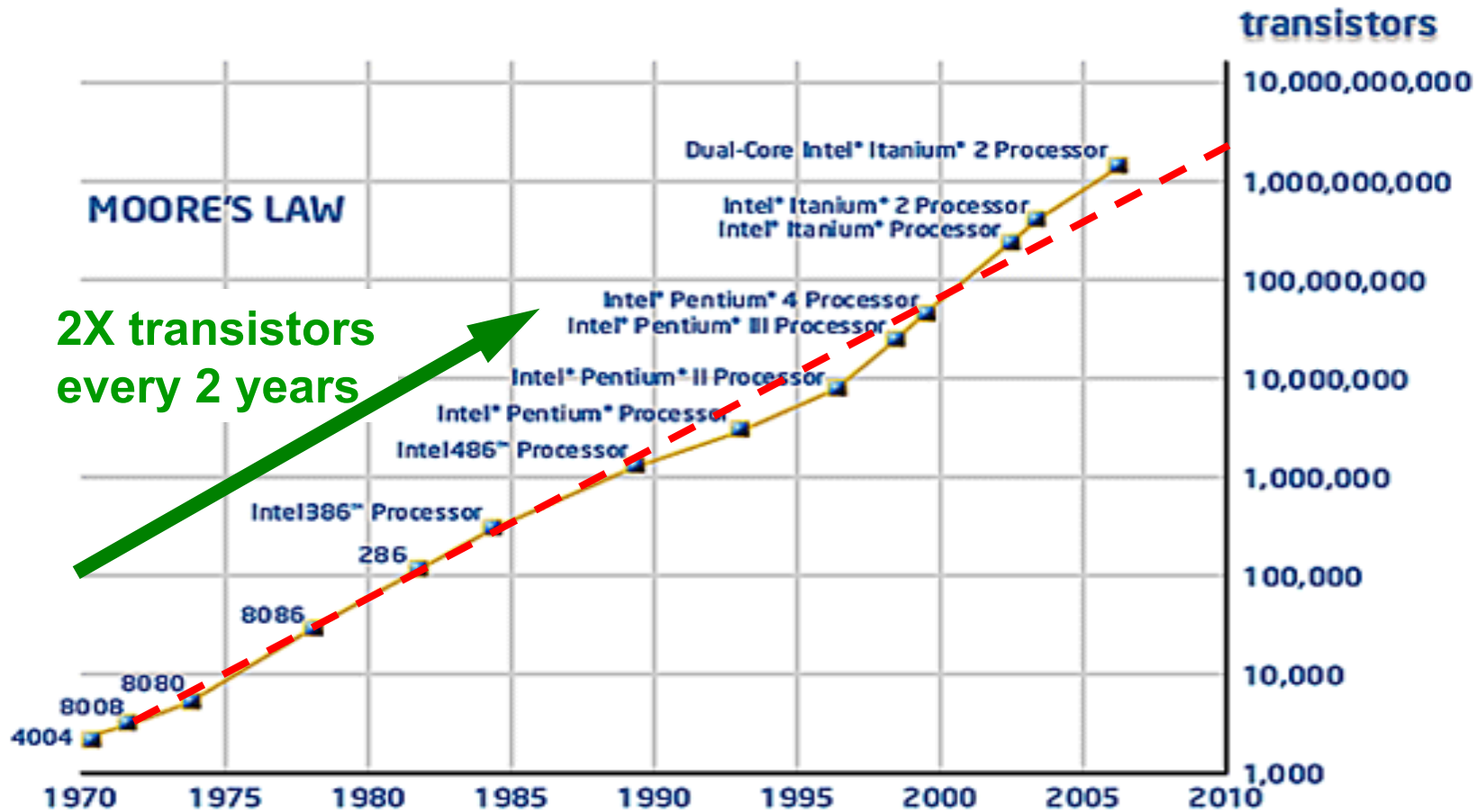
*Nikkei Presentation*

# Outline

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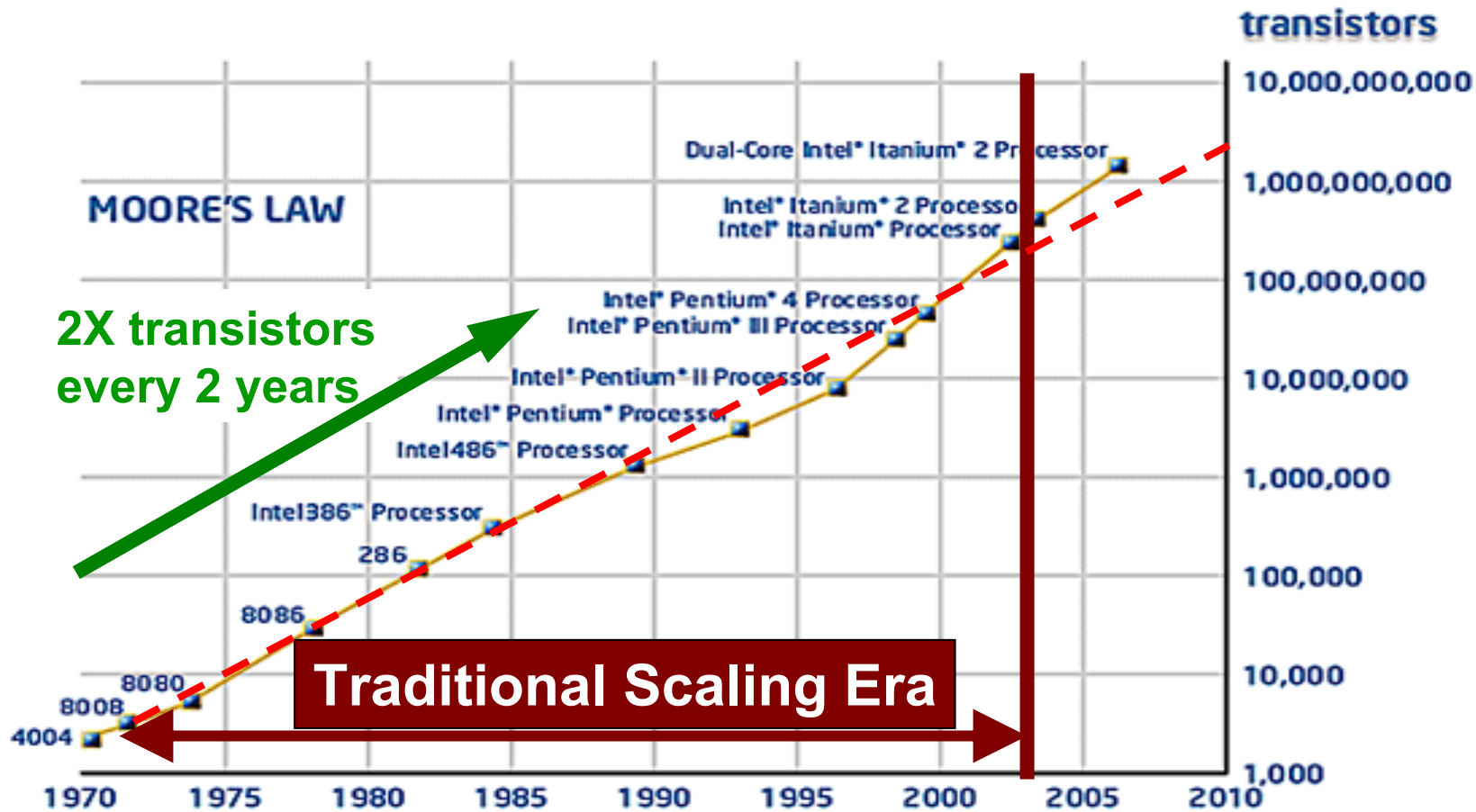
- **Traditional-Scaling**
  - Traditional Scaling Limiters, Device Implications
  - Intel's Response
- **Post “Traditional-Scaling” Innovations**
  - Mobility Booster: **Uniaxial Strain**
  - Poly Depletion Elimination: **Metal Gate**
  - Gate Leakage Reduction: **HiK**
- **Future Challenges and Options**
  - Power Limitation
  - Potential New Transistor Structures and Materials

# 40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors



**Transistor Count has Doubled Every Two Years**

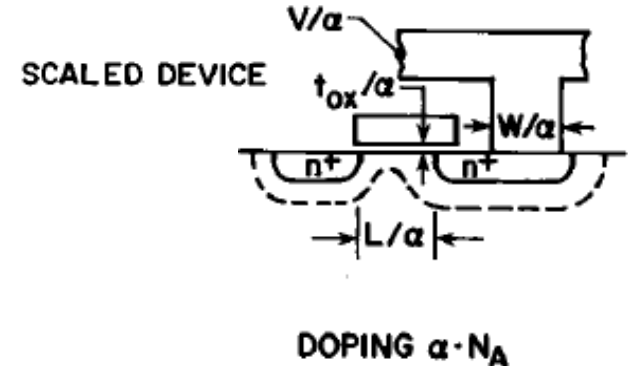
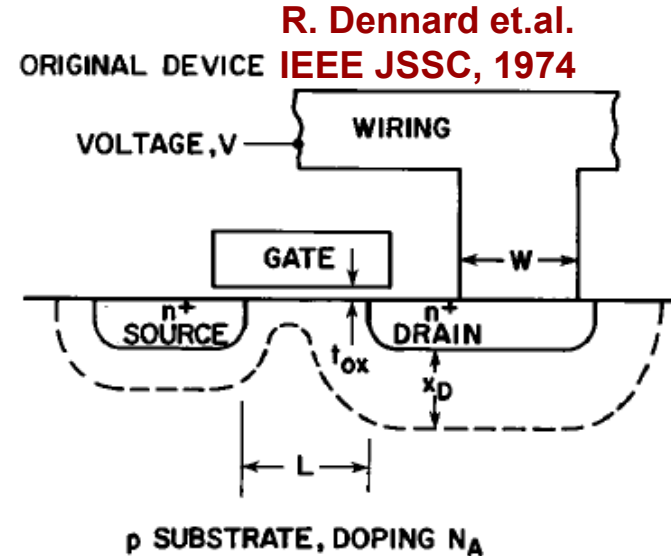
# 40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors



**END OF TRADITIONAL SCALING ERA ~ 2003**  
**Lasted ~40 YEARS**

# Top “Traditional-Scaling” Enablers

- **Gate Oxide Thickness Scaling**
  - Key enabler for Lgate scaling
- **Junction Scaling**
  - Another enabler for Lgate scaling
  - Improved abruptness ( $R_{EXT}$  reduction)
- **Vcc Scaling**
  - Reduce  $X_{DEP}$  (improve SCE)
  - However, did not follow const E field

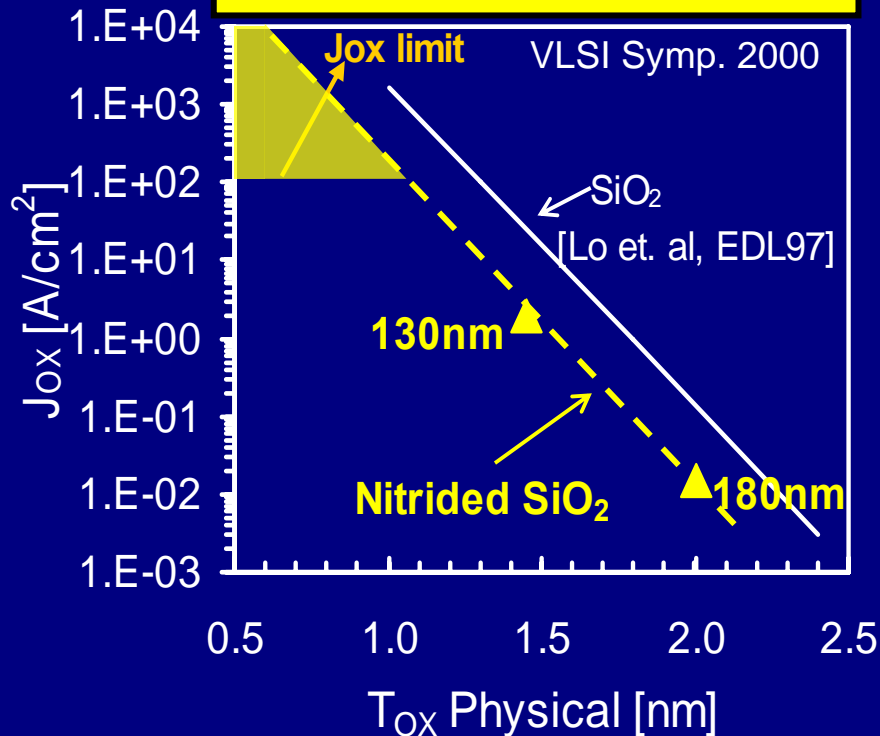


**1990's: Golden Era of Scaling**  
**Vcc,  $T_{ox}$  &  $L_g$  scaling & increasing  $I_{dsat}$**

# Year 2000: INTEL 90nm CMOS Pathfinding

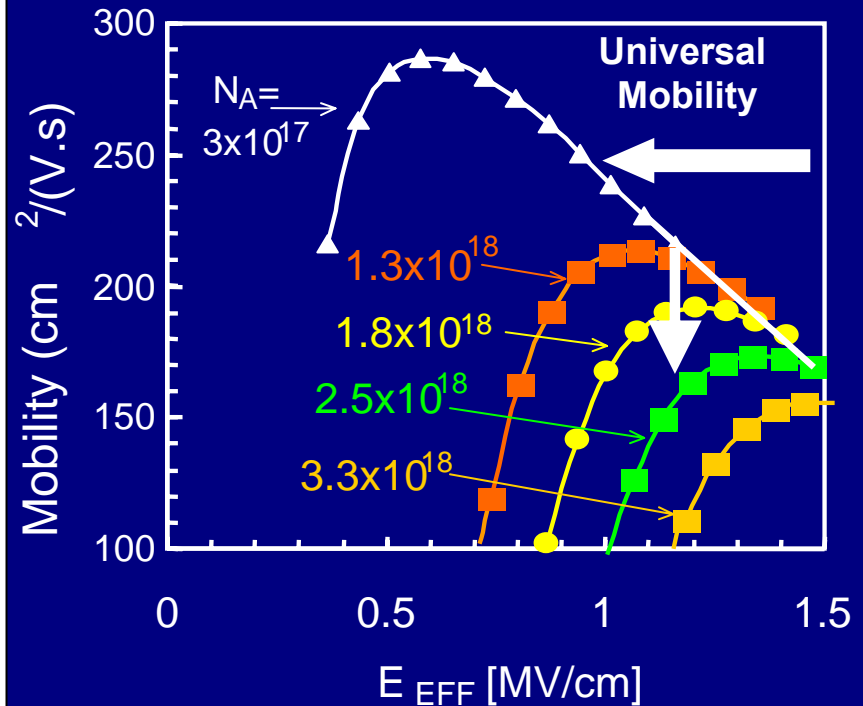
## End of “Traditional-Scaling” Era

### Gate oxide running out of atoms



- Gate Oxide Leakage direct tunneling limited

### Mobility degrades with scaling



- Universal Mobility Model
- Ionized impurity scattering

# Outline

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- **Traditional-Scaling**

- Traditional Scaling Limiters, Device Implications
- Intel's Response



- **Post “Traditional-Scaling” Innovations**

- Mobility Booster: *Uniaxial Strain*
- Poly Depletion Elimination: *Metal Gate*
- Gate Leakage Reduction: *HiK*

- **Future Challenges and Options**

- Power Limitation
- Potential New Transistor Structures and Materials

# **Innovations Pioneered by Intel to Overcome “Traditional-Scaling” Limiters**

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- Mobility enhancement through uniaxial strained silicon technology innovation introduced at 90nm node
  - **Epitaxial SiGe S/D**
  - **SiN Capping Layers**
- **HiK gate insulator** introduced at 45nm CMOS node to reduce gate leakage
- **Metal Gate** introduced at 45nm CMOS node to eliminate poly depletion

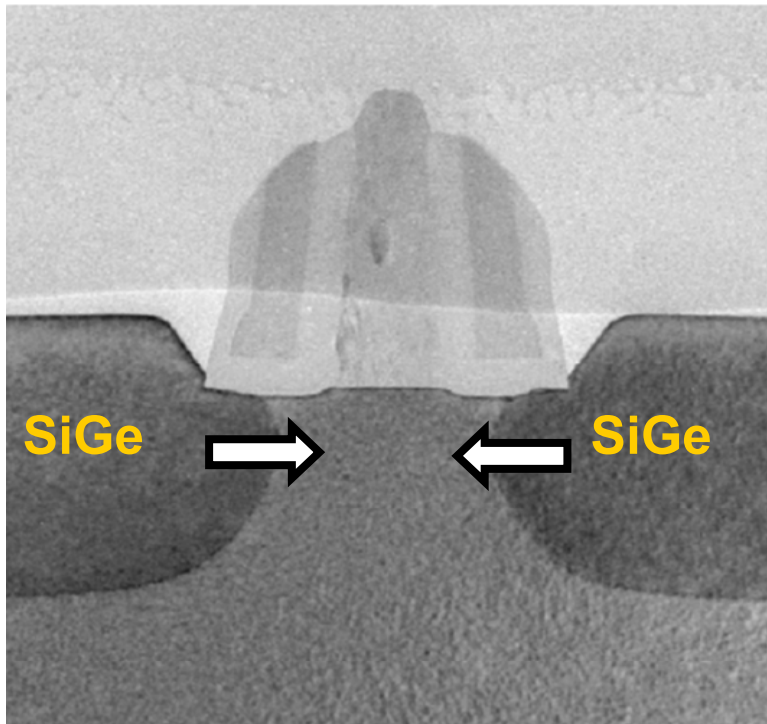


# Uniaxial Strain Silicon Transistors

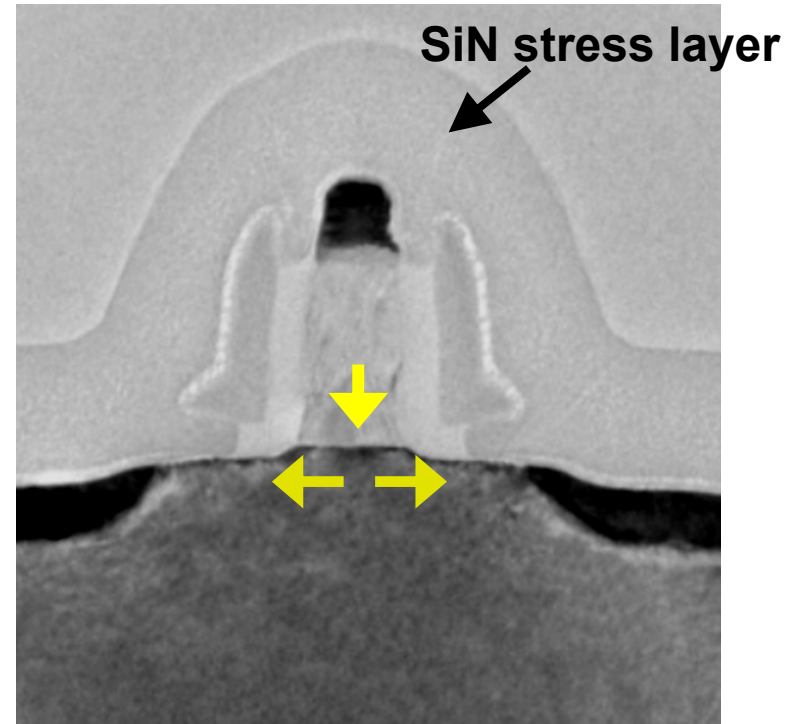
## Intel: IEDM 2003

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**PMOS** T. Ghani et. al. IEDM, 2003



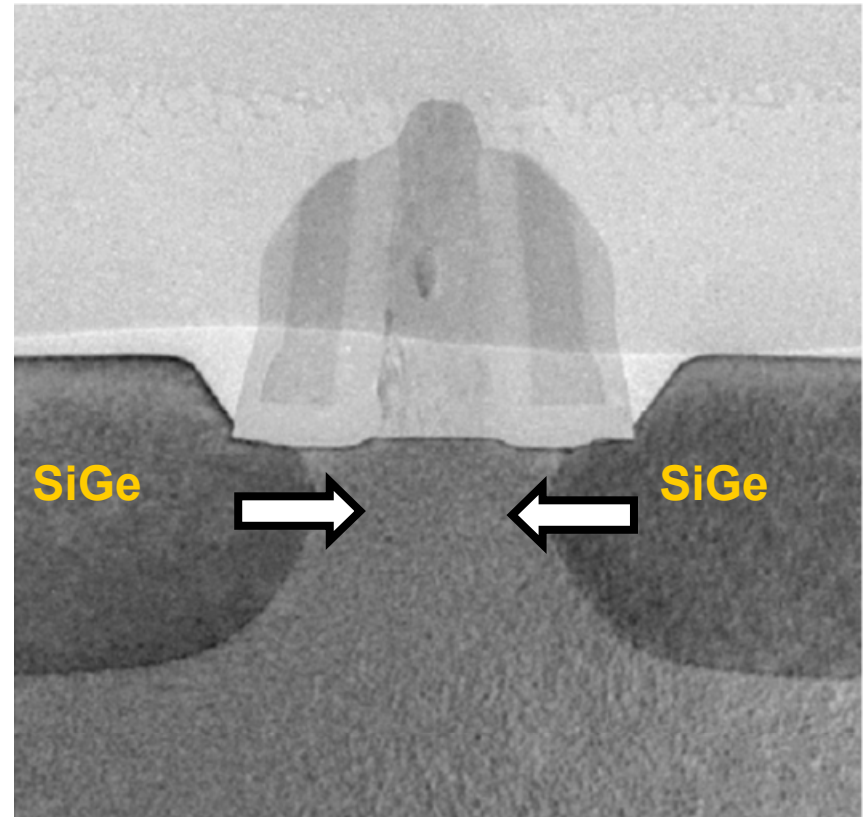
**NMOS**



**These transistor structures introduced first at Intel's 90nm CMOS node. These structures have now become industry standard for strain implementation**

# Strained SiGe S/D PMOS Transistor

- SiGe film embedded into source/drain
- SiGe film deposited by selective epitaxy
- Induces large uniaxial compressive strain in channel
- This strain leads to dramatic hole mobility enhancement

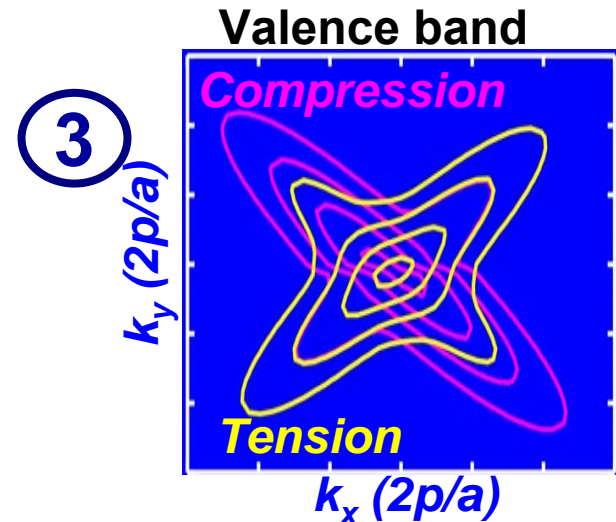
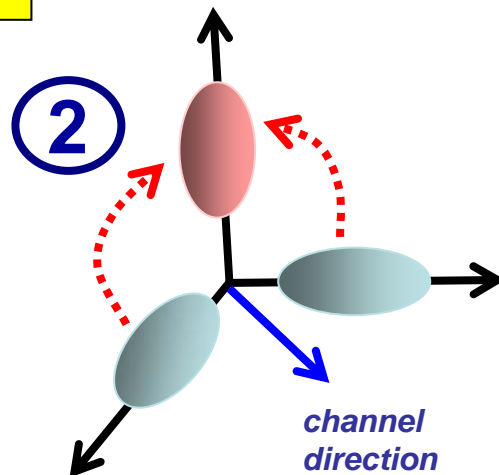
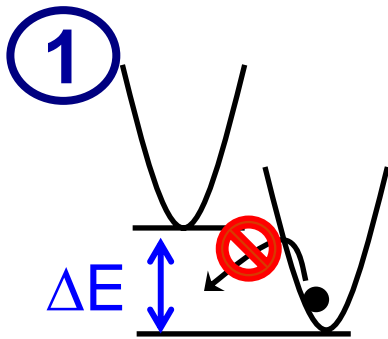


# How Strain Impacts Mobility?

Strain impacts mobility through:

- Energy/subband spacing which affects scattering ( $\tau$ ) ①
- Valley repopulation which changes transport mass ( $m_{\text{eff}}$ ) ②
- Band warpage which changes transport mass ( $m_{\text{eff}}$ ) ③

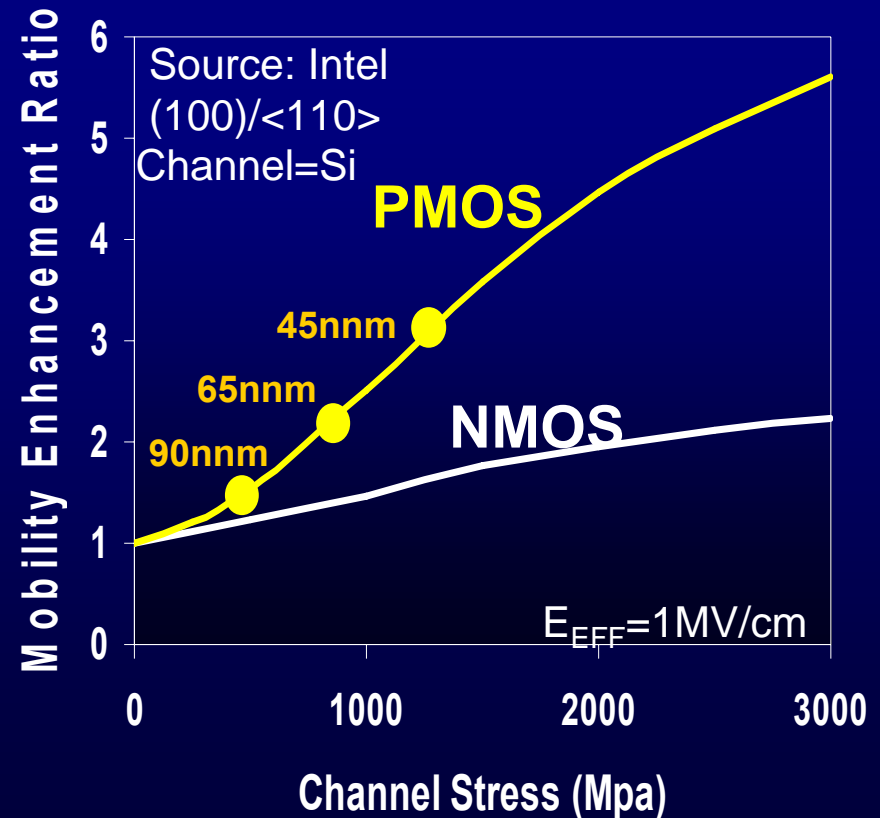
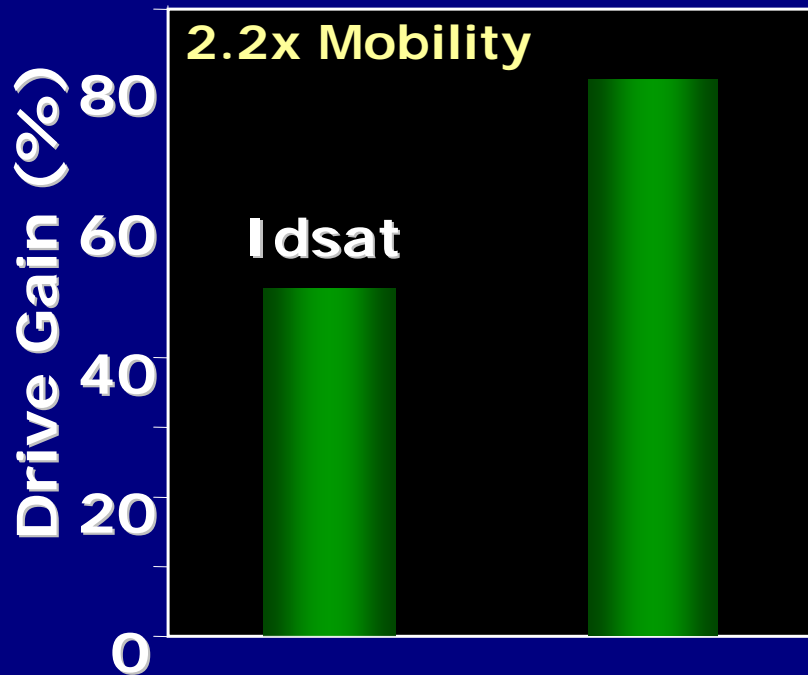
$$\mu = \frac{q \langle \tau \rangle}{m_{\text{eff}}}$$



# Performance Gains with Uniaxial Strain

## 2<sup>nd</sup> Gen PMOS: 65nm

Ref: Unstrained Silicon



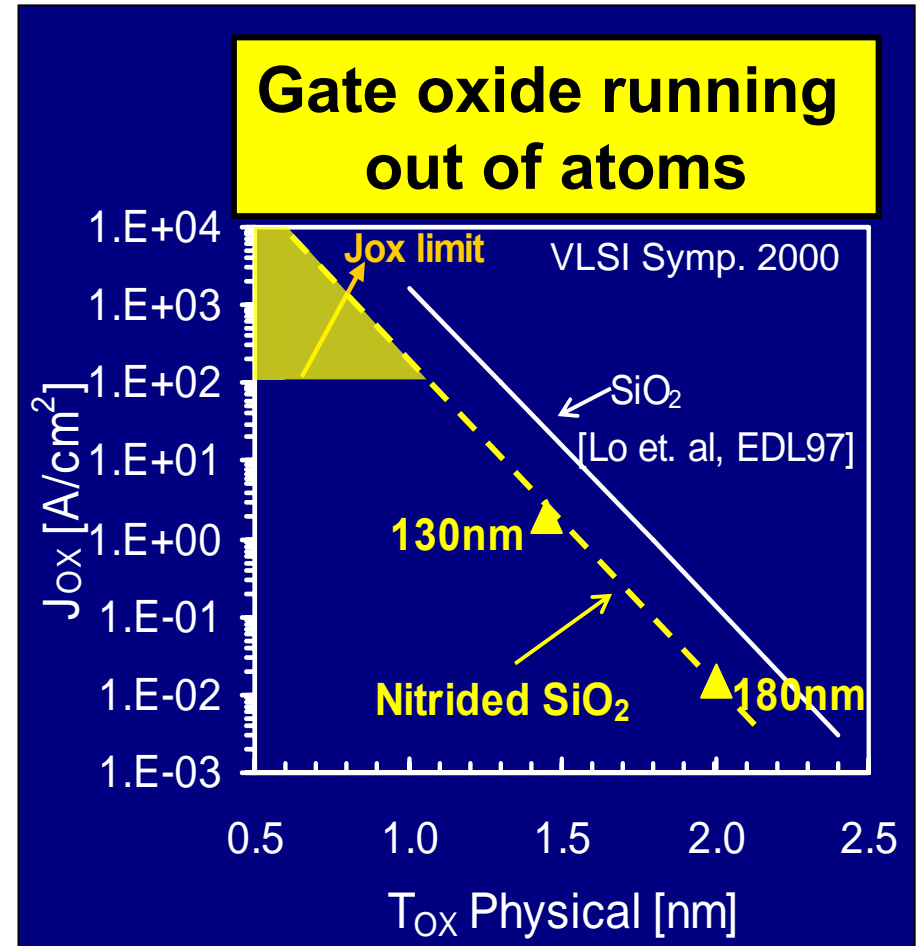
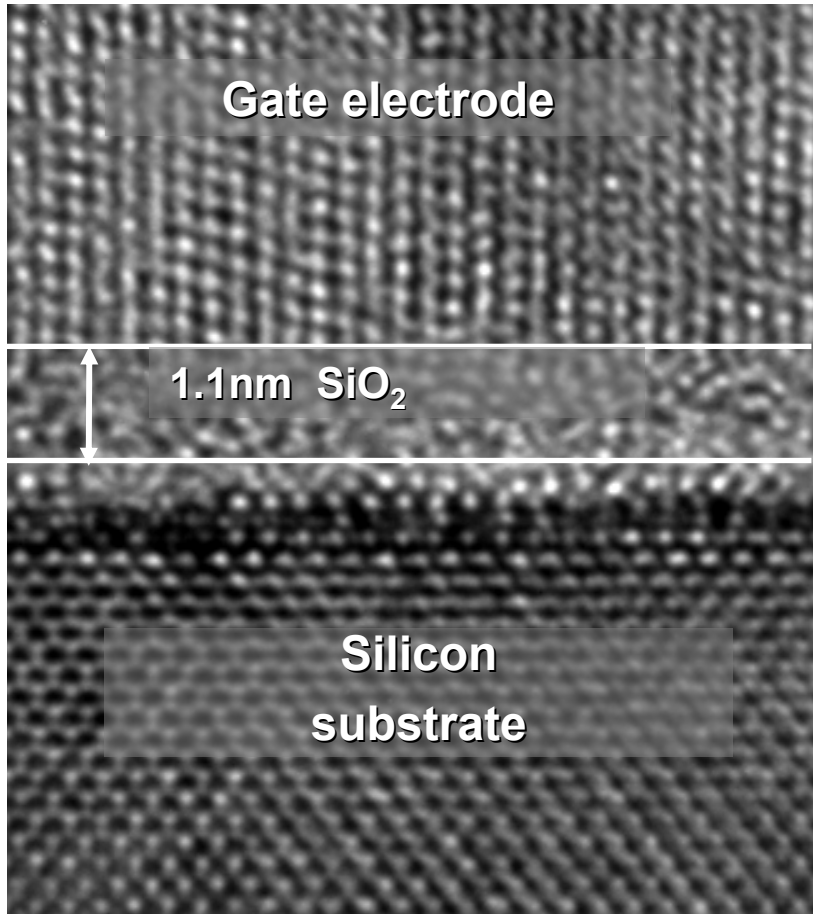
**Significant headroom left to increase PMOS mobility in future (> 5x)**

# Innovations Pioneered by Intel to Overcome Traditional Scaling Limiters

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- Mobility enhancement through uniaxial strained silicon technology innovation introduced at 90nm node
  - Epitaxial SiGe S/D
  - SiN Capping Layers
- ➔● HiK gate insulator introduced at 45nm CMOS node to reduce gate leakage
- ➔● Metal Gate introduced at 45nm CMOS node to eliminate poly depletion

# Year 2003: INTEL 65nm CMOS Pathfinding Gate Oxide Runs out of steam



## Intel 65nm production: 2005

- Gate Oxide only 3-4 atomic layers thick.
- Gate depletion also a limiter

- Gate Oxide Leakage direct tunneling limited

# High-k + Metal Gate Benefits

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- **High-k gate dielectric**
  - Reduced gate leakage
  - $T_{ox}(e)$  scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolves  $V_T$  pinning and poor mobility for high-k dielectrics

# High-k + Metal Gate Challenges

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- **High-k gate dielectric**
  - Poor mobility
  - Poor reliability
  
- **Metal gates**
  - Dual band edge work functions
  - Thermal stability
  - Integration scheme



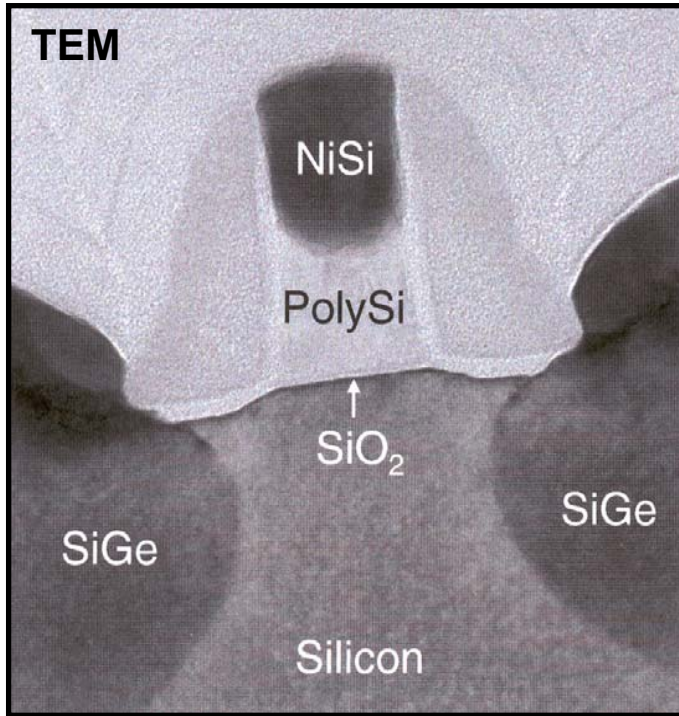
# Transistor Process Flow

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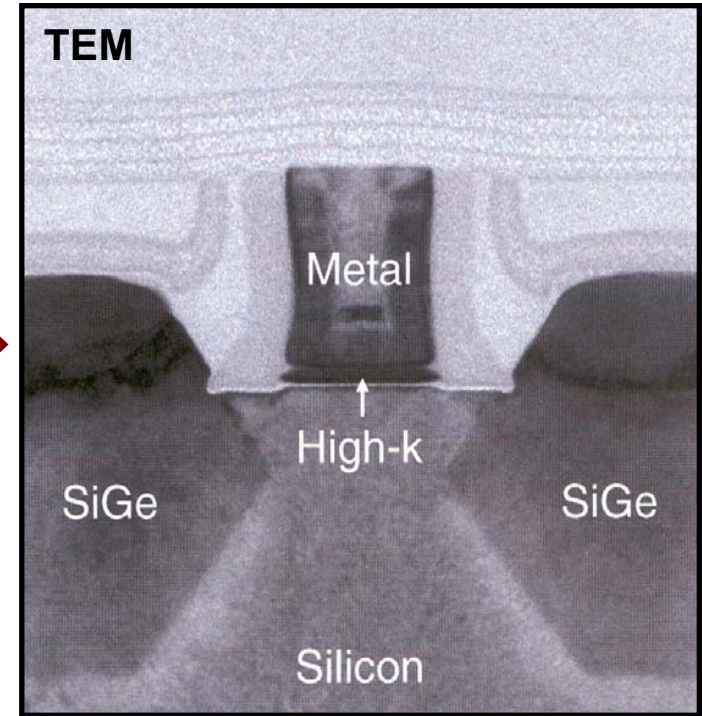
- **Key considerations**
  - Integrate hafnium-based high-k dielectric, dual metal gate electrodes, strained silicon
  - Thermal stability of metal gate electrodes
- **High-k First, Metal Gate Last**
  - Metal gate deposition after high temperature anneals
  - Integrated with strained silicon process

# 45nm High-k + Metal Gate Transistors

65 nm Transistor



45 nm HK + MG



**Hafnium-based high-k + metal gate transistors are the biggest advancement in transistor technology since the late 1960s**

# 45 nm High-k + Metal Gate Transistors

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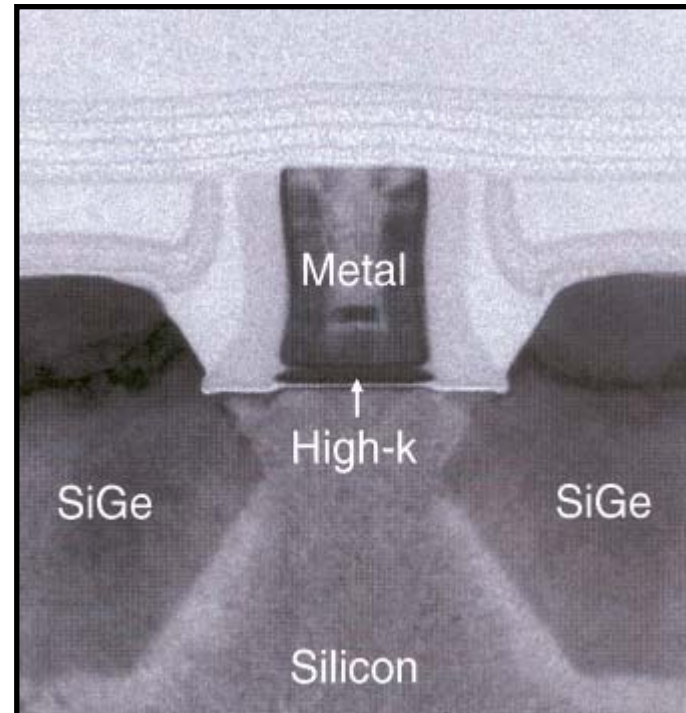
## Benefits compared to 65nm node

>25x lower gate oxide leakage

>30% lower switching power

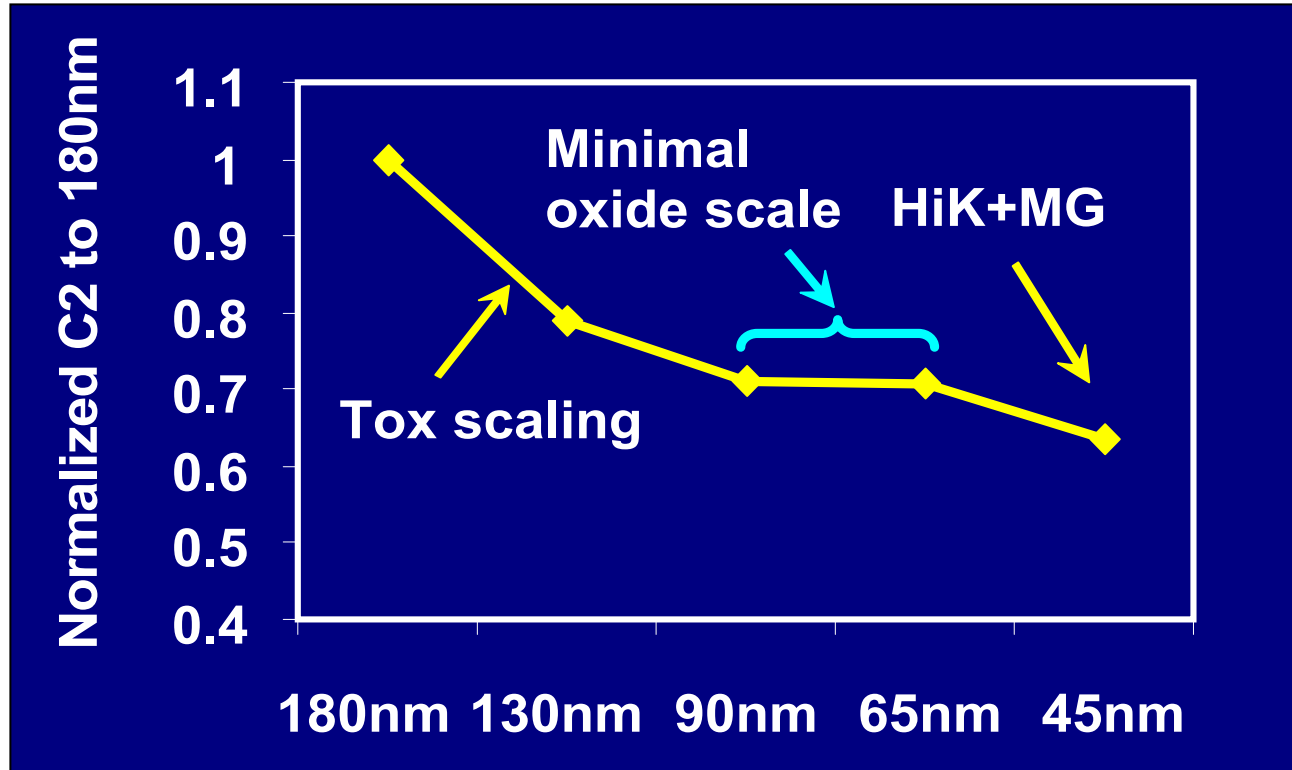
~30% higher drive current, or

>5x lower source-drain leakage



*Intel is only company with high-k + metal gate transistors  
in production, starting in Nov. '07*

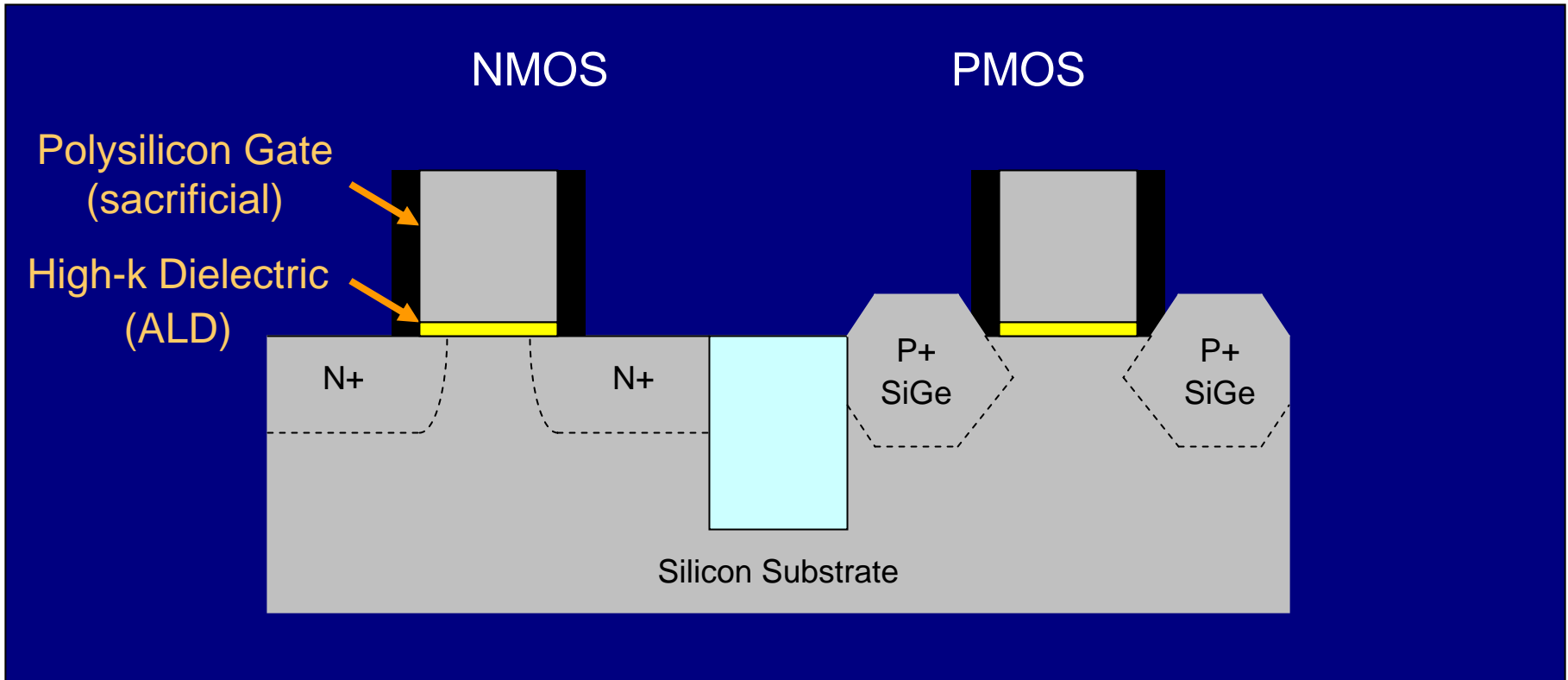
# Scaling of Vt Variation



$$\sigma V_{Tran} = \left( \frac{\sqrt[4]{4q^3 \epsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\epsilon_{ox}} \cdot \left( \frac{\sqrt[4]{N}}{\sqrt{L_{eff} \cdot Z_{eff}}} \right) = \frac{1}{\sqrt{2}} \left( \frac{c_2}{\sqrt{L_{eff} \cdot Z_{eff}}} \right) \quad (1)$$

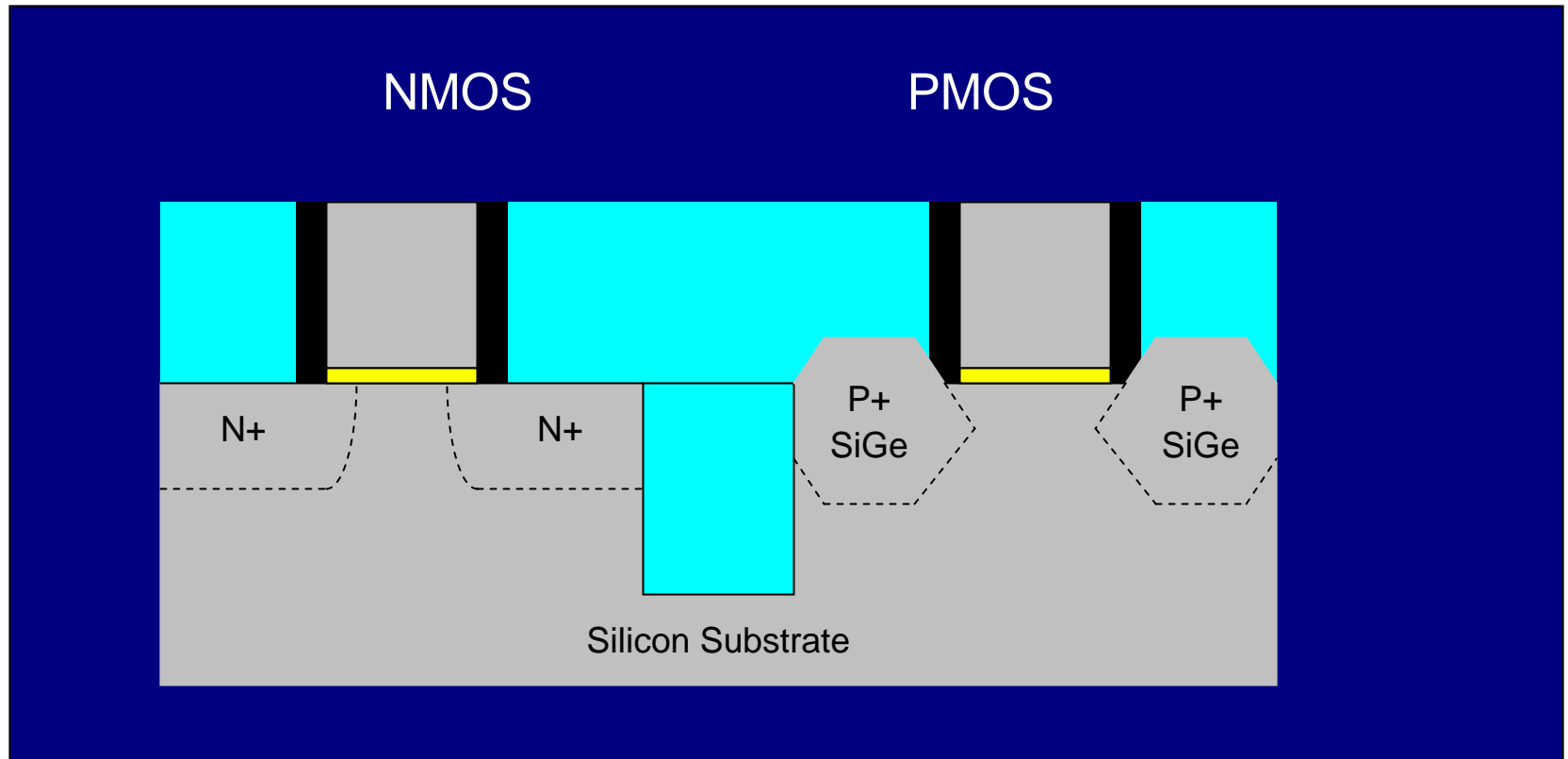
**HK+MG reduces random Vt variation**  
**Critical to SRAM Vmin**

# Replacement Metal Gate Flow



**Standard transistor process through source-drain formation,  
but including atomic layer deposition high-k dielectric**

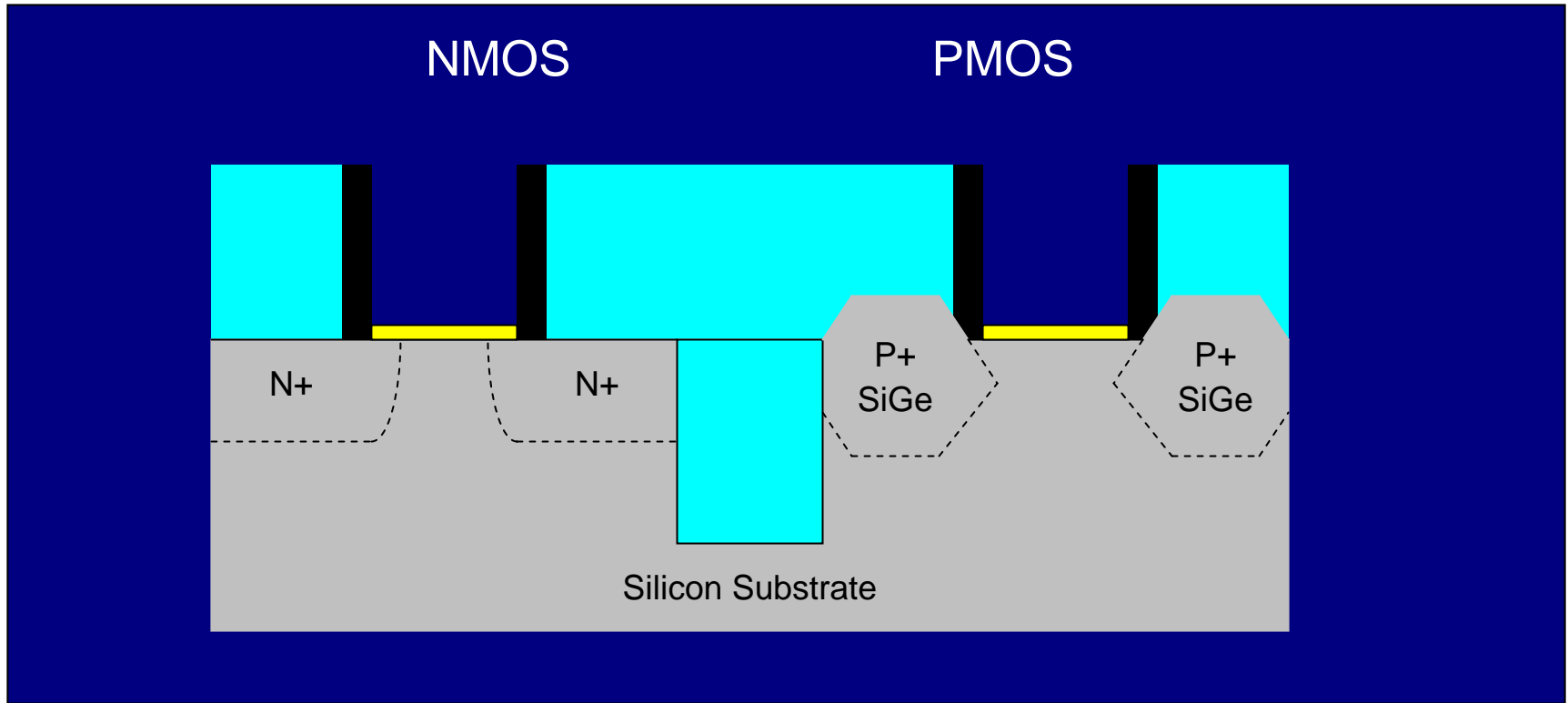
# Replacement Metal Gate Flow



**Deposit and planarize oxide layer**

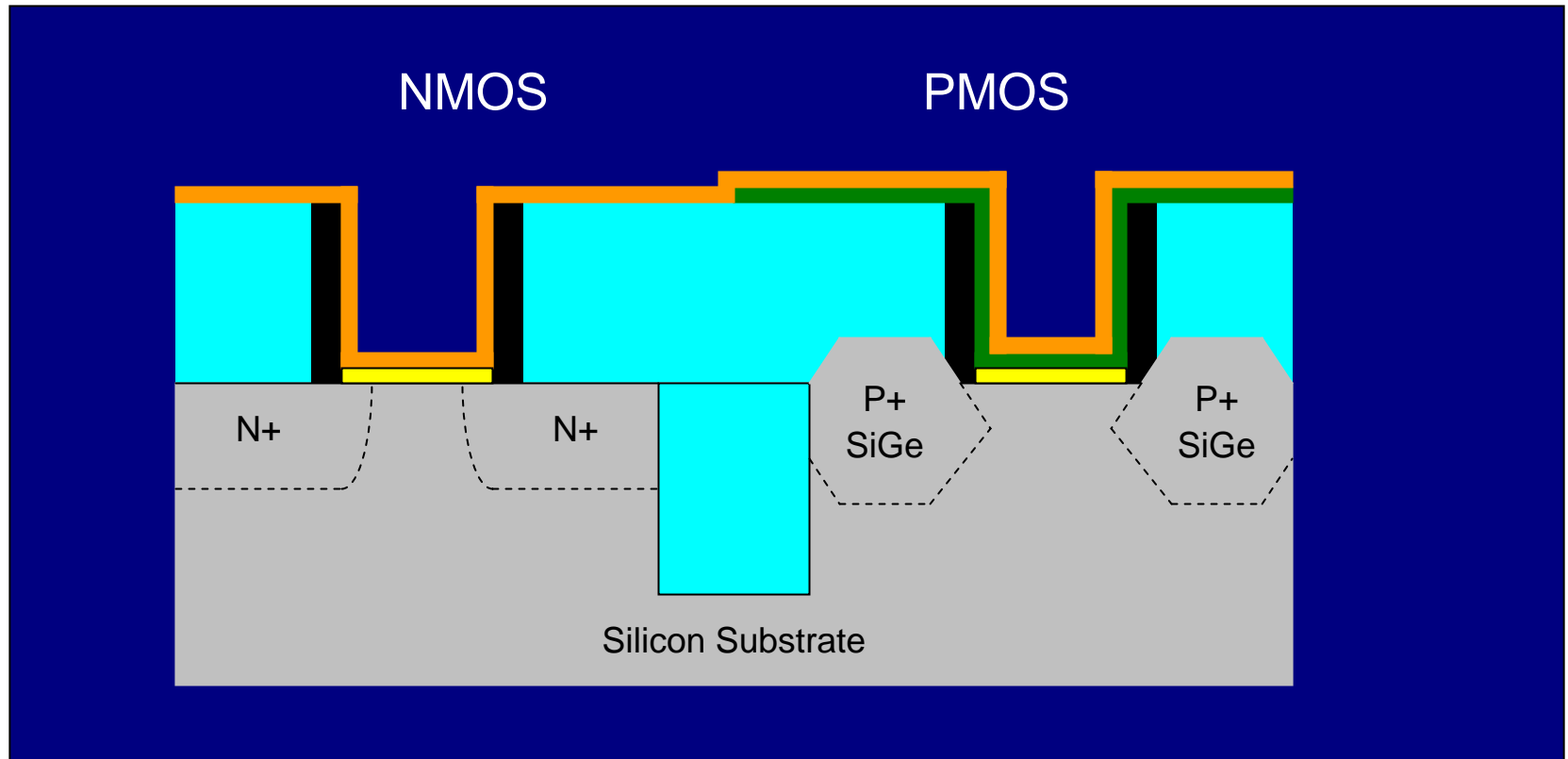
# Replacement Metal Gate Flow

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**Etch out sacrificial polysilicon gate**

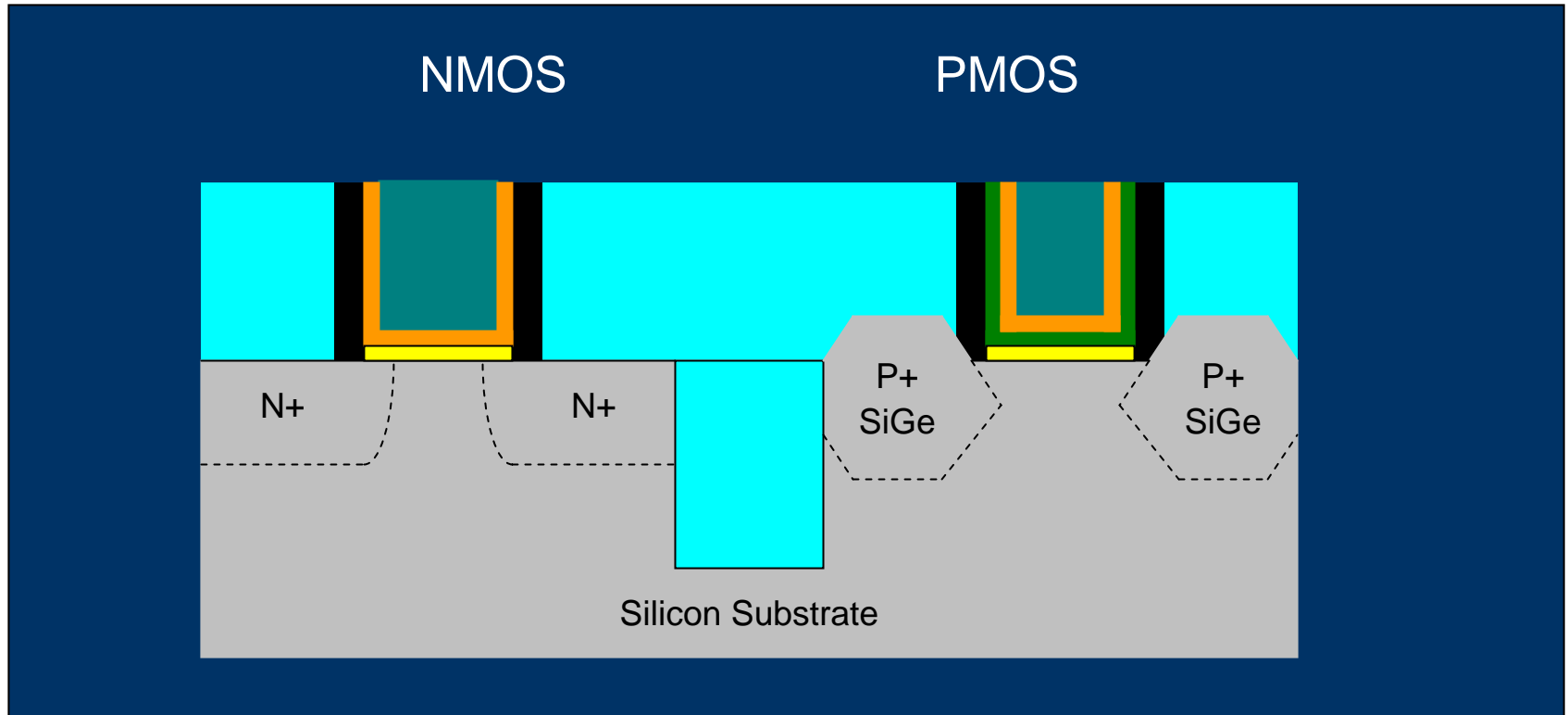
# Replacement Metal Gate Flow



**Deposit separate NMOS and PMOS WF metal layers**



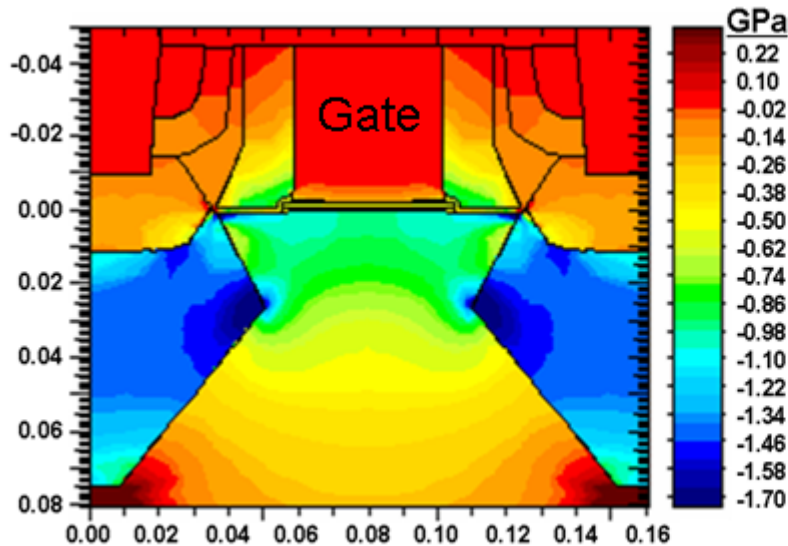
# Replacement Metal Gate Flow



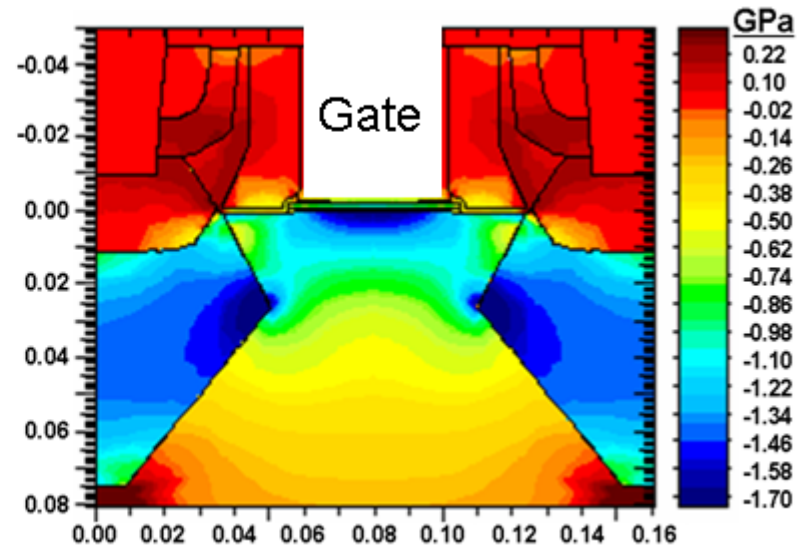
**Deposit Al fill metal, planarize surface**

# RMG PMOS Strain Benefit

Before gate removal



After gate removal

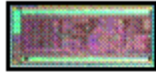


**RMG process provides significant additional PMOS performance gain by increasing channel strain**

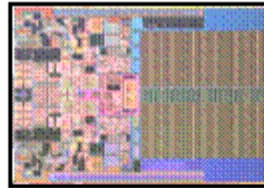
# 45 nm Microprocessor Products

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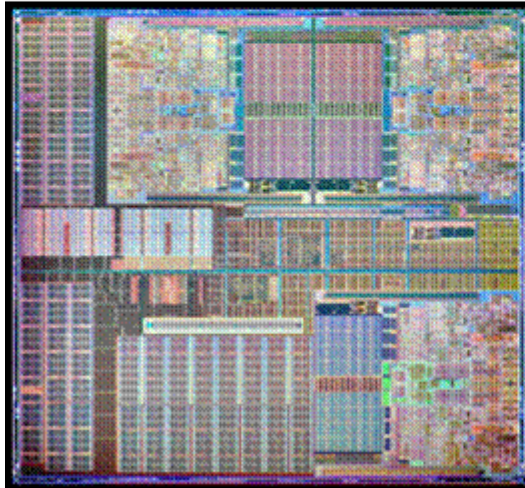
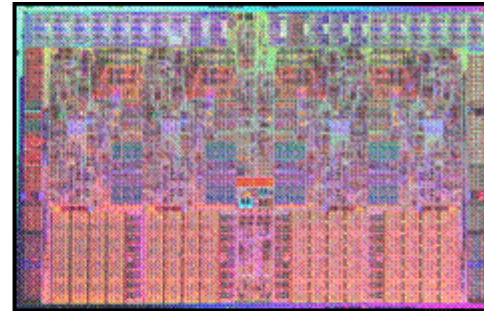
Single Core



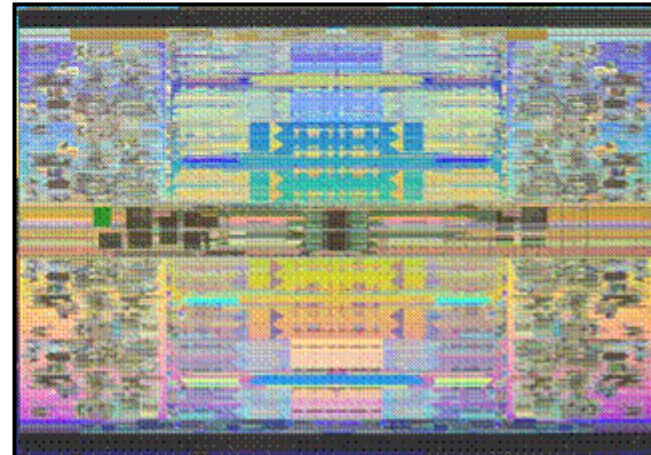
Dual Core



Quad Core



6 Core

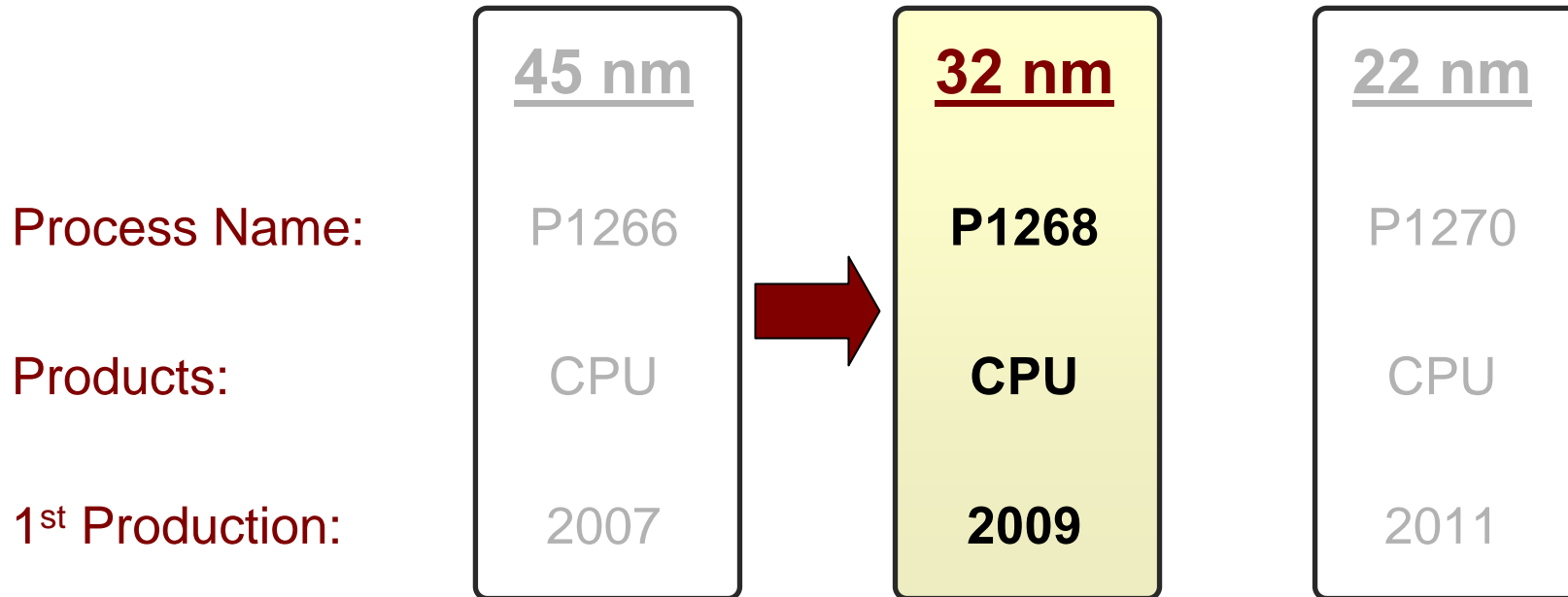


8 Core

*>200 million 45 nm CPUs shipped to date*

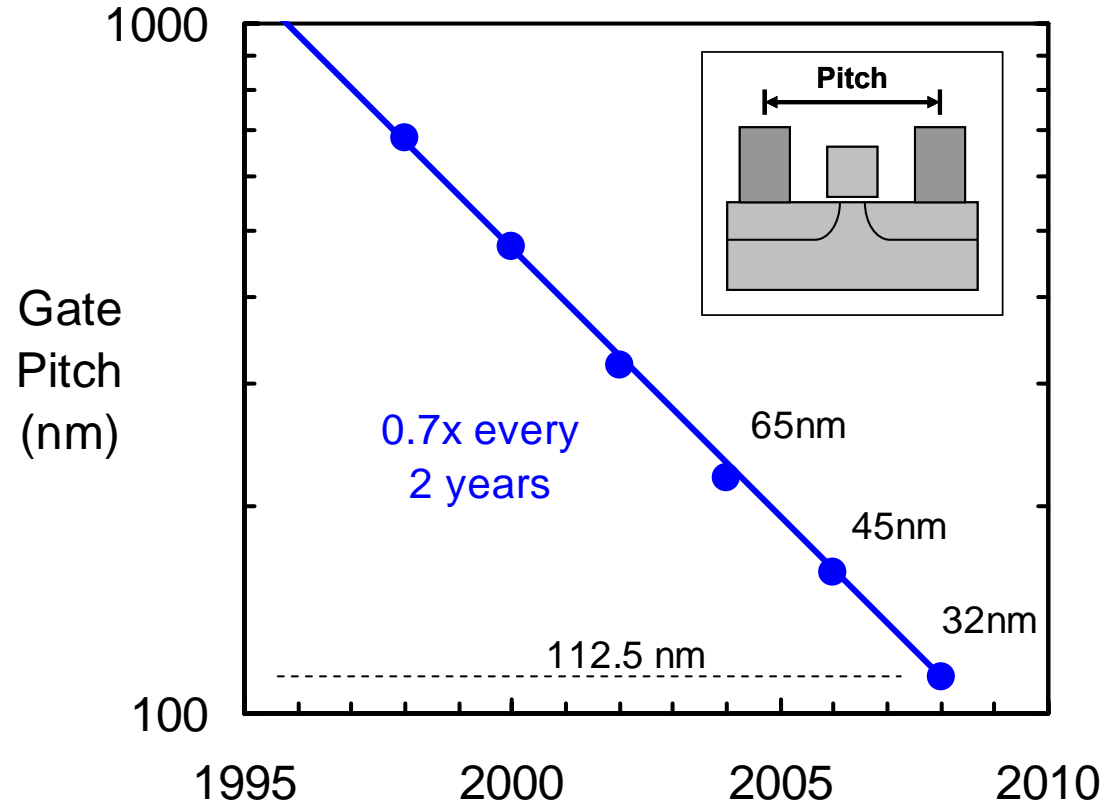
# Intel Logic Technology Roadmap

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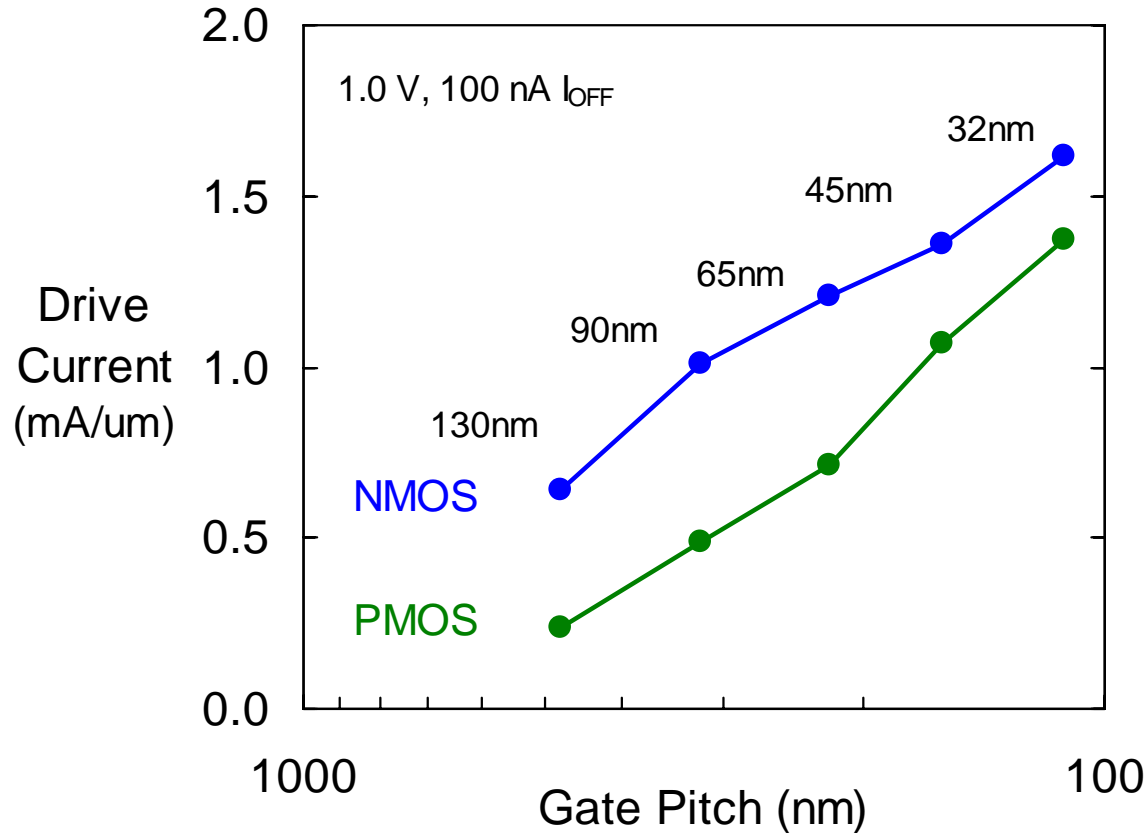
**Intel 32nm: 2nd generation high-k + metal gate transistors**

# Transistor Density



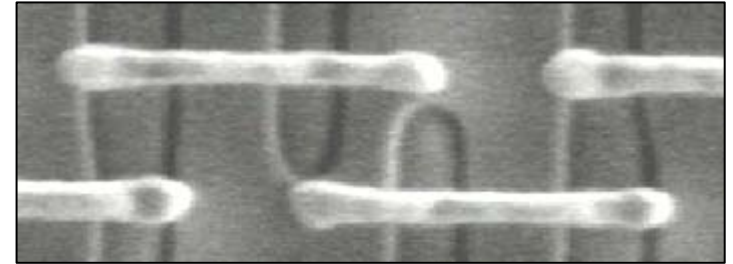
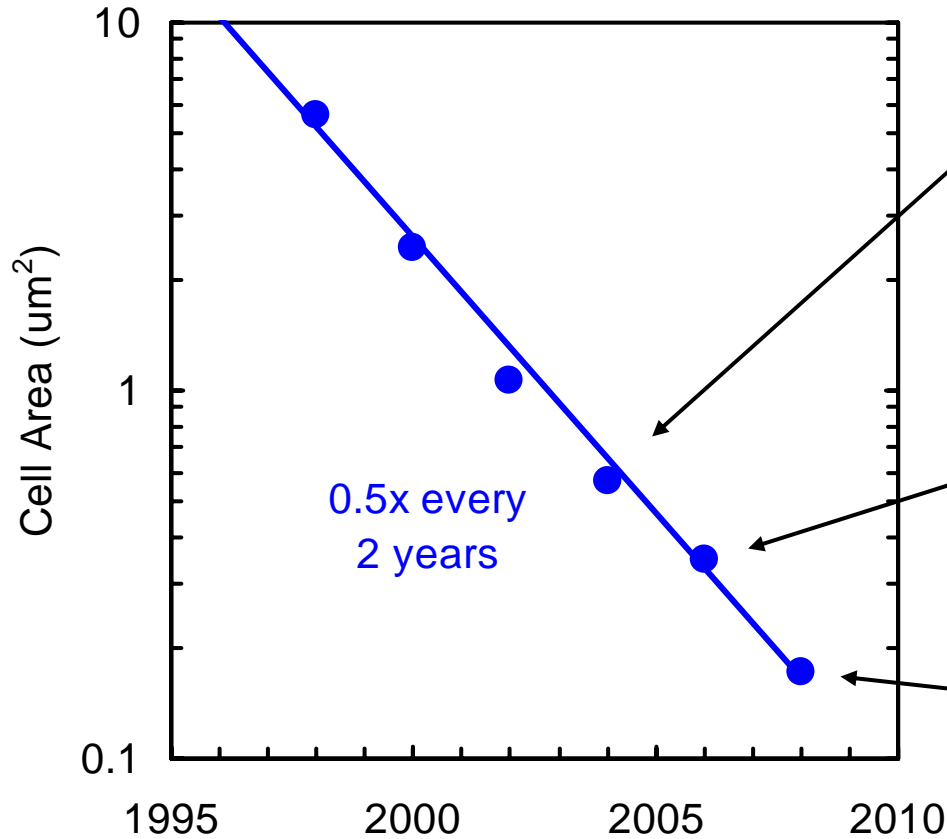
*Intel 32 nm transistors provide the tightest gate pitch of any reported 32 nm or 28 nm technology*

# Transistor Performance

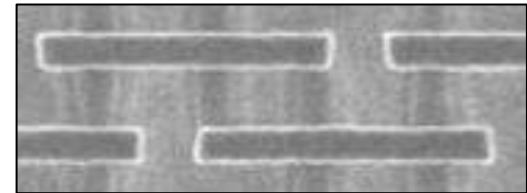


*Intel 32 nm transistors provide the highest drive currents of any reported 32 nm or 28 nm technology*

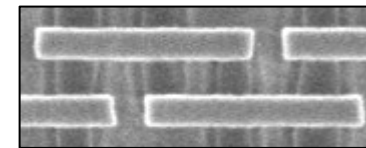
# SRAM Cell Size Scaling



65 nm,  $0.570 \mu\text{m}^2$



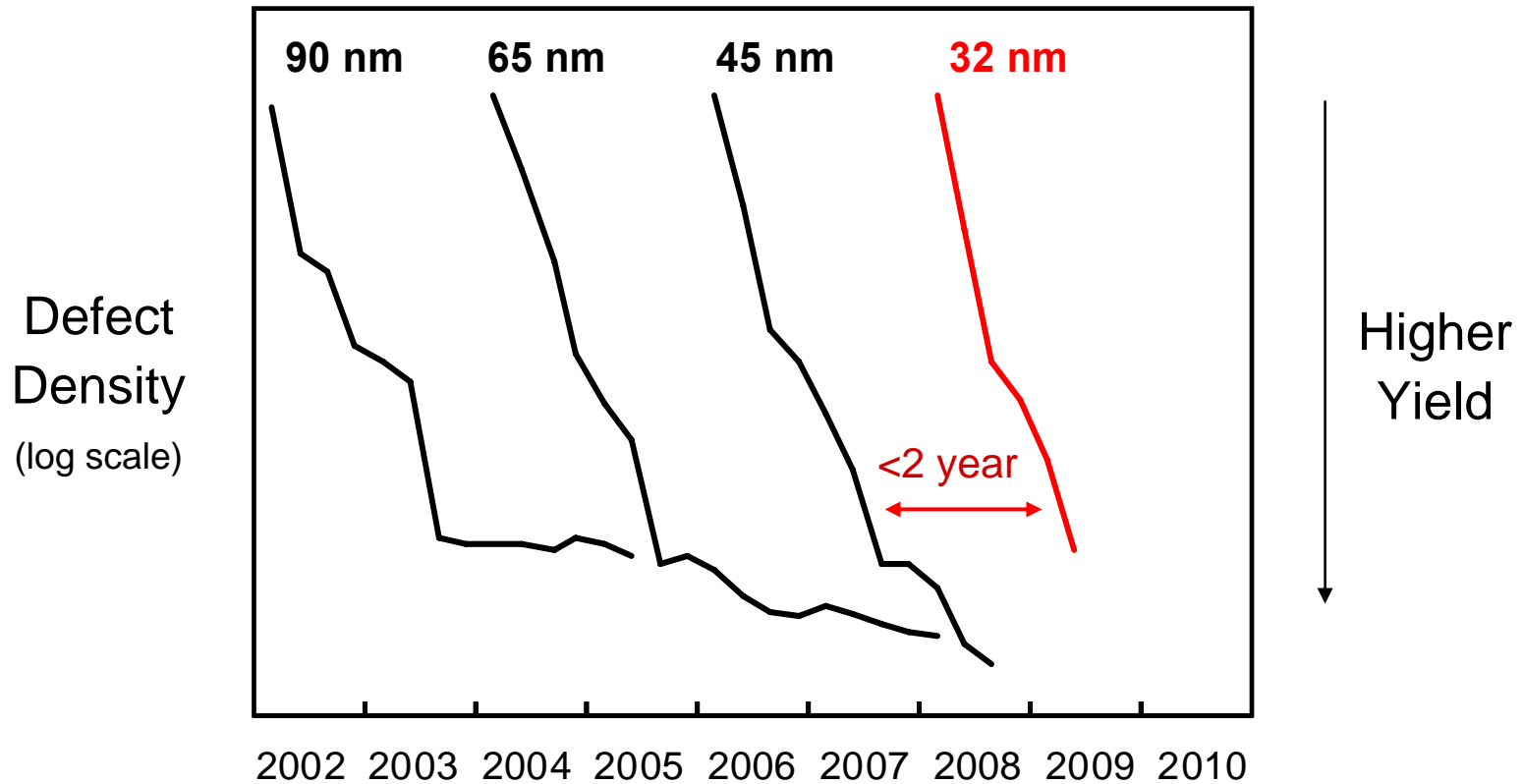
45 nm,  $0.346 \mu\text{m}^2$



32 nm,  $0.171 \mu\text{m}^2$

*Transistor density continues to double every 2 years*

# 32 nm Defect Density Trend



*Intel's 32 nm process is certified and CPU wafers are moving through the factory in support of planned Q4 revenue production*



# Outline

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- Traditional Scaling Limiters, Device Implications
- Intel's Response

- **Post “Traditional-Scaling” Innovations**

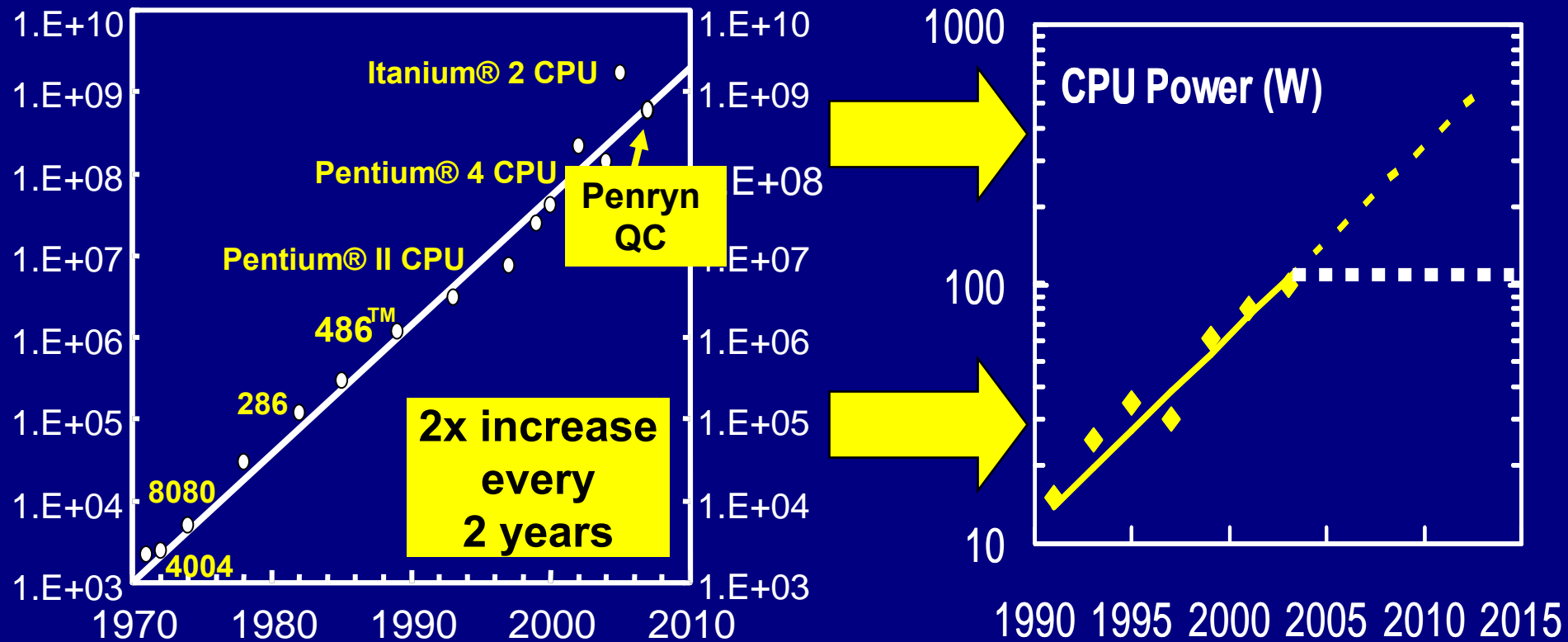
- Mobility Booster: *Uniaxial Strain*
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- **Future Challenges and Options**

- Power Limitation
- Potential New Transistor Structures and Materials

# CPU Transistor Count & Power Trend



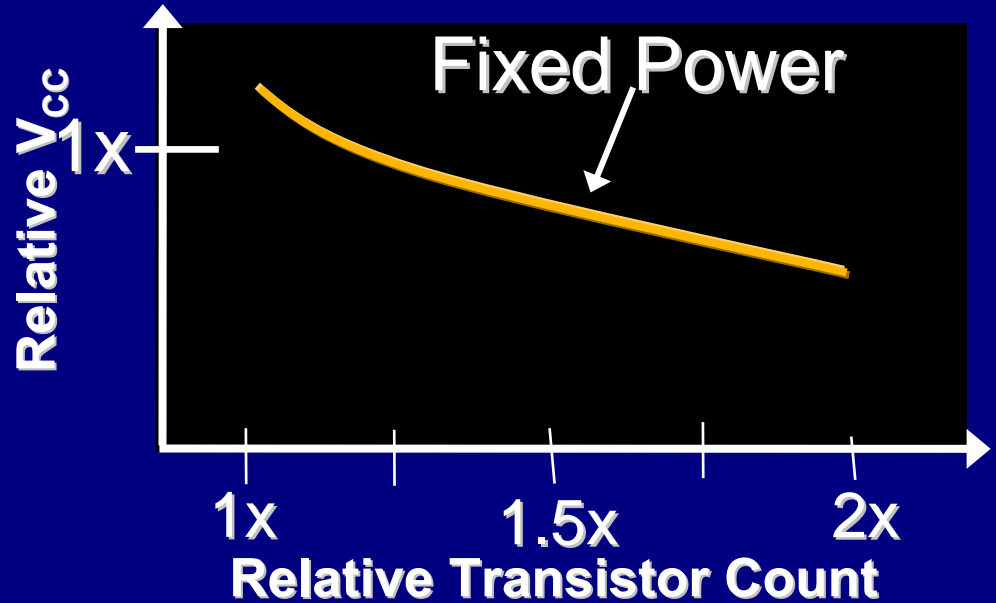
**Power Dissipation Limited to ~100W  
BUT increased transistor count needed  
in Multi-Core CPU Era !!!**

# Multi-Core CPU Power Limited Era

$P = \text{Switching Power} + \text{Leakage Power} + \dots$

$\sim (fC_{\text{gate}} V_{\text{CC}}^2 \alpha) * N$

**Constant**



- $V_{\text{CC}}$  scaling required for continued increase in transistor count in power limited world

**Future Transistors will need to continue to achieve Higher Performance while Scaling Power Supply Voltage**

# Possible Future Transistor Options

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- **Advanced Channel Materials**
  - **III-V and Ge channel materials**
- **Multi-Gate Fin Transistors**
  - **Non planar architecture**
- **Tunnel Transistors**
  - **New transport mechanism**

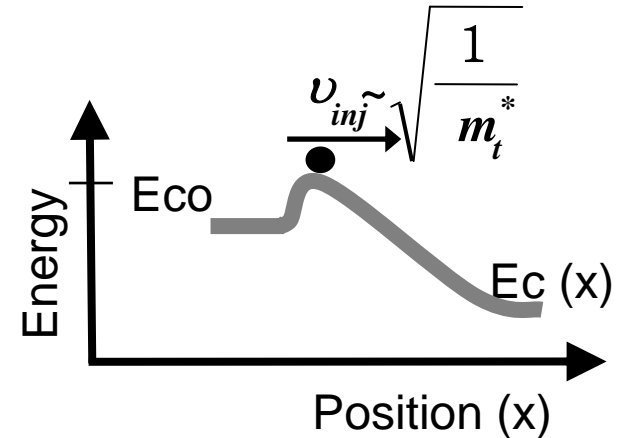
**Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET**

# Ultimate Channel Materials: Ballistic Transport

## Ultimate Ballistic Regime:

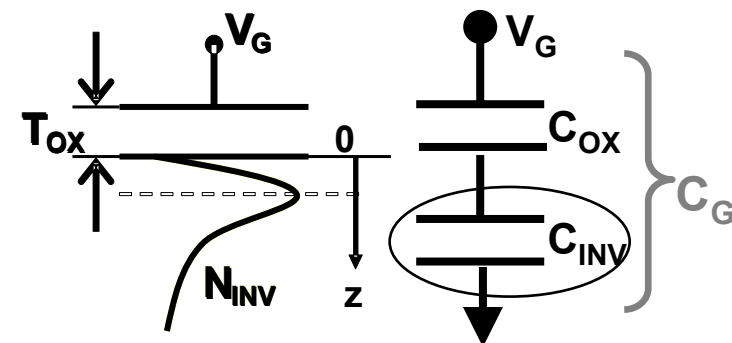
$$I_{\text{DSAT}} \sim Q_{\text{inv}} * v_{\text{inj}}$$

1. Need low  $m_t^*$  in channel direction to achieve high  $v_{\text{inj}}$  and maximize  $I_{\text{DSAT}}$



Quantum Capacitance very important at thin  $T_{\text{ox}}$

2. Need high  $m_{\text{DOS}}^*$  to achieve high  $C_{\text{GATE}}$  and  $Q_{\text{inv}}$  to maximize  $I_{\text{DSAT}}$



$$C_{\text{INV}}^{\text{2-D}} \sim \frac{q^2 m_{\text{DOS}}^*}{\pi h^2}$$

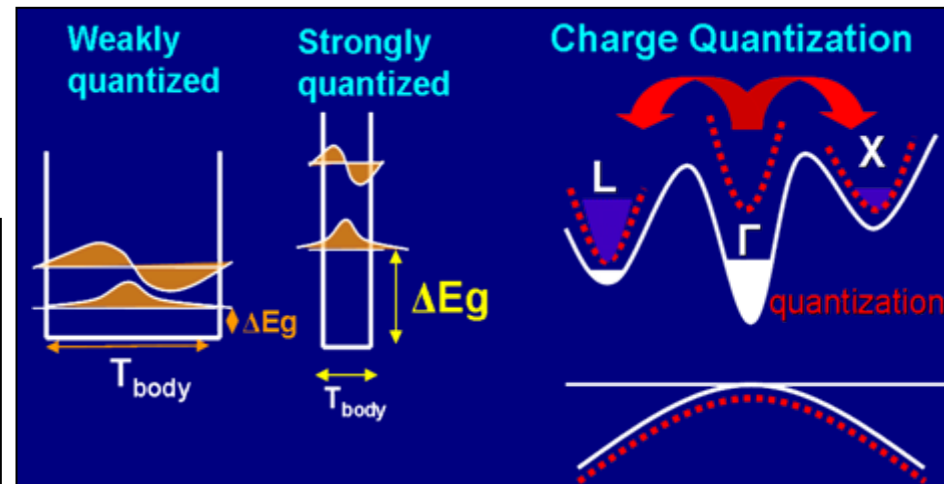
# III-V Materials for NMOS Channel?

- + Low  $m^*$   $\Gamma$  valley  $\Rightarrow$  High  $v_{inj}$
- Low  $m^*$   $\Gamma$  valley  $\Rightarrow$  Low  $m_{DOS}^*$   
 $\Rightarrow$  Low  $Q_{INV}$
- 2-D Quantization:  
 $\Rightarrow$  Charge transfer from low mass  $\Gamma$  to high mass X & L valleys  
 $\Rightarrow$  Lowers  $v_{inj}$
- Low  $E_g \Rightarrow$  Large  $I_{off}$  (junction)
- High  $\epsilon \Rightarrow$  Poor SCE

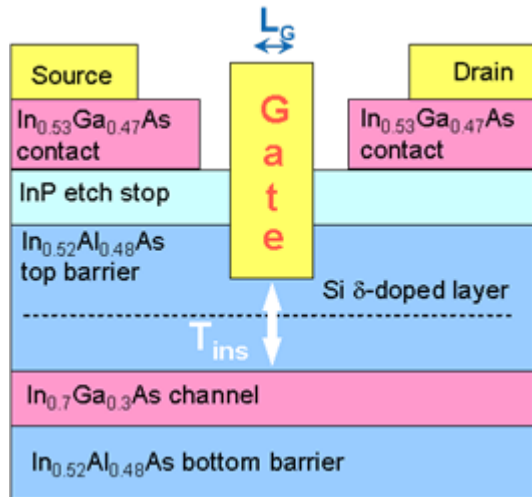
Properties of some NMOS candidates

Material/Property	Si	Ge	GaAs	InAs	InSb
$m_{eff}^*$	0.19	0.08	0.067	0.023	0.014
$\mu_n$ (cm <sup>2</sup> /Vs)	1600	3900	9200	40,000	77,000
$E_g$ (eV)	1.12	0.66	1.42	0.36	0.17
$\epsilon_r$	11.8	16	12.4	14.8	17.7

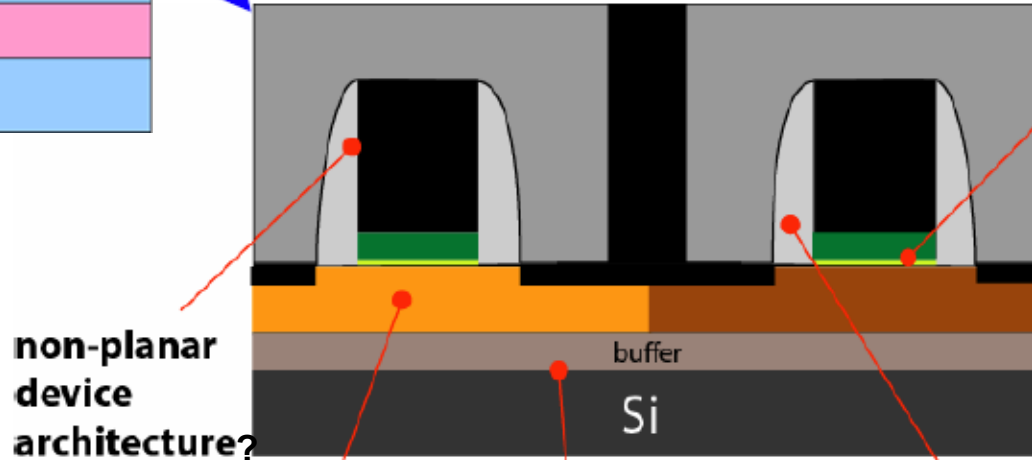
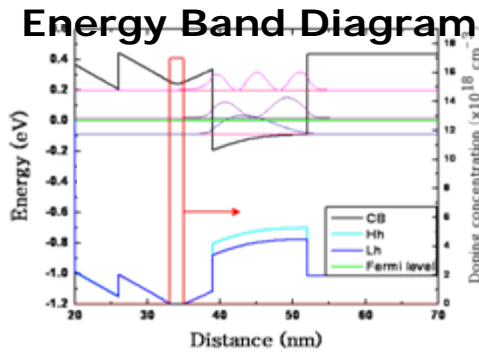
Projecting III-V NMOS performance based on simplistic models could lead to erroneous performance assessment.



# The Grand Challenges for III-V CMOS



- InGaAs Quantum Well channel
- InAlAs insulator (poor Jox)
- Ti/Pt/Au gate
- Non-self aligned contacts



high-K dielectric gate insulator

J. Del Alamo  
IEDM 2007

non-planar device architecture?

III-V p-type channel device

Scalable, self-aligned, E-mode device architectures

III-V epitaxy on large-area Si wafers

# Ge Transistor- Back to the Future?

## • Advantages:

- + Best hole mobility (unlike III-V)
- + Si(Ge) already used in logic tech
- + Col-IV: Non-Polar

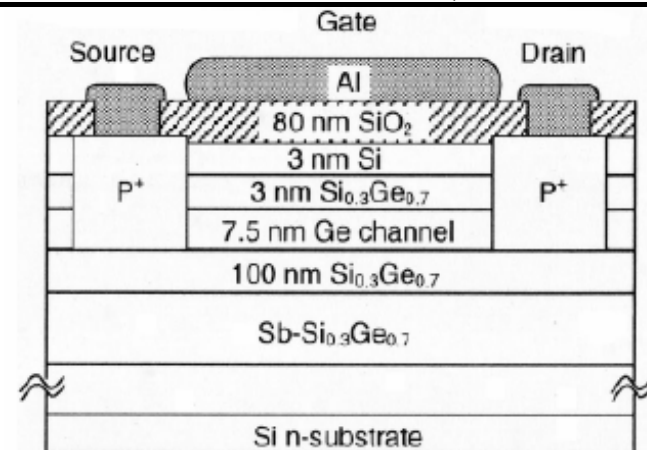
## • Challenges:

- Reference device is highly strained silicon
- Poor HiK interface:
  - \* Need better understanding
  - \* Buried strained QW Ge
- Higher dielectric constant
  - \* Poorer SCE
- Worse parasitic resistance
  - \* Worse dopant activation

Material ⇒ Property ↓	Si	Ge	GaAs	InAs	InSb
Electron mobility	1600	3900	9200	40000	77000
Hole mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

K. Saraswat et.al., IEDM 2006.

## Buried Strained Ge Quantum Well




(U. Tokyo, APL 2002)



# Possible Future Transistor Options

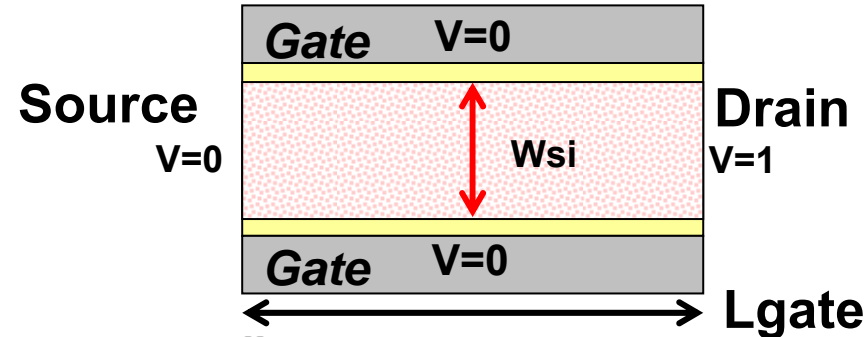
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- Advanced Channel Materials
  - III-V and Ge channel materials
-  • Multi-Gate Fin Transistors
  - Non planar architecture
- Tunnel Transistors
  - New transport mechanism

**Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET**

# Multi-Gate Transistor Architecture

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}}$$

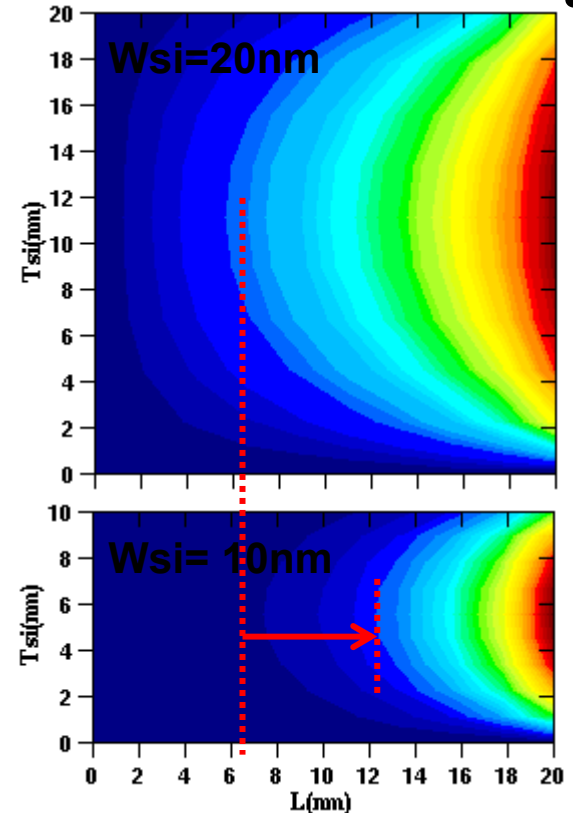


## Multi-Gate Transistors have better SCE:

- Gates reduce spread of  $V_{drain}$   
Enables lower threshold voltage ( $\uparrow I_D$ )
- Enable lower channel doping ( $\uparrow \mu$ )

## Multi-Gate Transistors have lower $E_{EFF}$ :

- Optimum gate work function is away from band-edge leading to lower  $E_{eff}$  ( $\uparrow \mu$ )

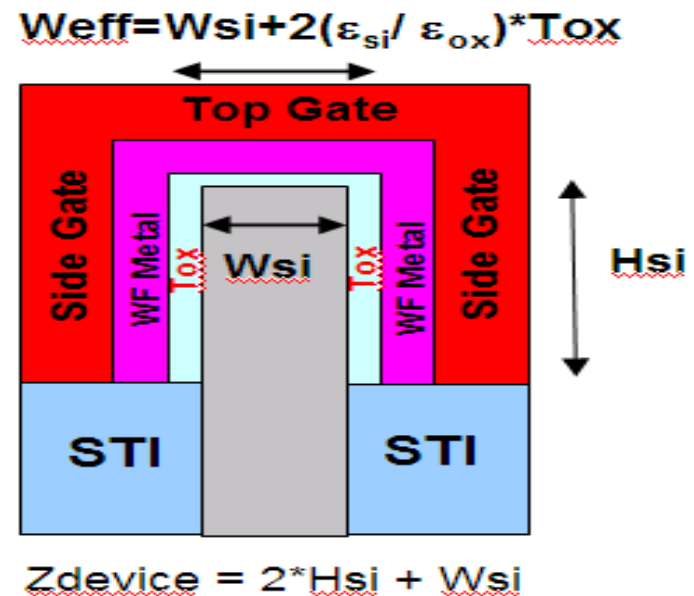
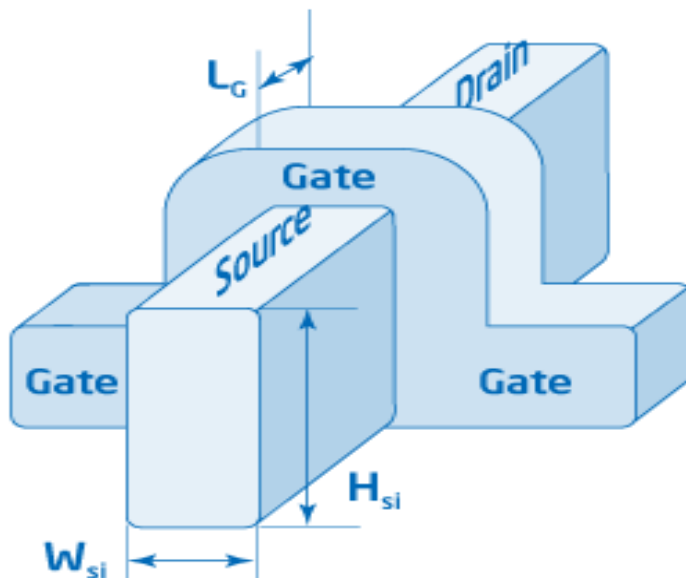


# Multi-Gate Transistors Implementation

## Multi-Gate Fin Transistor:

++ Self Aligned structure for S/D

-- Non-Planar structure



## Multi-Gate Fin Transistor

# Top Challenges for Multi-Gate Fin Transistors

## ➤ Implement High Strain in Fins?

Planar Ref= Highly strained  
4-5x p-mobility enhancement

High level of fin strain NOT  
published to date

## ➤ High Parasitics in Fin Transistors

Narrow fins lead to high  $R_{ext}$

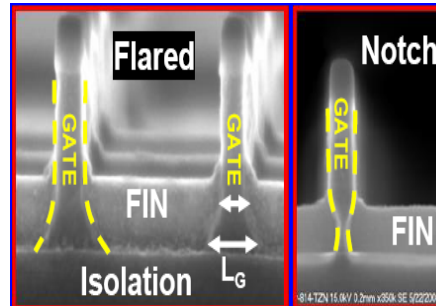
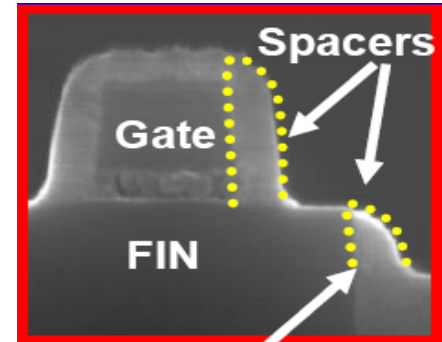
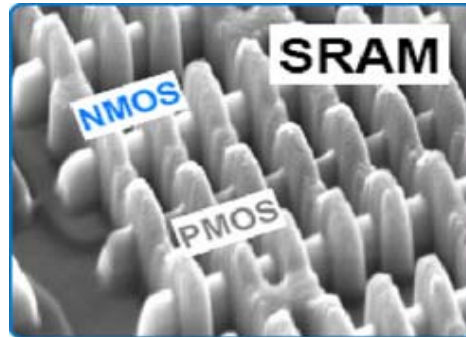
Fin architecture may also lead to  
higher fringe capacitance

## ➤ Manufacturing worthy Patterning

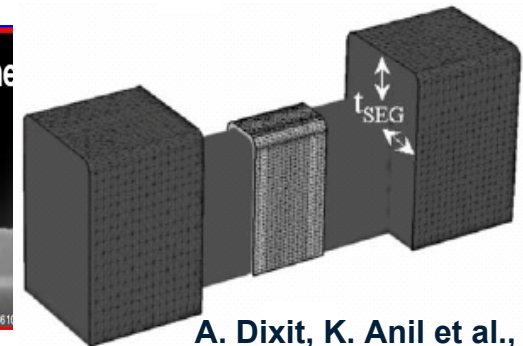
Fin, Gate and Spacer patterning  
will be extremely challenging in  
a manufacturing environment

## ➤ Design

Device Z increments quantized



J. Kavalieros et. al.  
VLSI Symp 2006




A. Dixit, K. Anil et al.,  
Solid State  
Electronics, 2006

- Best published drive currents for Multi-Gate Fin Transistors are significantly lower than best published planar transistors to date
- Many significant challenges remain to be resolved for Fin Transistors

# Possible Future Transistor Options

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- Advanced Channel Materials
  - **III-V and Ge channel materials**
- Multi-Gate Fin Transistors
  - **Non planar architecture**
-  • Tunnel Transistors
  - **New transport mechanism**

**Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET**

# Why we Need to Beat Sub-Threshold Slope of 60mV/decade?

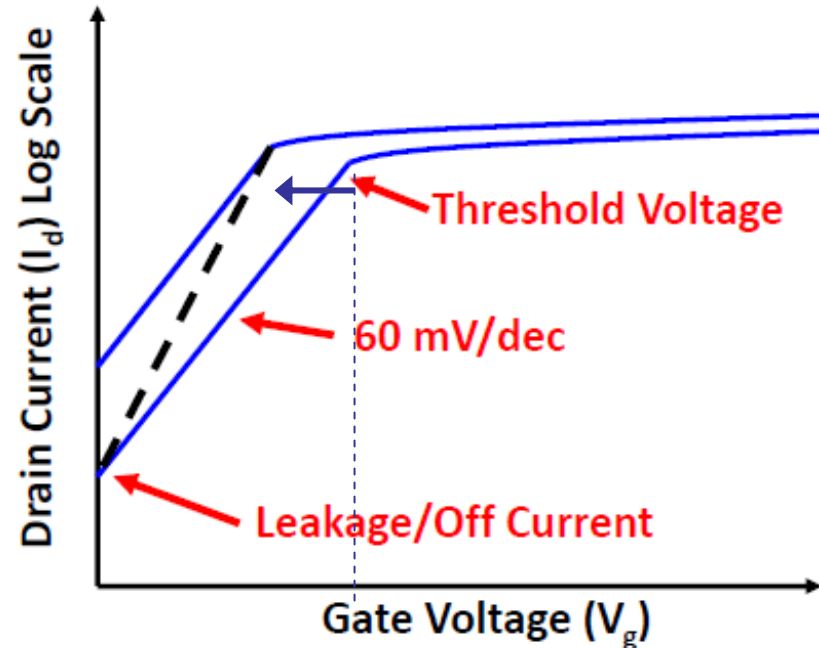
$$I_D \sim (V_{CC} - V_{TH})$$

At very low  $V_{CC}$  we need small  $V_{TH}$  for reasonable drive

**BUT**

Sub-threshold slope is limited by thermal  $kT/q$  limit  
→  $I_{off}$  increases exponentially with  $V_{TH}$  scaling.

**HOW TO BEAT  $kT/q$  limit?**

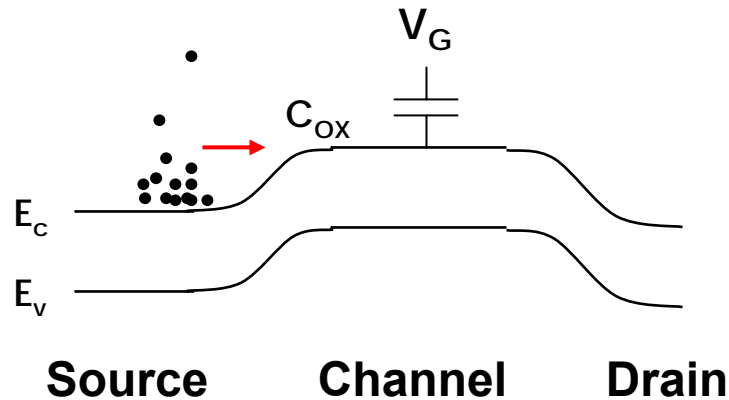


$$S = \left( \frac{d \log I_d}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_d}{C_{ox}} \right) \geq 2.3 \frac{kT}{q}$$

Leakage current increases *exponentially* as device is scaled

# Ultimate Frontier: Overcoming Thermal $kT/q$ Limit

C. Hu, STEEP Program

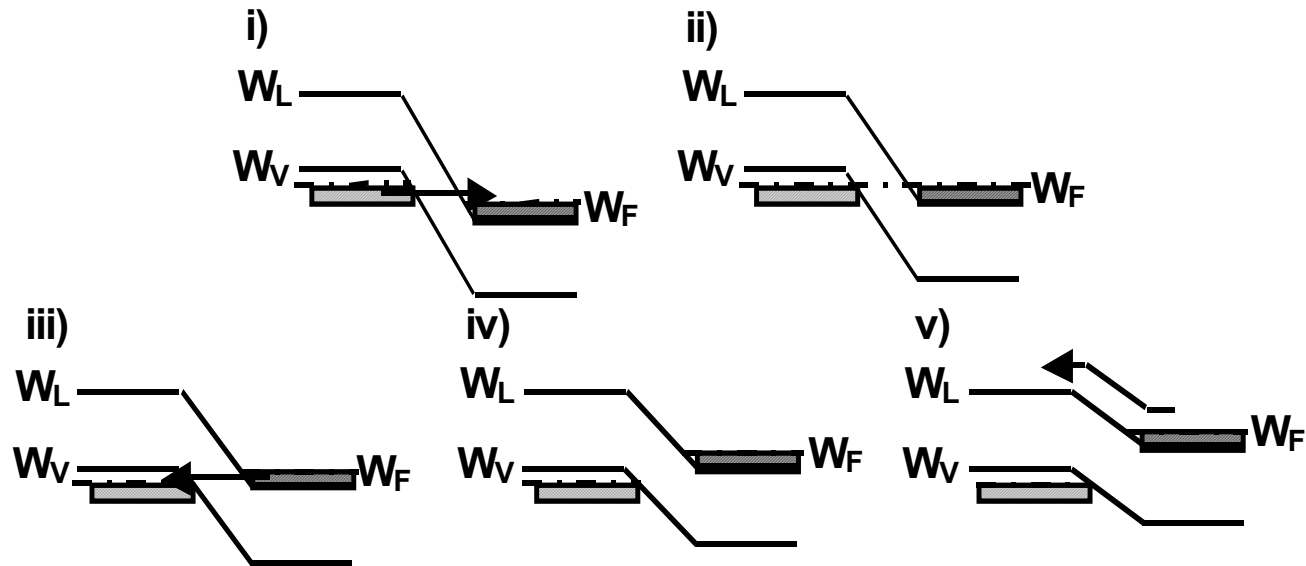


Electrons go over a potential barrier. Leakage current is determined by the Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET...

**How to overcome the limit:**

Let electrons go **through** the energy barrier, not **over** it → **Tunneling**

# Semiconductor Band-to-Band Tunneling

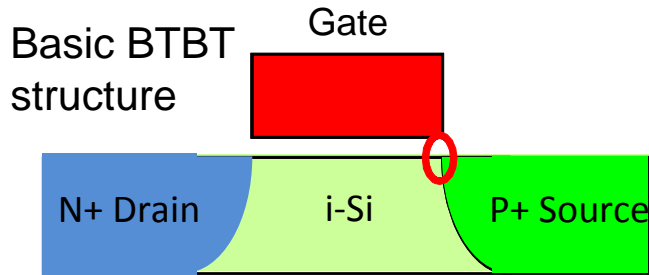


**Leo Esaki**  
**Nobel Prize for Physics 1973**

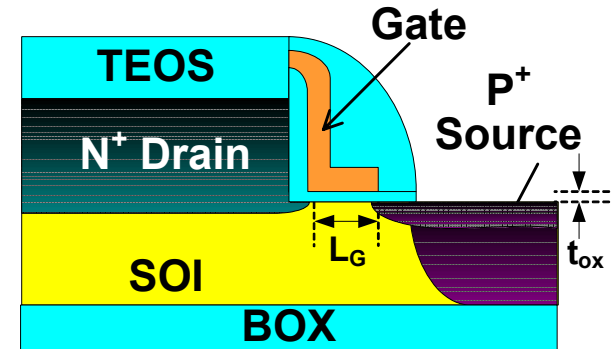
- **Esaki demonstrated this experimentally in 1958**
- **Can lead to negative resistance- Esaki diode**
- **Transistor: Tunneling can be controlled by gate!!**



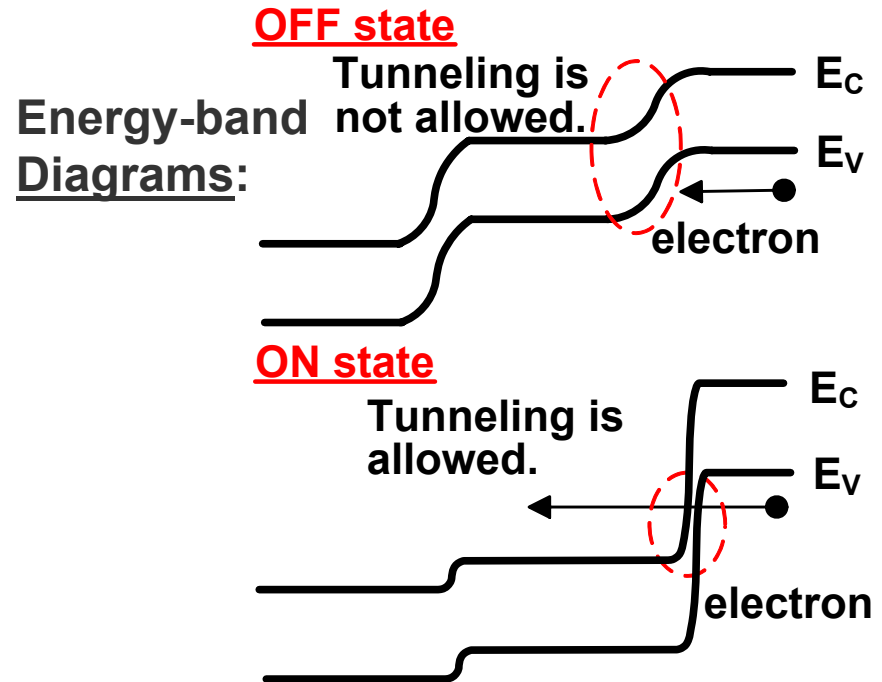
# Tunnel Transistor Concept and Challenges



Structure:



- Device behaves like reverse bias pin diode
- Positive  $V_{gs}$  induces electron channel
- Band bending allows tunneling at source channel interface → Gate controlled band tunneling
- BTBT Transistor suffer from extremely poor drive current → **Need materials with more efficient tunneling**



# Key Messages / Summary

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- **Intel's Response to end of "traditional-scaling":**

Uniaxial Strain (90nm and beyond): 32nm is 4<sup>th</sup> generation of uniaxial strain at Intel  
HiK + Metal Gate (45nm and beyond at Intel)

**These innovations have enabled Intel to maintain historical performance gains on recent nodes**

- **Future Novel Transistors:**

- **New Channel Materials:**

Integrate Ge & III-V on top of Silicon. Many device and material challenges remain

- **Multi-Gate Fin Transistors:**

Scaling benefits BUT need to demonstrate effective strain implementation, matched parasitic resistance to planar and overcome patterning challenges

- **BTBT (Tunnel) Transistors:**

Ultimate transistors may need tunnel injection at ultra-low V<sub>cc</sub>. Would need new materials with more efficient tunneling and atomic scale fabrication control

**Many exciting materials, physics and integration challenges left to continue CMOS scaling**