Lecture 01
FET review (part 1)

Specific topics include PN junctions, basic transistor structure, (transistor) modes of operation, first order I_{ds} models, an initial discussion of scaling models

(Some slides based on lecture notes by David Harris)

How we'll evaluate / study new devices

- Main goal:
  - Applications are generally executed by some technology "on chip"
  - Chips are usually comprised of different functional units
  - Functional units are made up of different sub circuits
  - Circuits are made up of devices

How we'll evaluate / study new devices

- Generally, given the above, we'll work backwards.
  - In other words, we'll start with the device and try to answer the following questions:
    - How does the device work?
    - How does it represent a 1 or 0?
    - How fast does the device switch between states?
    - How much energy is associated with switching?
    - How reliable is it?
    - How does 1 device interact with another? (e.g. how devices interconnected?)
    - What's the fundamental logic function the device supports? (What does transistor-based computation support well? AND/OR? Inversion? XOR?)

How we'll evaluate / study new devices

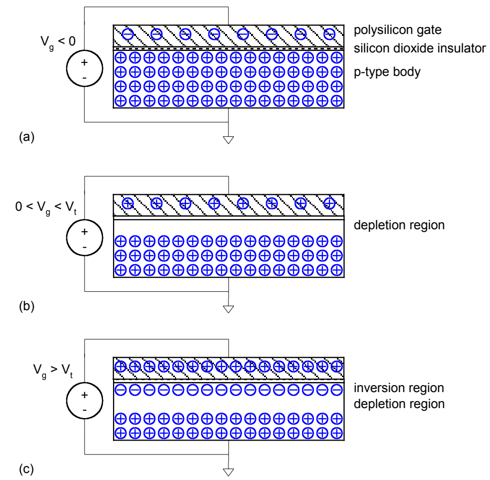
- Once we can answer these questions we can extrapolate device-level performance, to circuit performance, etc.

Outline for Lecture 02

- (Board)
  - Review of PN junctions
    - Important not only for transistors, but other devices studied in class too
- (Board + Slides)
  - Review of basic transistor structures
  - Review of basic modes of operation
  - Review of I_{ds} associated with given mode of operation
- (Board)
  - Impact of scaling on I_{ds}, other parameters…
  - …and the net effect on *systems*

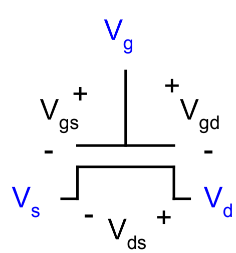
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes



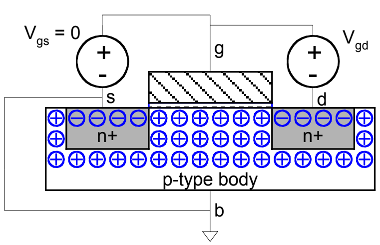
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g – V_s$
  - $V_{gd} = V_g – V_d$
  - $V_{ds} = V_d – V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



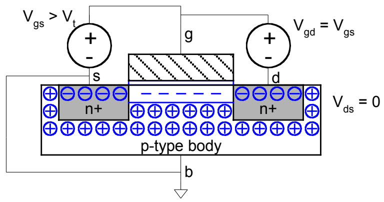
nMOS Cutoff

- No channel formed, so no current flows
- $I_{ds} = 0$

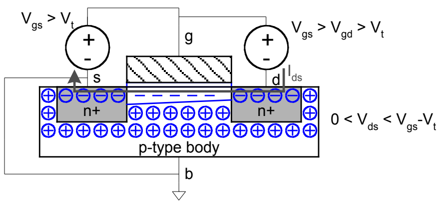


nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



$V_{gs} > V_t$
$V_{ds} = 0$, no current



$V_{gs} > V_t$
$V_{ds} > 0$, but $< (V_{gs} - V_t)$
(current flows)

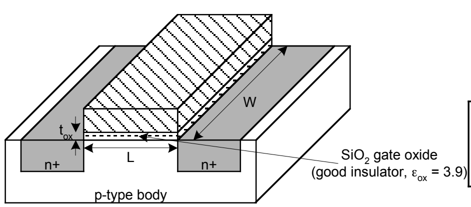
I-V Characteristics

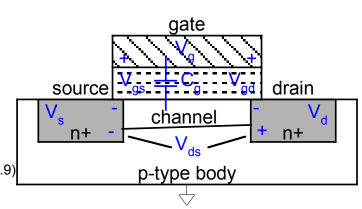
- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- $V = V_{gc} – V_t = (V_{gs} – V_{ds}/2) – V_t$

$C_{ox} = \varepsilon_{ox} / t_{ox}$





Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

- μ is *mobility* → a way to quantify electron velocity and a complex function of crystal structure, local field, etc.
  - People are looking for ways to improve (HW 1)

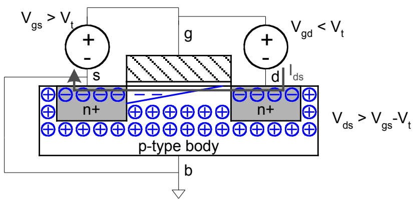
nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$
$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$
$$= \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} \qquad \beta = \mu C_{\text{ox}}\frac{W}{L}$$

nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



$V_{ds} > V_{gs} - V_t$
- Essentially, voltage difference over induced channel fixed at $V_{gs} - V_t$
- (current flows, but saturates)
- (or i_{ds} no longer a function of V_{ds})

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - \frac{V_{dsat}}{2}\right)V_{dsat}$$
$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Scaling models

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		1/S	1/S	1/S
V_{dd}, V_t		1/S	1/U	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	1/S	1/S	1/S
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	1/S	1/U	1
Current Density	I_{sat}/Area	S	S^2/U	S^2
R_{on}	V/I_{sat}	1	1	1
Intrinsic Delay	$R_{on}C_{gate}$	1/S	1/S	1/S
P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	P/Area	1	S^2/U^2	S^2

t_{ox}