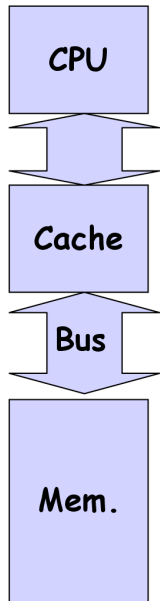


Board Notes on Memory Organization and Disk I/O

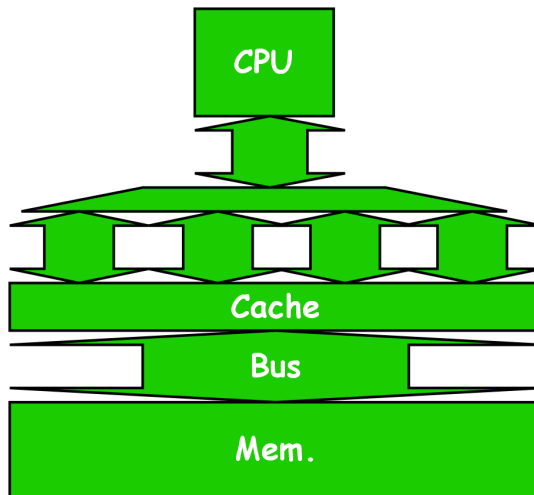
Part A: Memory Organization

Main memory can be organized in several different ways (see picture below)

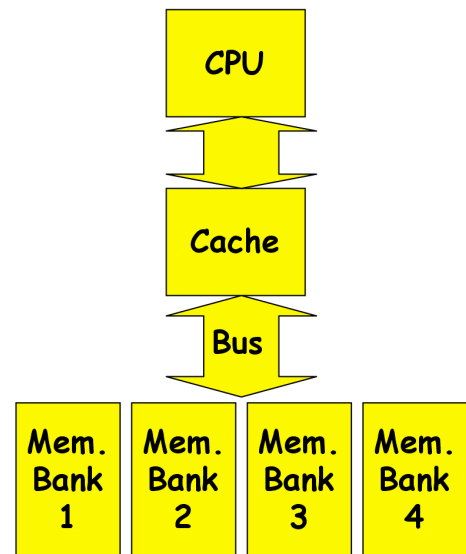
One-word-wide



Multyword-wide



Interleaved



Part A:

Given:

- A cache block size of 4 words
- 1 CC to send address to memory (e.g. time on bus)
- 10 CCs for each DRAM access initiated
- 1 CC to send a word of data on the bus

For a one-word-wide configuration, what is the miss penalty? How many bytes are transferred per CC?

- Miss penalty:
 - o 1 CC to send address + number of accesses x (access time + transfer time)
 - Transfer time is # of times bus is used
 - o Therefore:
 - $1 + 4 \times (10 + 1)$
 - $1 + 4 \times (11)$
 - 45
- Bytes / CC
 - o $4 \text{ words} \times (4 \text{ bytes / word}) / 45 \text{ CCs} = 0.36 \text{ Bytes / CC}$

Part B:

Now, if we use wider memory/cache, also need to increase the bandwidth between levels – otherwise, the wider memory/cache is not much good! For this example, let's add BW and assume the following:

- Main memory is 4 words wide
- We have the same cache/memory access times as before.

What is the miss penalty? How many bytes are transferred per clock cycle?

- Miss penalty:
 - o 1 CC to send address + number of accesses x (access time + transfer time)
 - Transfer time is # of times bus is used
 - o Therefore:
 - $1 + 1 \times (10 + 1)$
 - $1 + 1 \times (11)$
 - 12
- Bytes / CC
 - o $4 \text{ words} \times (4 \text{ bytes / word}) / 12 \text{ CCs} = 1.33 \text{ Bytes / CC}$
 - o 4x better, but 4x more HW too.

Part C:

With multiple DRAM chips, we could *interleave* them to get some parallelism and organize the data such that parallel reads are in fact practical. Further, assume the following:

- The bandwidth between the cache and main memory is the same as in Part A
- DRAM banks are one word wide
- By sending an address, all 4 banks can be addressed simultaneously, but data must be sent back serially.

What is the miss penalty? How many bytes are transferred per clock cycle?

- Miss penalty:
 - o Send time + access time x transfer time
 - o $1 + 10 \times (4 \times 1)$
 - o 15 CCs
- Bytes / CC
 - o $4 \text{ words} \times (4 \text{ bytes / word}) / 15 \text{ CCs} = 1.1 \text{ Bytes / CC}$
 - o 12 vs. 15 – for 75% less bandwidth!

Part B: Disk Seek Time

Part A:

A disk has the following parameters:

- 3600 RPM (= 60 Rotations per second – may help to think in terms of tracks per second)
- Average seek time = 9 ms
- 100 sectors per track, 512 bytes per sector
- Controller + queuing delays = 1 ms

What is the average time to read 1 sector (512 Bytes)?

$$\begin{aligned} \text{Rate_transfer} &= 100 \text{ sectors/track} * 512 \text{ Bytes/sector} * 60 \text{ RPS} &&= 2.4 \text{ MB/s} \\ \text{T_transfer} &= 512 \text{ B} / 2.4 \text{ MB/s} &&= 0.2 \text{ ms} \\ \text{T_rotation} &= 0.5 / 60 \text{ RPS} &&= 8.3 \text{ ms} \\ & \text{(on average, disk must rotate } \frac{1}{2} \text{ way around)} \end{aligned}$$

$$\text{T_disk} = 9 \text{ ms (seek)} + 8.3 \text{ ms (rotation)} + 0.2 \text{ ms (transfer)} + 1 \text{ ms (controller)} = 18.5 \text{ ms}$$

Notes:

- T_transfer only small part! What does this suggest?
 - o Bring in lots of information at a time so you don't have to pay mechanical overhead
- Also, t_queuing can get worse with more requests pending.

Part B:

A disk drive has 15 platters. Each platter has 2 surfaces. The drive has 250 cylinders. Each track has 256 sectors. Each sector has 64 bytes. The average seek time is 3 ms.

What is the average disk access time if we want to transfer 4,096 bytes (i.e. 4KB) of data, our disk rotates at 15,000 RPM, and there is a controller overhead of 2 ms? **Be exact. Do not round.**

Answer:

$$\begin{aligned} \text{Transfer Rate} &= 0.25 \text{ rotations / ms} * 256 \text{ sectors / track} * 64 \text{ bytes / sector} = 4096 \text{ bytes/ms} \\ \text{Average Disk Access Time} &= 3 \text{ ms (for average seek time)} + \\ & .5 / [15000 \text{ RPM} * (1 \text{ min} / 60\text{s}) * (1 \text{ s} / 1000 \text{ ms})]^{\$} + \\ & 4096 \text{ bytes} / 4096 \text{ bytes / ms} + \\ & 2 \text{ (controller overhead)} \\ \text{Average Disk Access Time} &= 3 + 0.125 \text{ ms} + 1 \text{ ms} + 2 \text{ ms} \\ \text{Average Disk Access Time} &= 6.125 \text{ ms} \end{aligned}$$

Part C: Disk Seek Time

The test sequence is: 1011, 57, 272, 40, 512, 717, 320
The disk head starts at 117.

Part A:

What is the total distance the disk head moves with the Shortest Seek Time First algorithm?

Answer: $117 \rightarrow 57 \rightarrow 40 \rightarrow 272 \rightarrow 320 \rightarrow 512 \rightarrow 717 \rightarrow 1011$
 $(117-57) + (57-40) + (272-40) + (320-272) + (512-320) + (717-512) + (1011-717)$
 $= 1048$

Part B:

There is a potential problem with using the Shortest Seek Time First (SSTF) algorithm. In 10 words or less, describe it.

Answer: **Starvation**