Chapter 8: Power Management

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and I/O Timing
  - Active Memory
  - Power Subsystem
  - Battery
  - DC – DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scheduling
  - Conceptual Architecture
    - Architectural Overview

Power Management

Energy is a scarce resource in WSNs for the following reasons:

1. the nodes are very small in size to accommodate high-capacity power supplies compared to the complexity of the task they carry out
2. it is impossible to manually change, replace, or recharge batteries - WSNs consist of a large number of nodes
3. the size of nodes is still a constraining factor for renewable energy and self-recharging mechanisms
4. the failure of a few nodes may cause the entire network to fragment prematurely

Energy is a scarce resource in WSNs for the following reasons:

1. the nodes are very small in size to accommodate high-capacity power supplies compared to the complexity of the task they carry out
2. it is impossible to manually change, replace, or recharge batteries - WSNs consist of a large number of nodes
3. the size of nodes is still a constraining factor for renewable energy and self-recharging mechanisms
4. the failure of a few nodes may cause the entire network to fragment prematurely
Power Management

- The problem of power consumption can be approached from two angles:
  - develop energy-efficient communication protocols
  - self-organization, medium access, and routing protocols
- identify activities in the networks that are both wasteful and unnecessary then mitigate their impact
- Most inefficient activities are results of non-optimal configurations in hardware and software components:
  - e.g., a considerable amount of energy is wasted by an idle processing or a communication subsystem
  - a radio that aimlessly senses the media or overhears while neighboring nodes communicate with each other consumes a significant amount of power

Power Management

- Wasteful and unnecessary activities can be described as local or global
  - e.g., some nodes exhausted their batteries prematurely because of unexpected overhearing of traffic that caused the communication subsystem to become operational for a longer time than originally intended
  - some nodes exhausted their batteries prematurely because they aimlessly attempted to establish links with a network that had become no longer accessible to them

Power Management

- A dynamic power management (DPM) strategy ensures that power is consumed economically
  - the strategy can have a local or global scope, or both
  - a local DPM strategy aims to
    - minimize the power consumption of individual nodes
      - by providing each subsystem with the amount of power that is sufficient to carry out a task at hand
    - when there is no task to be processed, the DPM strategy forces some of the subsystems to operate at the most economical power mode or puts them into a sleeping mode
  - a global DPM strategy attempts to
    - minimize the power consumption of the overall network by defining a network-wide sleeping state
Power Management

- Synchronous sleeping schedule
  - Let individual nodes define their own sleeping schedules
  - Share these schedules with their neighbors to enable a coordinated sensing and an efficient inter-node communication
  - The problem is that neighbors need to synchronize time as well as schedules and the process is energy intensive

- Asynchronous sleeping schedule
  - Let individual nodes keep their sleeping schedules to themselves
  - A node that initiates a communication should send a preamble until it receives an acknowledgment from its receiving partner
  - Avoids the need to synchronize schedules
  - It can have a latency side-effect on data transmission

In both approaches, individual nodes wake up periodically

- To determine whether there is a node that wishes to communicate with them
- To process tasks waiting in a queue

Fundamental premises about Embedded systems:

- Predominantly event-driven
- Experience non-uniform workload during operation time
- DPM refers to selectively shutting-off and/or slowing-down system components that are idle or underutilised
- A policy determines the type and timing of power transitions based on system history, workload and performance constraints
Power Management

- It has been described in the literature as a linear optimisation problem
  - the objective function is the expected performance
    - related to the expected waiting time and the number of jobs in the queue
  - the constraint is the expected power consumption
    - related to the power cost of staying in some operation state and the energy consumption for the transfer from one server state to the next

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC – DC Converter
  - Dynamic Power Management
    - Dynamic Operation Modes
    - Transition Costs
    - Dynamic Scaling
    - Task Scheduling
  - Conceptual Architecture
    - Architectural Overview

Local Power Management Aspects

- The first step is the understanding of how power is consumed by the different subsystems of a wireless sensor node, this knowledge enables
  - wasteful activities to be avoided and to frugally budget power
  - one to estimate the overall power dissipation rate in a node and how this rate affects the lifetime of the entire network
- In the following subsections, a mode detail observation into the different subsystems of a node is made
Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
  - Dynamic Power Management
    - Dynamic Operation Modes
    - Transition Costs
    - Dynamic Scaling
    - Task Scheduling
  - Conceptual Architecture
    - Architectural Overview

Processor Subsystem

- Most existing processing subsystems employ microcontrollers, notably
  - Intel's StrongARM and Atmel's AVR
- These microcontrollers can be configured to operate at various power modes
  - e.g., the ATmega128L microcontroller has six different power modes:
    - idle, ADC noise reduction, power save, power down, standby, and extended standby

<table>
<thead>
<tr>
<th>Sleep Mode</th>
<th>Active clock domains</th>
<th>Oscillators</th>
<th>Wake up sources</th>
<th>REST</th>
<th>Wake</th>
<th>Standby</th>
<th>Ready</th>
<th>Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power down</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X X X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power save</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X X X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X X X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXT standby</td>
<td>X X X X X X X X X X X</td>
<td>X X X X X X X X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td>X X X X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: ATMEAL, Atmega 128L: 2008
Processor Subsystem

- The **idle** mode stops the CPU
  - while allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning
- The **power down** mode saves the registers’ content
  - while freezing the oscillator and disabling all other chip functions until the next interrupt or Hardware Reset
- In the **power-save** mode, the asynchronous timer continues to run
  - allowing the user to maintain a timer base while the remaining components of the device enter into a sleep mode

Processor Subsystem

- The **ADC noise reduction** mode stops the CPU and all I/O modules
  - except the asynchronous timer and the ADC
  - the aim is to minimize switching noise during ADC conversions
- In **standby** mode, a crystal/resonator oscillator runs while the remaining hardware components enter into a sleep mode
  - this allows very fast start-up combined with low power consumption
- In **extended standby** mode, both the main oscillator and the asynchronous timer continue to operate

Processor Subsystem

- Additional to the above configurations, the processing subsystem can operate with different supply voltages and clock frequencies
- **Transiting** from one power mode to another also has its own power and latency cost
Power state machine for the StrongARM-1100 processor

- Processor Subsystem
- Communication Subsystem
- Bus Frequency and I/O Timing
- Active Memory
- Power Subsystem
  - Supply
  - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation/Mode
  - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview

The power consumption of the communication subsystem can be influenced by several aspects:
- the modulation type and index
- the transmitter’s power amplifier and antenna efficiency
- the transmission range and rate
- the sensitivity of the receiver
- These aspects can be dynamically reconfigured
Communication Subsystem

- Determining the most efficient active state operational mode is *not a simple decision*
  - e.g., the power consumption of a transmitter may *not* necessarily be reduced by simply reducing the transmission rate or the transmission power
  - the reason is that there is a *tradeoff* between the useful power required for data transmission and the power dissipated in the form of heat at the power amplifier
  - usually, the dissipation power (heat energy) *increases* as the transmission power *decreases*
  - in fact most commercially available transmitters operate efficiently at one or two transmission power levels
    - below a certain level, the efficiency of the power amplifier *falls drastically*

- In some cheap transceivers, even when at the maximum transmission power mode, more than *60%* of the supply DC power is dissipated in the form of useless *heat*
- For example, the *Chipcon CC2420* transceiver has eight programmable output power levels ranging from −24 dBm to 0 dBm

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC – DC Converter
  - Dynamic Power Management
    - Dynamic Operation Modes
    - Transition Costs
    - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview
Bus Frequency and RAM Timing

- The processor subsystem consumes power when it interacts with the other subsystems via the internal high-speed buses.
- The specific amount depends on the frequency and bandwidth of the communication.
- These two parameters can be optimally configured depending on the interaction type, but bus protocol timings are usually optimized for particular bus frequencies.
- Moreover, bus controller drivers require to be notified when bus frequencies change to ensure optimal performance.

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
    - Power Subsystem
    - Bus
    - DC–DC Converter
  - Dynamic Power Management
    - Dynamic Operation Modes
    - Transition Costs
    - Dynamic Scaling
    - Task Scheduling
    - Conceptual Architecture
    - Architectural Overview

Active Memory

- It is made up of capacitor-transistor pairs (DRAM)
  - arranged in rows and columns, each row being a single memory bank
  - have to be recharged periodically in order to store data
- The refresh interval
  - a measure of the number of rows that must be refreshed
  - a low refresh interval corresponds to a high clock frequency
  - a higher refresh interval corresponds to a low clock frequency
Active Memory

Consider two typical values: 2K and 4K
- 2K: refreshes more cells at a low interval and completes the process faster, thus it consumes more power.
- 4K: refreshes less cells at a slower frequency, but it consumes less power.

A DRAM memory unit can be configured to operate in one of the following power modes:
- Temperature-compensated self-refresh mode
- Partial array self-refresh mode
- Power down mode

Active Memory

Temperature-compensated self-refresh mode
- the standard refresh rate of a memory unit can be adjusted according to its ambient temperature

Partial array self-refresh mode
- the self-refresh rate can be increased if the entire memory array is not needed to store data
- the refresh operation can be limited to the portion of the memory array in which data will be stored

Power down mode
- if no actual data storage is required, the supply voltage of most or the entire on-board memory array can be switched off

Active Memory

The RAM timing is another parameter that affects the power consumption of the memory unit
- it refers to the latency associated with accessing the memory unit
- before a processor subsystem accesses a particular cell in a memory, it should first determine the particular row or bank
- then activate the row with a row access strob (RAS) signal
- the activated row can be accessed until the data is exhausted
- the time required to activate a row in a memory is tRAS, which is relatively small but could impact the system’s stability if set incorrectly.
Active Memory

- The delays between the activation of a row (a cell) and the writing of data into or reading of data from the cell is given as $t_{RCD}$
- This time can be short or long, depending on how the memory cell is accessed
- If it is accessed sequentially, it is insignificant
- If it is accessed in a random fashion, the current active row must first be deactivated before a new row is activated
- In this case, $t_{RCD}$ can cause significant latency

- A memory cell is activated through a column access strob (CAS)
- the delay between the CAS signal and the availability of valid data on the data pins is called CAS latency
- low CAS latency means high performance but also high power consumption
- the time required to terminate one row access and begin the next row access is $t_{RP}$
- the time required to switch rows and select the next cell for reading, writing, or refreshing is expressed as $t_{RP} + t_{RCD}$
- the duration of time required between the active and precharge commands is called $t_{RAS}$
- It is a measure of how long the processor must wait before the next memory access can begin

---

### Table 8.2 Parameters of RAM timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>Row Address Strobe or Row Address Select</td>
</tr>
<tr>
<td>CAS</td>
<td>Column Address Strobe or Column Address Select</td>
</tr>
<tr>
<td>$t_{RAS}$</td>
<td>A time delay between the precharge and activation of a row</td>
</tr>
<tr>
<td>$t_{CAS}$</td>
<td>The time required between RAS and CAS access</td>
</tr>
<tr>
<td>$t_{CL}$</td>
<td>CAS latency</td>
</tr>
<tr>
<td>$t_{RP}$</td>
<td>The time required to switch from one row to the next row</td>
</tr>
<tr>
<td>$t_{Cyc}$</td>
<td>The duration of a clock cycle</td>
</tr>
<tr>
<td>Command rate</td>
<td>The delay between Chip Select (CS)</td>
</tr>
<tr>
<td>Latency</td>
<td>The total time required before data can be written to or read from memory</td>
</tr>
</tbody>
</table>
Active Memory

- When a RAM is accessed by clocked logic, the times are generally rounded up to the nearest clock cycle
  - for example, when accessed by a 100-MHz processor (with 10 ns clock duration), a 50-ns SDRAM can perform the first read in 5 clock cycles and additional reads within the same page every 2 clock cycles
  - this is generally described as "5 – 2 – 2 – 2" timing

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
  - Dynamic Power Management
    - Dynamic Operation Modes
    - Transition Costs
    - Dynamic Scaling
    - Task Scheduling
  - Conceptual Architecture
    - Architectural Overview

Power Subsystem

- The power subsystem supplies power to all the other subsystems
- It consists of
  - the battery
  - the DC–DC converter
    - it provides the right amount of supply voltage to each individual hardware component
    - by transforming the main DC supply voltage into a suitable level
    - the transformation can be a step-down (buck), a step-up (boost), or an inversion (flyback) process, depending on the requirements of the individual subsystem
Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview

Battery

- A wireless sensor node is powered by **exhaustible batteries**
  - the main factor affect the quality of these batteries is **cost**
- Batteries are specified by a rated current capacity, $C$, expressed in **ampere-hour**
  - this quantity describes the rate at which a battery discharges without significantly affecting the prescribed supply voltage
  - as the discharge rate **increases**, the rated capacity **decreases**
  - most portable batteries are rated at 1C
    - this means a 1000 mAh battery provides 1000mA for 1 hour, if it is discharged at a rate of 1C
    - e.g., at a rate of 0.5C, providing 500mA for 2 hours
    - at a rate of 2C, 2000mA for 30 minutes
- In reality, batteries perform at **less than the prescribed rate**. Often, the **Peukert Equation** is applied to quantifying the capacity offset
  \[ t = \frac{C}{I^n} \]
  
  - where $C$ is the theoretical capacity of the battery expressed in ampere-hours
  - $I$ is the current drawn in Ampere ($A$)
  - $t$ is the time of discharge in seconds
  - $n$ is the Peukert number, a constant that directly relates to the internal resistance of the battery
Battery

- The value of the Peukert number indicates how well a battery performs under continuous heavy currents
  - A value close to 1 indicates that the battery performs well
  - The higher the number, the more capacity is lost when the battery is discharged at high currents
- Figure 8.3 shows how the effective battery capacity can be reduced at high and continuous discharge rates
  - By intermittently using the battery, it is possible during quiescent periods to increase the diffusion and transport rates of active ingredients and to match up the depletion created by excessive discharge
  - Because of this potential for recovery, the capacity reduction can be undermined and the operating efficiency can be enhanced

---

Figure 8.3 The Peukert curve displaying the relationship between the discharging rate and the effective voltage. The x-axis is a time axis.

---

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC-DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scheduling
- Conceptual Architecture
  - Architectural Overview
DC – DC Converter

- The DC – DC converter transforms one voltage level into another
- The main problem is its conversion efficiency
- A typical DC – DC converter consists of
  - a power supply
  - a switching circuit
  - a filter circuit
  - a load resistor

Figure 8.4 A DC – DC converter consisting of a supply voltage, a switching circuit, a filter circuit, and a load resistance

In the figure 8.4, the circuit consists of a single-pole, double-throw (SPDT) switch
- SPDT is connected to a DC supply voltage, \( V_c \)
- considering the inductor, \( L \), as a short circuit
- the capacitor, \( C \), as an open circuit for the DC supply voltage
- the switch’s output voltage, \( V_s(t) = V_g \) when the switch is in position 1
- \( V_s(t) = 0 \) When it is in position 2
- varying the position of the switch at a frequency, \( f_s \), yields a periodically varying square wave, \( v_s(t) \), that has a period \( T_s = 1/f_s \)
- \( v_s(t) \) can be expressed by a duty cycle \( D \)
- \( D \) describes the fraction of time that the switch is in position 1, \( 0 \leq D \leq 1 \)
DC – DC Converter

- A DC – DC converter is realized
  - by employing active switching components
  - such as diodes and power MOSFETs
- Using the inverse Fourier transformation
  - the DC component of \( v_s(t) \) is described as:
    \[
    \bar{v}_s = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = D V_s
    \]
  - which is the average value of \( v_s(t) \)
  - In other words, the integral value represents the area under the waveform of Figure 8.5 for a single period, or the height of \( V_s \) multiplied by the time \( T_s \)
  - It can be seen that the switching circuit reduces the DC component of the supply voltage by a factor that equals to the duty cycle, \( D \)
  - Since \( 0 \leq D \leq 1 \) holds, the expression: \( V_s \leq V_g \) is true

The switching circuit consumes power
- due to the existence of a resistive component in the switching circuit, there is power dissipation
- the efficiency of a typical switching circuit is between 70 and 90%
- In addition to the desired DC voltage, \( v_s(t) \) also contains undesired harmonics of the switching frequency, \( f_s \)
  - these harmonics must be removed so that the converter’s output voltage \( v(t) \) is essentially equal to the DC component \( \bar{v} = V_s \)
  - for this purpose, a DC – DC converter employs a lowpass filter

---

Figure 8.5 The output voltage of a switching circuit of a DC – DC converter.
In Figure 8.4, a first-order LC lowpass filter is connected to the switching circuit.

- The filter's cutoff frequency is given by:
  \[ f_c = \frac{1}{2\pi\sqrt{LC}} \]  
  (Equation 8.3)

- The cutoff frequency, \( f_c \), should be sufficiently less than the switching frequency, \( f_s \), so that the lowpass filter allows only the DC component of \( v_s(t) \) to pass.

- In an ideal filter, there is no power dissipation because the passive components (inductors and capacitors) are energy storage components.

- Subsequently, the DC-DC converter produces a DC output voltage whose magnitude is controlled by the duty cycle, \( D \), using circuit elements that (ideally) do not dissipate power.

The conversion ratio, \( M(D) \), is defined as the ratio of the DC output voltage, \( V \), to the DC input voltage, \( V_g \), under a steady-state condition:

\[
M(D) = \frac{V}{V_g} \]  
(Equation 8.4)

- For the buck converter shown in Figure 8.4, \( M(D) = D \).

- Figure 8.6 illustrates the linear relationship between the input DC voltage, \( V_g \), and the switching circuit's duty cycle, \( D \).

![Figure 8.6](image.png)
Dynamic Power Management

Once the design time parameters are fixed, a dynamic power management (DPM) strategy attempts to:

- minimize the power consumption of the system by dynamically defining the most economical operation conditions
- this condition takes the requirements of the application, the topology of the network, and the task arrival rate of the different subsystems into account.

Different approaches to a DPM strategy can be categorized:

1. dynamic operation modes
2. dynamic scaling
3. energy harvesting
Dynamic Operation Modes

- In general, a subcomponent or a part can have \( n \) different power modes
  - if there are \( x \) hardware components that can have \( n \) distinct power consumption levels, a DPM strategy can define \( x \times n \) different power mode configurations, \( P_{n} \)
- The task of the DPM strategy is:
  - select the optimal configuration that matches the activity of a wireless sensor node
- Two associated challenges:
  1. transition between the different power configurations costs extra power
  2. a transition has an associated delay and the potential of missing the occurrence of an interesting event

Selective Switching

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{\text{on}} )</td>
<td>10 W</td>
</tr>
<tr>
<td>( P_{\text{off}} )</td>
<td>0 W</td>
</tr>
<tr>
<td>( P_{\text{low}} )</td>
<td>-40 W</td>
</tr>
<tr>
<td>( P_{\text{sleep}} )</td>
<td>2 s</td>
</tr>
<tr>
<td>( t_{\text{on}} )</td>
<td>1 s</td>
</tr>
<tr>
<td>( t_{\text{off}} )</td>
<td>25 s</td>
</tr>
</tbody>
</table>

Policy Energy Avg. Latency

- Always on: 250 J 1 s
- Reactive greedy: 240 J 3 s
- Power-aware: 140 J 2.5 s

Source: Pedram, 2003

Dynamic Operation Modes

- Memory access

Source: Ellis, 2003
Selective Switching

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>StrongARM</th>
<th>Memory</th>
<th>MEEMS &amp; ADC</th>
<th>RF</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;0&lt;/sub&gt;</td>
<td>Sleep</td>
<td>Sleep</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>P&lt;sub&gt;1&lt;/sub&gt;</td>
<td>Sleep</td>
<td>Sleep</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>P&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Idle</td>
<td>Sleep</td>
<td>On</td>
<td>RX</td>
</tr>
<tr>
<td>P&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Active</td>
<td>Active</td>
<td>On</td>
<td>TX, RX</td>
</tr>
</tbody>
</table>

Source: Sinha and Chandrakasan, 2001

Dynamic Operation Modes

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Processor</th>
<th>Memory</th>
<th>Sensing subsystem</th>
<th>Communication subsystem</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;0&lt;/sub&gt;</td>
<td>Active</td>
<td>Active</td>
<td>On</td>
<td>Transmit/receiving</td>
</tr>
<tr>
<td>P&lt;sub&gt;1&lt;/sub&gt;</td>
<td>Active</td>
<td>On</td>
<td>On</td>
<td>On (transmitting)</td>
</tr>
<tr>
<td>P&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Idle</td>
<td>On</td>
<td>On</td>
<td>Receiving</td>
</tr>
<tr>
<td>P&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Sleep</td>
<td>On</td>
<td>Off</td>
<td>Receiving</td>
</tr>
<tr>
<td>P&lt;sub&gt;4&lt;/sub&gt;</td>
<td>Sleep</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>P&lt;sub&gt;5&lt;/sub&gt;</td>
<td>Sleep</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

Table 8.3 Power saving configurations

DFN strategy with six different power modes: {P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>, P<sub>4</sub>, P<sub>5</sub>}
Dynamic Operation Modes

- The decision for a particular power mode depends on
  - the anticipated task in the queues of the different hardware components
- Failure to realistically estimate future tasks can cause a node to miss interesting events or to delay in response
- In a WSN, the events outside of the network cannot be modeled as deterministic phenomena
  - e.g., a leak in a pipeline; a pestilence in a farm
  - no need for setting up a monitoring system
- An accurate event arrival model enables a DPM strategy to decide for the right configuration that has a long duration and minimal power consumption

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and I/O Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
  - Task Scheduling
  - Conceptual Architecture
    - Architectural Overview

Transition Costs

- Suppose:
  - each subsystem of a wireless sensor node operates in just two different power modes only, it can be either on or off
  - moreover, assume that the transition from on to off does not have an associated power cost
  - but the reverse transition (from off to on) has a cost in terms both of power and a time delay
  - these costs are justified if the power it saves in the off state is large enough
  - in other words, the amount of the off state power is considerably large and the duration of the off state is long
  - it is useful to quantify these costs and to set up a transition threshold
Transition Costs

- Suppose:
  - the minimum time that a subsystem stays in an off state is $t_{\text{off}}$
  - the power consumed during this time is $P_{\text{off}}$
  - the transition time is $t_{\text{off,\text{on}}}$
  - the power consumed during the transition is $P_{\text{off,\text{on}}}$
  - the power consumed in an on state is $P_{\text{on}}$

  Hence:
  \[ P_{\text{off}} \cdot t_{\text{off}} + P_{\text{off,\text{on}}} \cdot t_{\text{off,\text{on}}} + P_{\text{on}} \cdot (t_{\text{off}} + t_{\text{off,\text{on}}}) \]  
  Equation (8.5)

- therefore, the transition is justified if:
  \[ t_{\text{off}} \geq \max \left( 0, \frac{(P_{\text{off}} - P_{\text{on}}) t_{\text{off,\text{on}}}}{P_{\text{on}} - P_{\text{off}}} \right) \]  
  Equation (8.6)

- Equations (8.5) and (8.6) can describe a subsystem with $n$ distinct operational power modes
  - in this case a transition from any state $i$ into $j$ is described as $t_{ij}$
  - hence, the transition is justified if Equation (8.7) is satisfied
  \[ t_{ij} \geq \max \left( 0, \frac{(P_{ij} - P_{ji}) t_{ij}}{P_{ij} - P_{ji}} \right) \]  
  Equation (8.7)

  where $t_i$ is the duration of the subsystem in state $i$

- If the transition cost from a higher power mode (on) to a lower power mode (off) is not negligible
  - the energy that can be saved through a power transition (from state $i$ to state $j$, $E_{\text{saved}}$) is expressed as:
    \[ E_{\text{saved},ij} = P_{ij} \cdot \left( t_{ij} + t_{ij} \right) \cdot \left( P_{ij} + P_{ji} \cdot t_{ij} + P_{ji} \cdot t_{ij} \right) \]  
    Equation (8.8)

  - If the transition from state $i$ to state $j$ costs the same amount of power and time delay as the transition from state $j$ to state $i$, it can be expressed as:
    \[ E_{\text{saved},ij} = P_{ij} \cdot \left( t_{ij} + t_{ij} \right) \cdot \left( \frac{P_{ij} + P_{ji}}{2} \right) \cdot \left( P_{ij} + P_{ji} \cdot t_{ij} \right) \]  
    Equation (8.9)
Transition Costs

- Obviously, the transition is justified if $E_{\text{saved}} > 0$. This can be achieved in three different ways, by:
  1. increasing the gap between $P_i$ and $P_j$
  2. increasing the duration of state $P_j$
  3. decreasing the transition times, $t_{ji}$

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and I/O Timer
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview

Dynamic Scaling

- Dynamic voltage scaling (DVS) and dynamic frequency scaling (DFS) aim to:
  - adapt the performance of the processor core when it is in the active state

- In most cases, the tasks scheduled to be carried out by the processor core do not require its peak performance

- Some tasks are completed ahead of their deadline and the processor enters into a low-leakage idle mode for the remaining time

- In Figure 8.8, even though the two tasks are completed ahead of their schedule, the processor still runs at peak frequency and supply voltage - wasteful
Dynamic Scaling

In Figure 8.9 the performance of the processing subsystem is adapted (reduced) according to the criticality of the tasks it processes:

- Each task is stretched to its planned schedule while the supply voltage and the frequency of operation are reduced.

The basic building blocks of the processor subsystem are transistors:

- They are classified into analog and digital (switching) transistors.
- Depending on their operation regions (namely, cut-off, linear, and saturation).
Dynamic Scaling

- An analog transistor (amplifier)
  - operates in the linear amplification region
  - there is a linear relationship between the input and the output of the transistor. This is expressed as:
    \[ V_{\text{out}} = \frac{A}{1-AB} V_{\text{in}} \]  
    where \( A \) is the gain of the amplifier
  - \( B \) is a term that determines the portion of the output that should be fed back to the input in order to stabilize the amplifier

Dynamic Scaling

- A digital (switching) transistor
  - operates in either the cutoff or the saturation region
  - makes the relationship between the input and the output voltage nonlinear
  - that is how the zeros and ones of a digital system are generated, represented or processed
  - the transition duration from the cutoff to the saturation region determines how good a transistor is as a switching element
    - in an ideal switching transistor, the transition takes place in no time
    - in practical transistors, the duration is greater than zero
  - the quality of the processor depends on the switching time

Dynamic Scaling

- The switching time in turn depends on
  - the cumulative capacitance effect created between the three joints of the transistors
  - Figure 8.10 displays a typical NAND gate made up of CMOS transistors

- A capacitor is created by two conductors
  - two conductors are separated by a dielectric material
  - there is a potential difference between the two conductors

- The capacitance of a capacitor is
  - positive proportional to the cross-sectional area of the conductors
  - inversely proportional to the separating distance
Dynamic Scaling

- In a switching transistor:
  - a capacitance is created at the contact points of the source, gate, and drain
  - affecting the transistor’s switching response
  - the switching time can be approximated by the following equation:

\[ t_{\text{delay}} = \frac{C_s V_{dd}}{I_{dsat}} \]  
 Equation (8.11)

- where \( C_s \) is the source capacitance, \( V_{dd} \) is the biasing voltage of the drain, and \( I_{dsat} \) is the saturation drain current.

Dynamic Scaling

- Switching costs energy and the magnitude of the energy depends on:
  - the operating frequency and the biasing voltage

Sinha and Chandrakasan (2001) provide a first-order approximation that can be expressed as:

\[ E(t) = C_s V_{dd} T_s f_{\text{ref}} \left[ \frac{V}{T} + \frac{1}{2} \left( 1 - \frac{V}{T} \right)^2 \right] \]  
 Equation (8.12)

- where, \( C_s \) is the average switching capacitance per cycle
  - \( T_s \) is the sampling period
  - \( f_{\text{ref}} \) is the operating frequency at \( V_{dd} \)
  - \( r \) is the normalized processing rate \( \left( \frac{f}{f_{\text{ref}}} \right) \)
  - \( V_0 = (V_{dd} - V_t) \) being the threshold voltage

- It can be deduced that:
  - reducing the operating frequency linearly reduces the energy cost
  - reducing the biasing voltage reduces the energy cost quadratically

Dynamic Scaling

- However, these two quantities cannot be reduced beyond a certain limit:
  - for example, the minimum operating voltage for a CMOS logic to function properly was first derived by Swanson and Meinl (1972)
  - it is expressed as:

\[ V_0 \text{min,CMOS} = 2 \left( \frac{TF}{sg} \right) \left[ 1 + \frac{C_i}{C_{ox}} + C_i \right] \ln \left( 1 + \frac{C_i}{C_{ox}} \right) \]  
 Equation (8.13)

- where \( C_i \) is the surface state capacitance per unit area
  - \( C_{ox} \) is the gate-oxide capacitance per unit area
  - \( C_i \) is the channel depletion region capacitance per unit area

- finding the optimal voltage limit requires a tradeoff between the switching energy cost and the associated delay.
Task Scheduling

In a dynamic voltage and frequency scaling, the DPM strategy aims to
- autonomously determine the magnitude of the biasing voltage ($V_{dd}$)
- the clock frequency of the processing subsystem
The decision for a particular voltage or frequency is based on:
- the application latency requirement
- the task arrival rate
- ideally, these two parameters are adjusted so that a task is completed “just in time” - the processor does not remain idle and consume power unnecessarily

Practically, idle cycles cannot be completely avoided
- the processor’s workload cannot be known a priori
- the estimation contains error
Comparison between an ideal and real dynamic voltage scaling strategies is shown in Figure 8.11
Task Scheduling

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
- Conceptual Architecture
  - Architectural Overview

Conceptual Architecture

- A conceptual architecture for enabling a DPM strategy in a wireless sensor node should address three essential concerns:
  1. In attempting to optimize power consumption, how much is the extra workload that should be produced by the DPM itself?
  2. Should the DPM be a centralized or a distributed strategy?
  3. If it is a centralized approach, which of the subcomponents should be responsible for the task?
Conceptual Architecture

- A typical DPM strategy:
  - monitors the activities of each subsystem
  - makes decisions concerning the most suitable power configuration
  - optimizes the overall power consumption
  - this decision should take the application requirements
- An accurate DPM strategy requires benchmarking to estimate the task arrival and processing rate

Conceptual Architecture

- A DPM strategy can be
  - central approach
  - distributed approach
- Advantage of a centralized approach
  - it is easier to achieve a global view of the power consumption of a node and to implement a comprehensible adaptation strategy
  - a global strategy can add a computational overhead on the subsystem that does the management
- Advantage of a distributed approach
  - scales well by authorizing individual subsystems to carry out local power management strategies

Conceptual Architecture

- Local strategies may contradict with global goals
- Given the relative simplicity of a wireless sensor node and the quantifiable tasks that should be processed, most existing power management strategies advocate a centralized solution
Conceptual Architecture

- In case of a centralized approach, the main question is
- which subsystems is responsible for handling the task — the processor subsystem or the power subsystem

- The power subsystem
  - has complete information about the energy reserve of the node
  - the power budget of each subsystem
  - but it requires vital information from the processing subsystems
    - the task arrival rate
    - priority of individual tasks
  - it needs to have some computational capability
  - presently available power subsystems do not have these characteristics

Most existing architectures
- place the processor subsystem at the center
- all the other subsystems communicate with each other through it
- the operating system runs on the processing subsystem, managing, prioritizing and scheduling tasks

Subsequently, the processing subsystem
- have more comprehensive knowledge about the activities of all the other subsystems
- these characteristics make it appropriate place for executing a DPM

Outline

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Galaxy
    - DC–DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview
Architectural Overview

- The DPM strategy should not affect the system’s stability
- The application requirements should be satisfied
  - the quality of sensed data and latency
- A WSN is deployed for a specific task
  - that task does not change, or changes only gradually
- The designer of a DPM has at his or her disposal the architecture of the wireless sensor node, the application requirements, and the network topology to devise a suitable strategy

![Diagram showing factors affecting dynamic power management strategy](image)

Figure 8.12 Factors affecting a dynamic power management strategy

Architectural Overview

- The system’s hardware architecture
  - it is the basis for defining multiple operational power modes and the possible transitions between them
- A local power management strategy
  - it defines rules to describe the behavior of the power mode transition
    - according to a change in the activity of the node; or
    - based on a request from a global power management scheme; or
    - based on a request from the application
  - This (see Figure 8.13) can be described as a circular process consisting of three basic operations
    - energy monitoring
    - power mode estimation
    - task scheduling
Figure 8.13 illustrates how dynamic power management can be thought of as a machine that moves through different states in response to different types of events. Tasks are scheduled in a task queue, and the execution time and energy consumption of the system are monitored. Depending on how fast the tasks are completed, a new power budget is estimated and transitions in power modes. The DPM strategy decides the higher level of operating power mode in case of a deviation in the estimated power budget from the power mode.
Architectural Overview

- Figure 8.14 shows
  - an implementation of the abstract architecture of Figure 8.13 to support dynamic voltage scaling
  - the processing subsystem
    - receives tasks from the application, the communication subsystem, and the sensing subsystem
    - handles tasks pertaining to network management such as managing a routing table and sleeping schedules
  - each of these sources produces a task at a rate of $\lambda_i$
  - the overall task arrival rate, $\lambda$, is the summation of the individual tasks arrival rates,
    $$\lambda = \sum \lambda_i$$
  - the workload monitor observes $\lambda_i$ for a duration of $\tau_i$ seconds and predicts the task arrival rate for the next $\beta_i$ seconds

- The estimated task arrival rate is represented by $r$ in the figure
- Based on the newly computed task arrival rate $r$, the processing subsystem estimates the supply voltage and the clock frequency it requires to process upcoming tasks