A Comparison of Various Bipolar Transistor Biasing Circuits

Application Note 1293

Introduction

The bipolar junction transistor (BJT) is quite often used as a low noise amplifier in cellular, PCS, and pager applications due to its low cost. With a minimal number of external matching networks, the BJT can quite often produce an LNA with RF performance considerably better than an MMIC. Of equal importance is the DC performance. Although the device's RF performance may be quite closely controlled, the variation in device dc parameters can be quite significant due to normal process variations. It is not unusual to find a 2 or 3 to 1 ratio in device h_{FE}. Variation in h_{FE} from device to device will generally not show up as a difference in RF performance. In other words, two devices with widely different h_{FE}'s can have similar RF performance as long as the devices are biased at the same V_{CE} and I_C. This is the primary purpose of the bias network, i.e., to keep V_{CE} and I_C constant as the dc parameters vary from device to device.

Quite often the bias circuitry is overlooked due to its apparent simplicity. With a poorly designed fixed bias circuit, the variation in I_C from lot to lot can have the same maximum to minimum ratio as the h_{FE} variation from lot to lot. With no compensation, as h_{FE} is doubled, I_C will double. It is the task of the dc bias circuit to maximize the circuit's tolerance to h_{FE} variations. In addition, transistor parameters can vary over temperature causing a drift in I_C at temperature. The low power supply voltages typically available for handheld applications also make it more difficult to design a temperature stable bias circuit.

One solution to the biasing dilemma is the use of active biasing. Active biasing often makes use of an IC or even just a PNP transistor and a variety of resistors, which effectively sets V_{CE} and I_C regardless of variations in device h_{FE}. Although the technique of active biasing would be the best choice for the control of device to device variability and over temperature variations, the cost associated with such an arrangement is usually prohibitive.

Other biasing options include various forms of passive biasing. Various passive biasing circuits will be discussed along with their advantages and disadvantages.

Various BJT Passive Bias Circuits

Passive biasing schemes usually consist of two to five resistors properly arranged about the transistor. Various passive biasing schemes are shown in Figure 1. The simplest form of passive biasing is shown as Circuit #1 in Figure 1. The collector current I_C is simply h_{FE} times the base current I_B. The base current is determined by the value of R_B. The collector voltage V_{CE} is determined by subtracting the voltage drop across resistor R_C from the power supply voltage V_{CC}. As the collector current is varied, the V_{CE} will change based on the voltage drop across R_C. Varying h_{FE} will cause I_C to vary in a fairly direct manner. For constant V_{CC} and constant V_{BE}, I_C will vary in direct proportion to h_{FE}. As an example, as h_{FE} is doubled, collector current, I_C, will also double. Bias circuit #1 provides no compensation for variation in device h_{FE}.

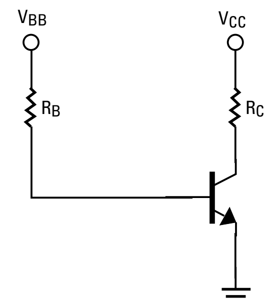


Figure 1A. Circuit #1 – Non-stabilized BJT Bias Network

Bias circuit #2 provides voltage feedback to the base current source resistor R_B. The base current source is fed from the voltage V_{CE} as opposed to the supply voltage V_{CC}. The value of the base bias resistor R_B is calculated based upon nominal

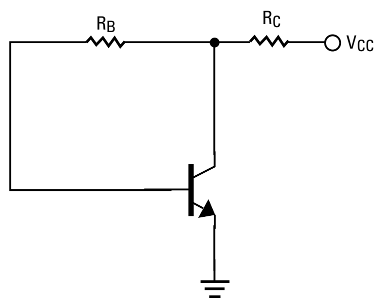


Figure 1B. Circuit #2 – Voltage Feedback BJT Bias Network

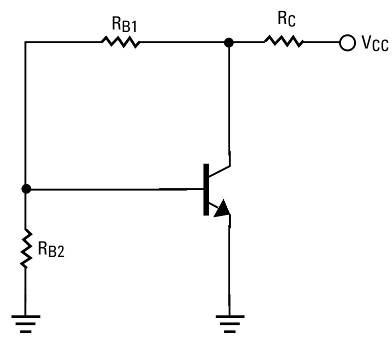


Figure 1D. Circuit #4 – Voltage Feedback with Voltage Source BJT Bias Network

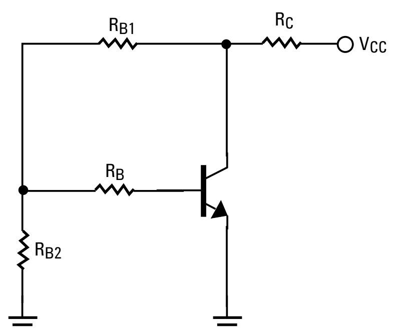


Figure 1C. Circuit #3 – Voltage Feedback with Current Source BJT Bias Network

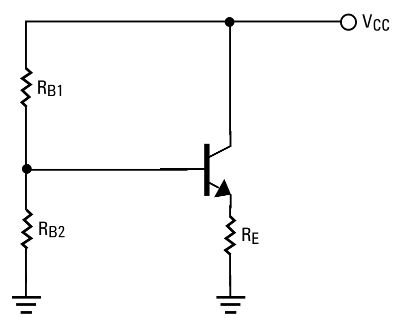


Figure 1E. Circuit #5 – Emitter Feedback BJT Bias Network

device V_{BE} and the desired V_{CE}. Collector resistor R_C has both I_C and I_B flowing through it. The operation of this circuit is best explained as follows. An increase in h_{FE} will tend to cause I_C to increase. An increase in I_C causes the voltage drop across resistor R_C to increase. The increase in voltage across R_C causes V_{CE} to decrease. The decrease in V_{CE} causes I_B to decrease because the potential difference across base bias resistor R_B has decreased. This topology provides a basic form of negative feedback which tends to reduce the amount that the collector current increases as h_{FE} is increased.

Bias circuit #3 has been quite often written up in past literature but predominately when very high V_{CC} (>15 V) and V_{CE} (>12 V) has been used [1]. The voltage divider network consisting of R_{B1} and R_{B2} provides a voltage divider from which resistor R_B is connected. Resistor R_B then determines the base current. I_B times h_{FE} provides I_C. The voltage drop across R_C is determined by the collector current I_C, the bias current I_B, and the current consumed by the voltage divider consisting of R_{B1} and R_{B2}. This circuit provides similar voltage feedback to bias circuit #2.

Bias circuit #4 is similar to bias circuit #3 with the exception that the series current source resistor R_B is omitted. This circuit is seen quite often in bipolar power amplifier design with resistor R_{B2} replaced by a series silicon power diode providing temperature compensation for the bipolar device. The current flowing through resistor R_{B1} is shared by both resistor R_{B2} and the emitter base junction V_{BE}. The greater the current through resistor R_{B2}, the greater the regulation of the emitter base voltage V_{BE}.

Bias circuit #5 is the customary textbook circuit for biasing BJTs. A resistor is used in series with the device emitter lead to provide voltage feedback. This circuit ultimately provides the best control of h_{FE} variations from device to device and over temperature. The only disadvantage of this circuit is that the emitter resistor must be properly bypassed for RF. The typical bypass capacitor quite often has internal lead inductance which can create unwanted regenerative feedback. The feedback quite often creates device instability. Despite the problems associated with using the emitter resistor technique, this biasing scheme generally provides the best control on h_{FE} and over temperature variations.

The sections that follow begin with a discussion of the BJT model and its temperature dependent variables. From the basic model, various equations are developed to predict the device's behavior over h_{FE} and temperature variations. This article is an update to the original article written by Kenneth Richter of Hewlett-Packard [2] and Hewlett-Packard Application Note 944-1 [3].

BJT Modeling

The BJT is modeled as two current sources as shown in Figure 2. The primary current source is h_{FE} I_B. In parallel is a secondary current source I_{CBO} $(1+ h_{FE})$ which describes the leakage current flowing through a reverse biased PN junction. I_{CBO} is typically $1x10^{-7}$ A @ 25°C for an Agilent Technologies HBFP-0405 transistor. V'_{BE} is the internal base emitter voltage with h_{ie} representing the equivalent Hybrid PI input impedance of the transistor. h_{ie} is also equal to $h_{FE} / \lambda I_C$ where $\lambda = 40$ @ +25°C. V_{BE} will be defined as measured between the base and emitter leads of the transistor. It is equivalent to $V'_{BE} + I_B h_{ie}$. V_{BE} is approximately 0.78 V @ 25°C for the HBFP-0405 transistor.

The device parameters that have the greatest change as temperature is varied consist of h_{FE}, V'_{BE}, and I_{CBO}. These temperature dependent variables have characteristics which are process dependent and fairly well understood. h_{FE} typically

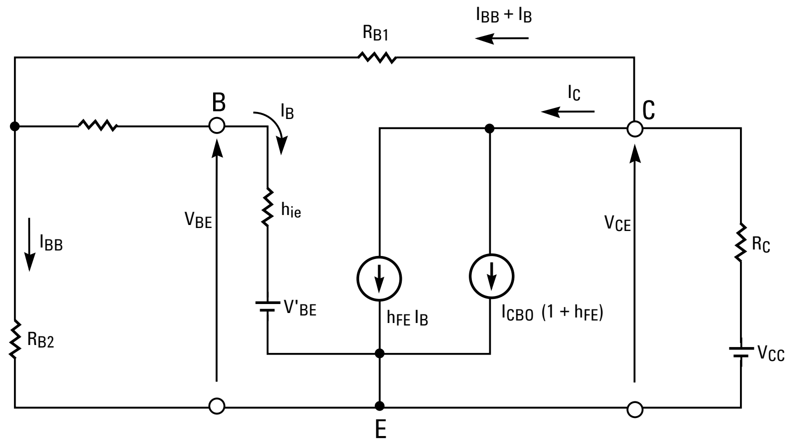


Figure 2. Gummel Poon model of BJT with Voltage Feedback and Constant Base Current Source Network

increases with temperature at the rate of 0.5% / °C. V'_{BE} has a typical negative temperature coefficient of -2 mV / °C. This indicates that V_{BE} decreases 2 mV for every degree increase in temperature. I_{CBO} typically doubles for every 10°C rise in temperature. Each one of these parameters contributes to the net resultant change in collector current as temperature is varied.

For each bias network shown in Figure 1, several sets of simplified circuit equations have been generated to allow calculation of the various bias resistors. These are shown in Figures 3, 4, 5, 6, and 7. Each of the bias resistor values is calculated based on various design parameters such as desired I_C, V_{CE}, power supply voltage V_{CC} and nominal h_{FE}. I_{CBO} and h_{ie} are assumed to be zero for the basic calculation of resistor values.

Additional designer provided information is required for the three circuits that utilize the voltage divider consisting of R_{B1} and R_{B2}. In the case of the bias network that uses voltage feedback with current source, the designer must pick the voltage across R_{B2} (V_{RB2}) and the bias current through resistor R_{B2} which will be termed I_{RB2}.

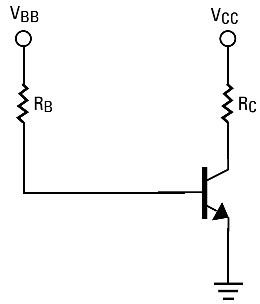
Choose $V_{CE} > V_{RB2} > V_{BE}$

Suggest $V_{RB2} = 1.5$ V

Suggest I_{RB2} to be about 10% of I_C

The voltage feedback with a voltage source network and the emitter feedback network also require that the designer choose I_{RB2}. As will be learned later, the ratio of I_C to I_{RB2} is an important ratio that plays a major part in bias stability.

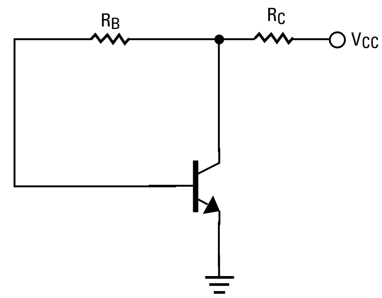
An equation was then developed for each circuit that calculates collector current, I_C, based on nominal bias resistor values and typical device parameters including h_{FE}, I_{CBO}, and V'_{BE}. MATHCAD version 7 was used to help develop the I_C equation. Although the I_C equation starts out rather simply, it develops into a rather lengthy equation for some of the more complicated circuits. MATHCAD helped to simplify the task.



$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$I_C = \frac{h_{FE} \bullet (V_{CC} - V'_{BE})}{h_{ie} + R_B} + I_{CBO} \bullet (1 + h_{FE})$$

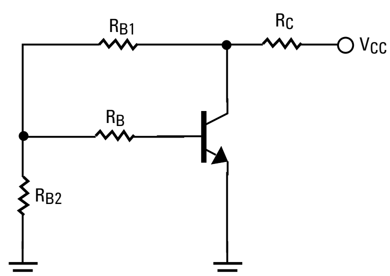
Figure 3. Equations for Non-stabilized Bias Network



$$R_B = \frac{V_{CE} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B}$$

$$I = \frac{h_{FE} \bullet (V_{CC} - V'_{BE}) + I_{CBO} \bullet (1 + h_{FE}) \bullet (h_{ie} + R_B + R_C)}{h_{ie} + R_B + R_C \bullet (1 + h_{FE})}$$

Figure 4. Equations for Voltage Feedback Bias Network



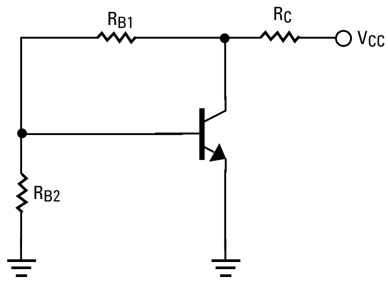
$$R_B = \frac{V_{RB2} - V_{BE}}{I_B} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C + I_{B2} + I_B}$$

$$R_{B1} = \frac{V_{CE} - V_{RB2}}{I_{B2} + I_B} \qquad R_{B2} = \frac{V_{RB2}}{I_{B2}}$$

Designer must choose I_{B2} and V_{RB2} such that $V_{CE} > V_{RB2} > V_{BE}$

$$I_C = \left[\frac{-V'_{BE} \bullet (R_{B1} + R_{B2} + R_C) - R_{B2} \bullet [R_C \bullet I_{CBO} \bullet (1 + h_{FE}) - V_{CC}]}{(R_B + h_{ie}) \bullet (R_{B1} + R_{B2} + R_C) + R_{B2} \bullet (h_{FE} \bullet R_C + R_C + R_{B1})}\right] \bullet h_{FE} + I_{CBO} \bullet (1 + h_{FE})$$

Figure 5. Equations for Voltage Feedback with Current Source Bias Network



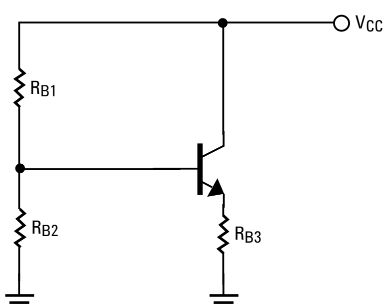
$$R_{B2} = \frac{V_{BE}}{I_{B2}} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B + I_{B2}}$$

$$R_{B1} = \frac{V_{CE} - (I_{B2} \bullet R_{B2})}{I_B + I_{B2}}$$

Designer must choose I_{B2}

$$I_C = \frac{-\left[\frac{-R_C}{h_{FE}} \bullet I_{CBO} - R_C \bullet I_{CBO} + \frac{R_C}{R_{B2}} \bullet V'_{BE} - \frac{R_C}{(R_{B2} \bullet h_{FE})} \bullet h_{ie} \bullet I_{CBO} - \frac{R_C}{R_{B2}} \bullet h_{ie} \bullet I_{CBO} - \frac{R_{B1}}{h_{FE}} \bullet I_{CBO} - R_{B1} \bullet I_{CBO} + \frac{R_{B1}}{R_{B2}} \bullet V'_{BE} - \frac{R_{B1}}{(R_{B2} \bullet h_{FE})} \bullet h_{ie} \bullet I_{CBO} - \frac{R_{B1}}{R_{B2}} \bullet h_{ie} \bullet I_{CBO} + V'_{BE} - \frac{1}{h_{FE}} \bullet h_{ie} \bullet I_{CBO} - h_{ie} \bullet I_{CBO} - V_{CC}\right]}{\left[R_C + \frac{R_C}{h_{FE}} + \frac{R_C}{(R_{B2} \bullet h_{FE})} \bullet h_{ie} + \frac{R_{B1}}{h_{FE}} + \frac{R_{B1}}{(R_{B2} \bullet h_{FE})} \bullet h_{ie} + \frac{1}{h_{FE}} \bullet h_{ie}\right]}$$

Figure 6. Equations for Voltage Feedback with Voltage Source Bias Network



$$R_E = \frac{V_{CC} - V_{CE}}{I_C\left(1 + \frac{1}{h_{FE}}\right)} \qquad R1 = \frac{V_{CC} - I_{B2} \bullet R_2}{I_{B2} + I_B}$$

Pick I_{B2} to be 10% of I_C

$$R_2 = \frac{V_{RB2}}{I_{B2}} \qquad V_{RB2} = V'_{BE} + (I_B + I_C) \bullet R_E$$

$$I_C = \frac{-\left[V'_{BE} - \frac{1}{h_{FE}} \bullet h_{ie} \bullet I_{CBO} - h_{ie} \bullet I_{CBO} - \frac{R_E}{h_{FE}} \bullet I_{CBO} - R_E \bullet I_{CBO} + \frac{R_1}{R_2} \bullet V'_{BE} - \frac{R_1}{(R_2 \bullet h_{FE})} \bullet h_{ie} \bullet I_{CBO} - \frac{R_1}{R_2} \bullet h_{ie} \bullet I_{CBO} - \frac{R_1}{R_2} \bullet \frac{R_E}{h_{FE}} \bullet I_{CBO} - \frac{R_1}{R_2} \bullet R_E \bullet I_{CBO} - \frac{R_1}{h_{FE}} \bullet I_{CBO} - R_1 \bullet I_{CBO} - V_{CC}\right]}{\left[\frac{1}{h_{FE}} \bullet h_{ie} + \frac{R_E}{h_{FE}} + R_E + \frac{R_1}{(R_2 \bullet h_{FE})} \bullet h_{ie} + \frac{R_1}{R_2} \bullet \frac{R_E}{h_{FE}} + \frac{R_1}{R_2} \bullet R_E + \frac{R_1}{h_{FE}}\right]}$$

Figure 7. Equations for Emitter Feedback Bias Network

Design example using the Agilent HBFP-0405 BJT

The HBFP-0405 transistor will be used as a test example for each of the bias circuits. The Agilent HBFP-0405 is described in an application note [4] as a low noise amplifier for 1800 to 1900 MHz applications. The HBFP-0405 will be biased at a V_{CE} of 2.7 Volts and a drain current I_C of 5 mA. A power supply voltage of 3 volts will be assumed. The nominal h_{FE} of the HBFP-0405 is 80. The minimum is 50 while the maximum is 150. The calculated bias resistor values for each bias circuit are described in Table 1.

With the established resistor values, I_C is calculated based on minimum and maximum h_{FE}. The performance of each bias circuit with respect to h_{FE} variation is shown in Table 2. Bias circuit #1 clearly has no compensation for varying h_{FE} allowing I_C to increase 85% as h_{FE} is taken to its maximum. Circuit #2 with very simple collector feedback offers considerable compensation due to h_{FE} variations allowing an increase of only 42%. Surprisingly, circuit #3 offers very little improvement over circuit #2. Circuit #4 provides considerable improvement in h_{FE} control by only allowing a 9% increase in I_C. Circuit #4 offers an improvement over the previous circuits by providing a stiffer voltage source across the base emitter junction. As will be shown later, this circuit has worse performance over temperature as compared to circuits #2 and #3. However, when both h_{FE} and temperature are considered, circuit #4 will appear to be the best performer for a grounded emitter configuration. As expected, circuit #5 provides the best control on I_C with varying h_{FE} allowing only a 5.4% increase in I_C. Results are very much power supply dependent and with higher V_{CC}, results may vary significantly.

Table 1. Bias resistor values for HBFP-0405 biased at V_{CE} = 2 V, V_{CC} = 2.7 V, I_C = 5 mA, h_{FE} = 80 for the various bias networks

Resistor	Non-stabilized Bias Network	Voltage Feedback Bias Network	Voltage Feedback w/Current Source Bias Network	Voltage Feedback w/Voltage Source Bias Network	Emitter Feedback Bias Network
R_C	140 Ω	138 Ω	126 Ω	126 Ω	
R_B	30770 Ω	19552 Ω	11539 Ω		
R_{B1}			889 Ω	2169 Ω	2169 Ω
R_{B2}			3000 Ω	1560 Ω	2960 Ω
R_E					138 Ω

Table 2. Summary of I_C variation vs. h_{FE} for various bias networks for the HBFP-0405 V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA, T_J = +25°C

Bias Circuit	Non-stabilized Bias Network	Voltage Feedback Bias Network	Voltage Feedback w/Current Source Bias Network	Voltage Feedback w/Voltage Source Bias Network	Emitter Feedback Bias Network
I_C (mA) @ minimum h_{FE}	3.14	3.63	3.66	4.53	4.70
I_C (mA) @ typical h_{FE}	5.0	5.0	5.0	5.0	5.0
I_C (mA) @ maximum h_{FE}	9.27	7.09	6.98	5.44	5.27
Percentage change in I_C from nominal I_C	+85% -37%	+42% -27%	+40% -27%	+9% -9%	+5.4% -6%

BJT Performance over Temperature

Since all three temperature dependent variables (I_{CBO}, h_{FE}, and V'_{BE}) exist in the I_C equation, then differentiating the I_C equation with respect to each of the parameters provides insight into their effect on I_C. The partial derivative of each of the three parameters represents a stability factor. The various stability factors and their calculation are shown in Table 3. Each circuit then has three distinctly different stability factors which are then multiplied times a corresponding change in either V'_{BE}, h_{FE}, or I_{CBO} and then summed. These changes or deltas in V'_{BE}, h_{FE}, and I_{CBO} are calculated based on variations in these parameters due to manufacturing processes.

A comparison of each circuit's stability factors will certainly provide insight as to which circuit compensates best for each parameter. MATHCAD was again pushed into service to calculate the partial derivatives for each desired stability factor. The stability factors for each circuit are shown in Table 4.

The change in collector current from the nominal design value at 25°C is then calculated by taking each stability factor and multiplying it times the corresponding change in each parameter. Each product is then summed to determine the absolute change in collector current.

As an example, the collector current of the HBFP-0405 will be analyzed as temperature is increased from +25°C to +65°C. For the HBFP-0405, I_{CBO} is typically 100 nA @ +25°C and typically doubles for every 10°C temperature rise. Therefore, I_{CBO} will increase from 100 nA to 1600 nA at +65°C. The difference or ΔI_{CBO} will be 1600 - 100 = 1500 nA. The 1500 nA will then be multiplied times its corresponding I_{CBO} Stability factor.

V'_{BE} @ 25°C was measured at 0.755 V for the HBFP-0405. Since V'_{BE} has a typical negative temperature coefficient of -2 mV / °C, V'_{BE} will be 0.675 V @ +65°C. The difference in V'_{BE} will then be 0.675 - 0.755 = -0.08 V. The -0.08 V will then be multiplied times its corresponding V'_{BE} stability factor.

h_{FE} is typically 80 @ +25°C and typically increases at a rate of 0.5% / °C. Therefore, h_{FE} will increase from 80 to 96 @ +65°C making Δh_{FE} equal to 96 - 80 = 16. Again the Δ is multiplied times its corresponding stability factor.

Once all stability terms are known, they can be summed to give the resultant change in collector current from the nominal value at +25°C. The results of the stability analysis are shown in Table 5. The non-stabilized circuit #1 allows I_C to increase about 27% while circuits 2 and 3 show a 19 to 20% increase in I_C. Somewhat surprising is the fact that circuit #4 shows a nearly 30% increase in I_C with temperature. In looking at the contribution of the individual stability factors for circuit #4, one finds that V'_{BE} is the major contributor. This is probably due to the impedance of the R_{B1} and R_{B2} voltage divider working against V'_{BE}. It is also interesting

Table 3. Calculation of the Stability Factors and their combined effect on I_C

$I_{CBO} = \dfrac{\partial I_C}{\partial I_{CBO}} \quad h_{FE}, V'_{BE} = \text{constant}$	First calculate the stability factors for V'_{BE}, I_{CBO}, and h_{FE}. Then, to find the change in collector current at any temperature, multiply the change from 25°C of each temperature dependent variable with its corresponding stability factor and sum.
$V'_{BE} = \dfrac{\partial I_C}{\partial V'_{BE}} \quad I_{CBO}, h_{FE} = \text{constant}$	
$h_{FE} = \dfrac{\partial I_C}{\partial h_{FE}} \quad I_{CBO}, V'_{BE} = \text{constant}$	
$\Delta I_C = SI_{CBO} \bullet \Delta I_{CBO} + SV'_{BE} \bullet \Delta V'_{BE} + Sh_{FE} \bullet \Delta h_{FE}$	

to note that both circuit #2 and #3 have very similar performance over temperature. Both offer a significant improvement over circuit #1 and #4. As expected, circuit #5 offers the best performance over temperature by nature of emitter feedback. Emitter feedback can be used effectively if the resistor can be adequately RF bypassed without producing stability problems.

The degree of control that each bias circuit has on controlling I_C due to h_{FE} variations and the intrinsic temperature dependent parameters has a lot to due with how the bias circuit is designed. Increasing the voltage differential between V_{CE} and V_{CC} can enhance the circuits' ability to control I_C. In handset applications, this becomes difficult with 3 volt batteries as power sources. The current that is allowed to flow through the various bias resistors can also have a major effect on I_C control.

In order to analyze the various configurations, an AppCAD module was generated. AppCAD was created by Bob Myers of the Agilent Technologies WSD Applications Department and is available free of charge via the Agilent web site. AppCAD consists of various modules developed to help the RF designer with microstrip, stripline, detector, PIN diode, MMIC biasing, RF amplifier, transistor biasing and system level calculations, just to name a few. The AppCAD BJT biasing module allows the designer to fine tune each bias circuit design for optimum performance. AppCAD also allows the designer to input device variation parameters peculiar to a certain manufacturer's semiconductor process. A sample screen showing a typical bias circuit is shown in Figure 8. The data from AppCAD is used to create the graphs in the following sections.

The first exercise is to graphically show the percentage change in I_C versus h_{FE}. AppCAD is used to calculate the resistor values for each of the five bias networks. The HBFP-0405 transistor is biased at a V_{CE} of 2 V, I_C of 5 mA, and V_{CC} of 2.7 V. Various values of h_{FE} are substituted into AppCAD. The results are shown in Figure 9. The data clearly shows that the Emitter Feedback and Voltage Feedback with Voltage Source networks are superior to the remaining circuits with regards to controlling h_{FE} at room temperature. These networks provide a 4:1 improvement over the other two Voltage Feedback networks.

AppCAD is then used to simulate a temperature change from T_J = -25°C to +65°C holding h_{FE} constant. Whereas the original Matchcad analysis assumed that $T_C = T_J$, AppCAD takes into account that T_J is greater than T_C. AppCAD calculates the thermal rise based on dc power dissipated and the thermal impedance of the device. The results of the analysis are shown in Figure 10. Somewhat surprising was the fact that the Voltage Feedback with Voltage Source network performed nearly as poorly as the non-stabilized circuit. This is due to V_{BE} decreasing with temperature and the bias circuit trying to keep V_{BE} constant. This is why power bipolar designers will utilize a silicon diode in place of R_{B2} so that the bias voltage will track the V_{BE} of the transistor. Depending on the impedance of the voltage divider network, V_{BE} could actually rise causing I_C to increase. The Emitter Feedback network performed very well as expected. The simple Voltage Feedback network appeared to be optimum when one considers the simplicity of the circuit.

Bias networks 3 through 5 make use of an additional resistor that shunts some of the total power supply current to ground. Properly chosen, this additional bias current can be used to assist in controlling I_C over temperature and h_{FE} variations from device to device. AppCAD is set up such that the designer can make a few decisions regarding the amount of bias resistor current that is allowed to flow from the power supply. AppCAD is again used to analyze each bias circuit.

The graphs in Figures 11 and 12 plot the percentage change in I_C versus the ratio of I_C to I_{RB1}. I_{RB1} is the current flowing through resistor RB1 which is the summation of base current I_B and current flowing through resistor RB2. The maximum permissible ratio of I_C to I_{RB1} is limited by the h_{FE} of the transistor. Figure 11 represents the worst case condition where I_C increases at maximum h_{FE} and highest temperature. Figure 12 shows the opposite scenario where lowest I_C results from lowest h_{FE} and lowest temperature. The percentage change is certainly more pronounced at high h_{FE} and high temperature.

Some of the actual predicted results are somewhat surprising. However, as expected, the bias network with emitter resistor feedback offers the best performance overall. For a ratio of I_C to I_{RB1} of 10 to 1 or less, the resultant change in collector current is less than 20%. The Voltage Feedback with Voltage Source network provides its best

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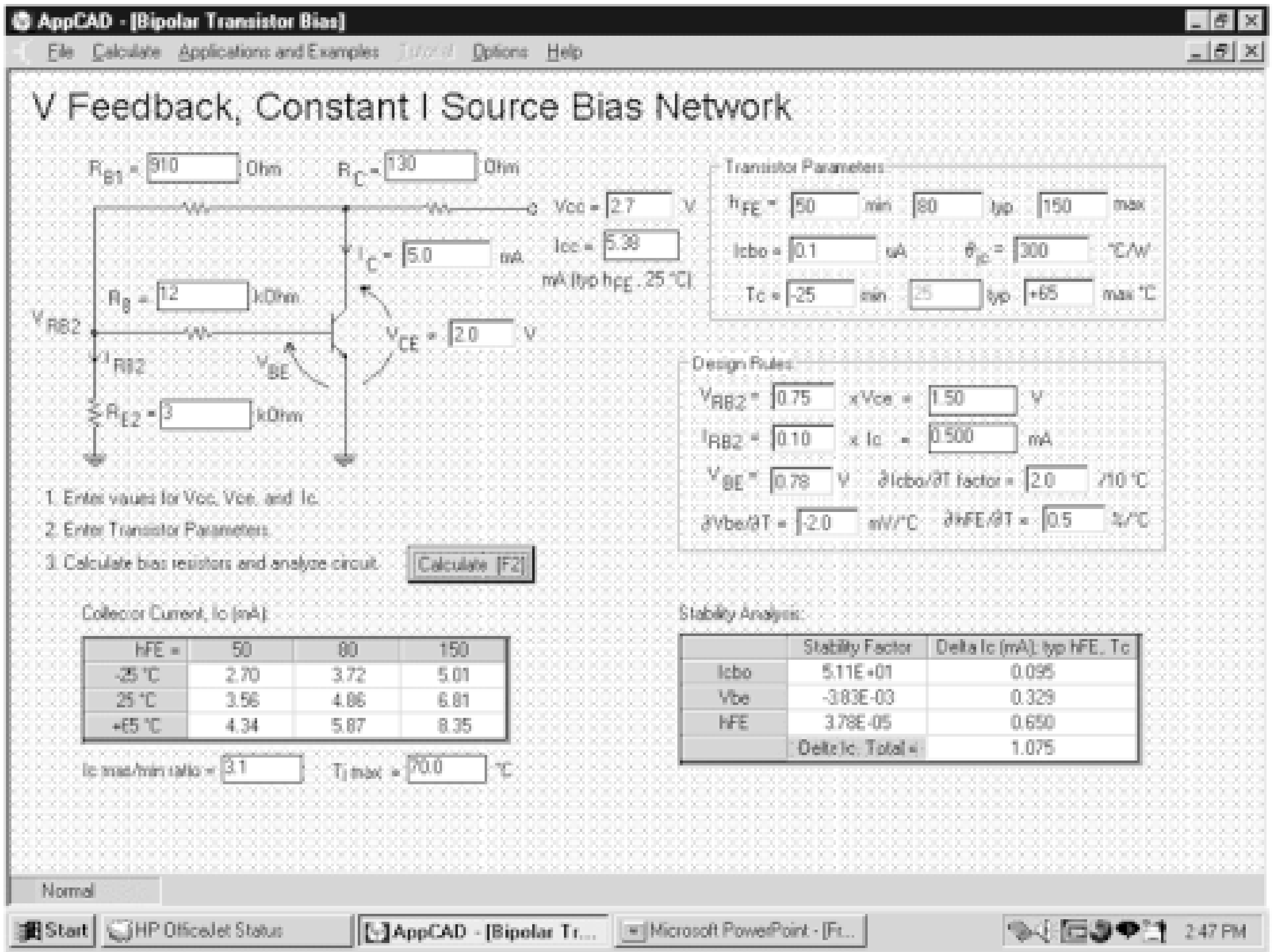

Figure 8. Agilent Technologies' AppCAD module for BJT Biasing

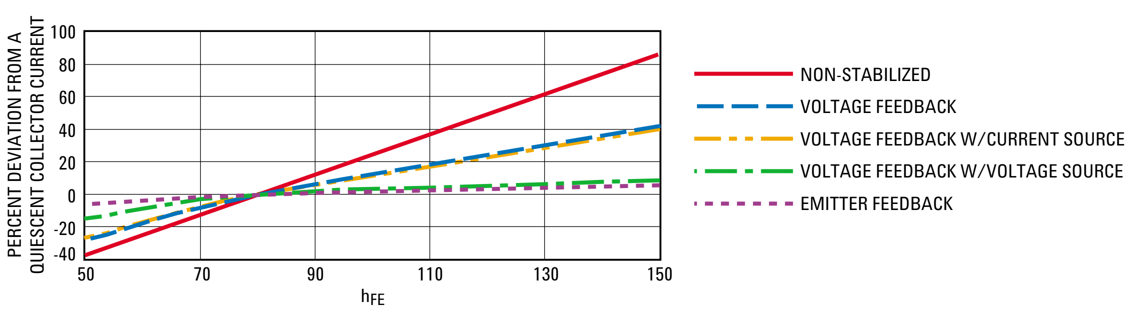

Figure 9. Percent Change in Quiescent Collector Current vs. h_{FE} for the HBFP-0405

V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA, T_J = +25°C

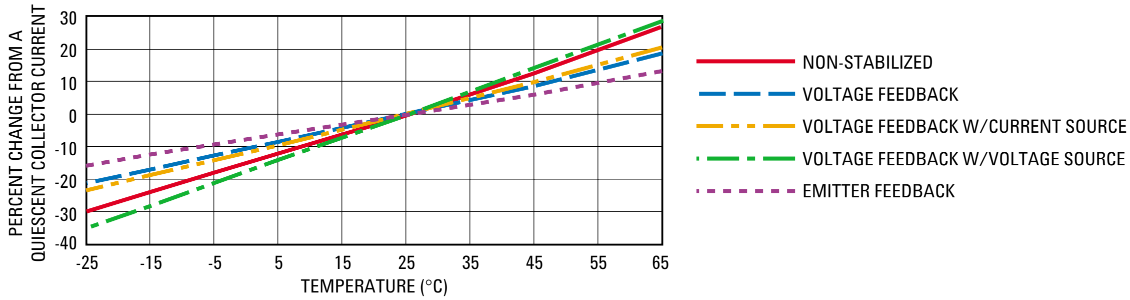

Figure 10. Percent Change in Quiescent Collector Current vs. Temperature for the HBFP-0405

V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA, T_J = +25°C

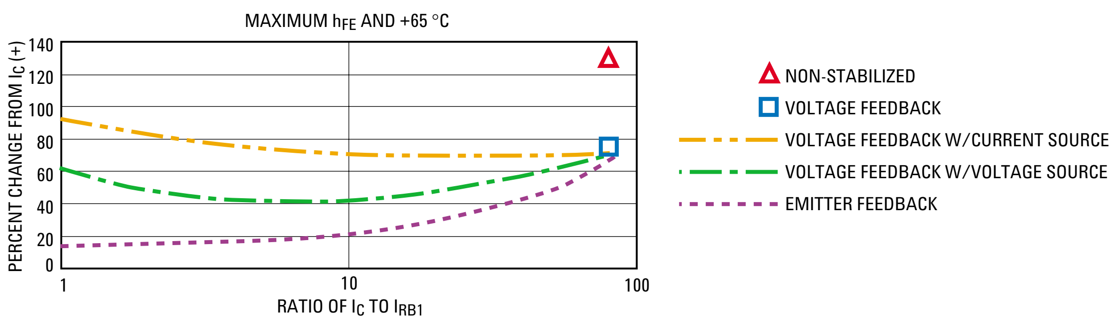

Figure 11. Percent Change in Quiescent Collector Current vs. Ratio of I_C to I_{RB1} for Maximum h_{FE} and +65°C for the HBFP-0405

V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA, T_J = +25°C

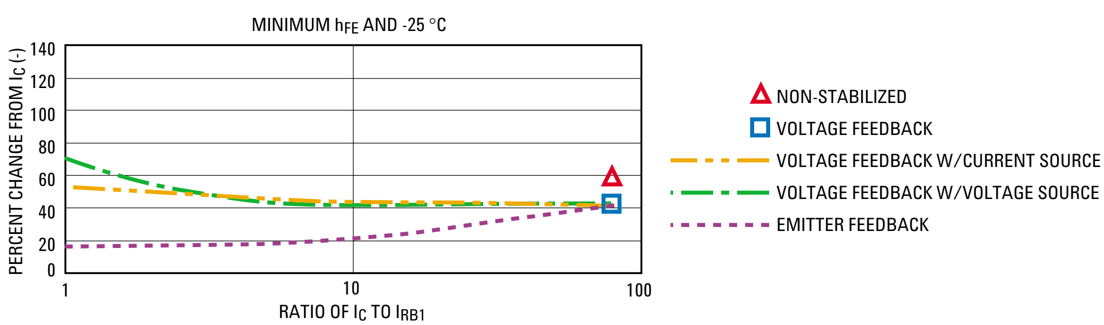

Figure 12. Percent Change in Quiescent Collector Current vs. Ratio of I_C to I_{RB1} for Minimum h_{FE} and T_J = -25°C for the HBFP-0405

V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA

Table 4.
Stability Factors for Non-stabilized Bias Network #1

Collector current at any temperature (I_C)	$\dfrac{h_{FE} \bullet (V_{CC} - V'_{BE})}{(h_{ie} + R_B)} + I_{CBO} \bullet (1 + h_{FE})$
I_{CBO} Stability factor $I_{CBO} = \dfrac{\partial I_C}{\partial I_{CBO}} \Big\vert h_{FE}, V'_{BE} = \text{Constant}$	$1 + h_{FE}$
V'_{BE} Stability factor $V'_{BE} = \dfrac{\partial I_C}{\partial V'_{BE}} \Big\vert I_{CBO}, h_{FE} = \text{Constant}$	$\dfrac{-h_{FE}}{h_{ie} + R_B}$
h_{FE} Stability factor $h_{FE} = \dfrac{\partial I_C}{\partial h_{FE}} \Big\vert I_{CBO}, V'_{BE} = \text{Constant}$	$\dfrac{V_{CC} - V'_{BE}}{h_{ie} + R_B} + I_{CBO}$

Table 4.
Stability Factors for Voltage Feedback Bias Network #2

Collector current at any temperature (I_C)	$\dfrac{h_{FE} \bullet (V_{CC} - V'_{BE}) + I_{CBO} \bullet (1 + h_{FE}) \bullet A}{h_{ie} + R_B + R_C \bullet (1 + h_{FE})}$
I_{CBO} Stability factor $I_{CBO} = \dfrac{\partial I_C}{\partial I_{CBO}} \Big\vert h_{FE}, V'_{BE} = \text{constant}$	$\dfrac{(1 + h_{FE}) \bullet A}{h_{ie} + R_B + R_C \bullet (1 + h_{FE})}$
V'_{BE} Stability factor $V'_{BE} = \dfrac{\partial I_C}{\partial V'_{BE}} \Big\vert I_{CBO}, h_{FE} = \text{constant}$	$\dfrac{-h_{FE}}{h_{ie} + R_B + R_C \bullet (1 + h_{FE})}$
h_{FE} Stability factor $h_{FE} = \dfrac{\partial I_C}{\partial h_{FE}} \Big\vert I_{CBO}, V'_{BE} = \text{constant}$	$\dfrac{V_{CC} - V'_{BE} + A \bullet I_{CBO}}{h_{FE} \bullet R_C + R_B + h_{ie} + R_C} -$ $\dfrac{R_C \bullet h_{FE} \bullet (V_{CC} - V'_{BE} + A \bullet I_{CBO}) + A \bullet I_{CBO}}{(h_{FE} \bullet R_C + R_B + h_{ie} + R_C)^2}$ Where: $A = h_{ie} + R_B + R_C$

Table 4.
Stability Factors for Voltage Feedback with Current Source Bias Network #3

Collector current at any temperature (I_C)	$h_{FE}\left[\frac{-V'_{BE} \bullet A - R_{B2} \bullet [R_C \bullet I_{CBO} \bullet (1 + h_{FE}) - V_{CC}]}{(R_B + h_{ie}) \bullet A + R_{B2} \bullet (h_{FE} \bullet R_C + R_C + R_{B1})}\right] + I_{CBO} \bullet (1 + h_{FE})$
I_{CBO} Stability factor $I_{CBO} = \frac{\partial I_C}{\partial I_{CBO}} \vert h_{FE}, V'_{BE} = \text{constant}$	$(1 + h_{FE}) - \frac{R_{B2} \bullet h_{FE} \bullet R_C \bullet (1 + h_{FE})}{A \bullet (R_B + h_{ie}) + R_{B2} \bullet (h_{FE} \bullet R_C + R_C + R_{B1})}$
V'_{BE} Stability factor $V'_{BE} = \frac{\partial I_C}{\partial V'_{BE}} \vert I_{CBO}, h_{FE} = \text{constant}$	$\frac{-h_{FE} \bullet A}{(R_B + h_{ie}) \bullet A + R_{B2} \bullet (h_{FE} \bullet R_C + R_C + R_{B1})}$
h_{FE} Stability factor $h_{FE} = \frac{\partial I_C}{\partial h_{FE}} \vert I_{CBO}, V'_{BE} = \text{constant}$	$\frac{h_{FE} \bullet \left\{R_{B2} \bullet R_C \bullet \left[(-R_{B2} \bullet V_{CC} + B) + R_{B2} \bullet R_C \bullet I_{CBO} \bullet (1 + h_{FE})\right]\right\}}{D^2} - \left[\frac{B + R_{B2} \bullet \left[R_C \bullet I_{CBO} \bullet (1 + h_{FE}) - V_{CC} + h_{FE} \bullet R_C \bullet I_{CBO}\right]}{D}\right] + I_{CBO}$ Where: $A = R_{B1} + R_{B2} + R_C$ $B = V'_{BE} \bullet (R_{B1} + R_{B2} + R_C)$ $C = (R_B + h_{ie}) \bullet (R_{B1} + R_{B2} + R_C)$ $D = (R_B + h_{ie}) \bullet (R_{B1} + R_{B2} + R_C) + R_{B2} \bullet (h_{FE} \bullet R_C + R_C + R_{B1})$

Table 4.
Stability Factors for Voltage Feedback with Voltage Source Bias Network #4

Collector current at any temperature (I_C)	$\dfrac{I_{CBO} \bullet (-A) + I_{CBO} \bullet h_{ie} \bullet (-B) + D - V_{CC}}{C}$
I_{CBO} Stability factor $I_{CBO} = \dfrac{\partial I_C}{\partial I_{CBO}} \Big\vert h_{FE}, V'_{BE} = \text{constant}$	$\dfrac{h_{ie} \bullet B + A}{C}$
V'_{BE} Stability factor $V'_{BE} = \dfrac{\partial I_C}{\partial V'_{BE}} \Big\vert I_{CBO}, h_{FE} = \text{constant}$	$\dfrac{\dfrac{-R_C}{R_{B2}} - \dfrac{R_{B1}}{R_{B2}} - 1}{C}$
h_{FE} Stability factor $h_{FE} = \dfrac{\partial I_C}{\partial h_{FE}} \Big\vert I_{CBO}, V'_{BE} = \text{constant}$	$\dfrac{I_{CBO} \bullet \left[\dfrac{-R_C}{h_{FE}^2} - \dfrac{R_{B1}}{h_{FE}^2}\right] + I_{CBO} \bullet h_{ie} \bullet E}{C} -$ $\dfrac{I_{CBO} \bullet A + I_{CBO} \bullet h_{ie} \bullet B - D + V_{CC}}{C^2} \bullet \left[\dfrac{-R_C}{h_{FE}^2} - \dfrac{R_{B1}}{h_{FE}^2} + h_{ie} \bullet E\right]$ Where: $A = \dfrac{R_C}{h_{FE}} + R_C + \dfrac{R_{B1}}{h_{FE}} + R_{B1}$ $B = \dfrac{R_C}{R_{B2} \bullet h_{FE}} + \dfrac{R_C}{R_{B2}} + \dfrac{R_{B1}}{R_{B2} \bullet h_{FE}} + \dfrac{R_{B1}}{R_{B2}} + \dfrac{1}{h_{FE}} + 1$ $C = R_C + \dfrac{R_C}{h_{FE}} + \dfrac{R_{B1}}{h_{FE}} + h_{ie} \bullet \left[\dfrac{R_C}{R_{B2} \bullet h_{FE}} + \dfrac{R_{B1}}{R_{B2} \bullet h_{FE}} + \dfrac{1}{h_{FE}}\right]$ $D = \dfrac{R_C}{R_{B2}} \bullet V'_{BE} + \dfrac{R_{B1}}{R_{B2}} \bullet V'_{BE} + V'_{BE}$ $E = \dfrac{-R_C}{R_{B2} \bullet h_{FE}^2} - \dfrac{R_{B1}}{R_{B2} \bullet h_{FE}^2} - \dfrac{1}{h_{FE}^2}$

Table 4.
Stability Factors for Emitter Feedback Bias Network #5

Collector current at any temperature (I_C)	$\frac{h_{ie} \bullet I_{CBO} \bullet (-A) + I_{CBO} \bullet (-B) + D}{C}$
I_{CBO} Stability factor $I_{CBO} = \frac{\partial I_C}{\partial I_{CBO}} \|_{h_{FE}, V'_{BE}} = \text{constant}$	$\frac{h_{ie} \bullet A + B}{C}$
V'_{BE} Stability factor $V'_{BE} = \frac{\partial I_C}{\partial V'_{BE}} \|_{I_{CBO}, h_{FE}} = \text{constant}$	$\frac{-1 - \frac{R_1}{R_2}}{C}$
h_{FE} Stability factor $h_{FE} = \frac{\partial I_C}{\partial h_{FE}} \|_{I_{CBO}, V'_{BE}} = \text{constant}$	$\frac{I_{CBO} \bullet E + h_{ie} \bullet I_{CBO} \bullet \left[\frac{-1}{h_{FE}^2} - \frac{R_1}{R_2 \bullet h_{FE}^2}\right]}{C} - \frac{I_{CBO} \bullet B + h_{ie} \bullet I_{CBO} \bullet A - D}{C^2} \bullet \left[h_{ie} \bullet \left(\frac{-1}{h_{FE}^2} - \frac{R_1}{R_2 \bullet h_{FE}^2}\right) + E\right]$ Where: $A = \frac{R_1}{R_2 \bullet h_{FE}} + \frac{R_1}{R_2} + \frac{1}{h_{FE}} + 1$ $B = \frac{R_1}{R_2} \bullet \frac{R_E}{h_{FE}} + \frac{R_1}{R_2} \bullet R_E + \frac{R_E}{h_{FE}} + R_E + \frac{R_1}{h_{FE}} + R_1$ $C = h_{ie} \bullet \left(\frac{1}{h_{FE}} + \frac{R_1}{R_2 \bullet h_{FE}}\right) + \frac{R_E}{h_{FE}} + R_E + \frac{R_1}{R_2} \bullet \frac{R_E}{h_{FE}} + \frac{R_1}{R_2} \bullet R_E + \frac{R_1}{h_{FE}}$ $D = V'_{BE} + \frac{R_1}{R_2} \bullet V'_{BE} - V_{CC}$ $E = \frac{-R_E}{h_{FE}^2} - \frac{R_1}{R_2} \bullet \frac{R_E}{h_{FE}^2} - \frac{R_1}{h_{FE}^2}$

Table 5. Bias Stability Analysis at +65°C using the HBFP-0405
V_{CC} = 2.7 V, V_{CE} = 2 V, I_C = 5 mA

Bias Circuit	#1 Non-Stabilized	#2 Voltage Feedback	#3 Voltage Feedback w/Current Source	#4 Voltage Feedback	#5 Emitter Feedback
I_{CBO} Stability Factor	81	52.238	50.865	19.929	11.286
V'_{BE} Stability Factor	-2.56653×10^{-3}	-2.568011×10^{-3}	-3.956×10^{-3}	-0.015	-6.224378×10^{-3}
h_{FE} Stability Factor	6.249877×10^{-5}	4.031×10^{-5}	3.924702×10^{-5}	1.537669×10^{-5}	8.707988×10^{-6}
ΔI_C due to I_{CBO} (mA)	0.120	0.078	0.076	0.030	0.017
ΔI_C due to V'_{BE} (mA)	0.210	0.205	0.316	1.200	0.497
ΔI_C due to h_{FE} (mA)	0.999	0.645	0.628	0.246	0.140
Total ΔI_C (mA)	1.329	0.928	1.020	1.476	0.654
Percentage change in I_C from nominal I_C	26.6%	18.6%	20.4%	29.5%	13.1%

performance at an I_C to I_{RB1} ratio between 6 and 10 with a worst case change of 41% in collector current.

To complete the comparison, two additional points representing the Non-Stabilized and the Voltage Feedback networks have been added to the graphs. They are shown as single points because only the base current is in addition to the collector current. The Non-stabilized network has a +129% change while the Voltage Feedback network has an increase of 74.5%. It is also interesting to note that the Voltage Feedback with Current Source network really offers no benefit over the simpler Voltage Feedback network.

Conclusion

This paper has presented the circuit analysis of four commonly used stabilized bias networks and one non-stabilized bias network for the bipolar junction transistor. In addition to the presentation of the basic design equations for the bias resistors for each network, an equation was presented for collector current in terms of bias resistors and device parameters. The collector current equation was then differentiated with respect to the three primary temperature dependent variables resulting in three stability factors for each network. These stability factors plus the basic collector current equation give the designer insight as to how best bias any bipolar transistor for best performance over h_{FE} and temperature variations. The basic equations were then integrated into an AppCAD module providing the circuit designer an easy and effective way to analyze bias networks for bipolar transistors.

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1. “A Cost-Effective Amplifier Design Approach at 425 MHz Using the HXTR-3101 Silicon Bipolar Transistor”, Hewlett-Packard Application Note 980, 2/81 (out of print).

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3. “Microwave Transistor Bias Considerations”, Hewlett-Packard Application Note 944-1, 8/80, (out of print).

4. “1800 to 1900 MHz Amplifier using the HBFP-0405 and HBFP-0420 Low Noise Silicon Bipolar Transistors”, Hewlett-Packard Application Note 1160, (11/98), publication number 5968-2387E.

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