Vertical InGaAs/InP Tunnel FETs With Tunneling Normal to the Gate

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Abstract—Vertical n-channel tunnel field-effect transistors (TFETs) based on compound semiconductors, in a new geometry with tunneling normal to the gate, are demonstrated for the first time using an n+ In0.53Ga0.47As/n+ In0.53−xGaAs/p+ InP heterojunction. At 300 K, the TFETs show an on-current of \( \sim 20 \mu A/\mu m \) and a minimum subthreshold swing (SS) of 130 mV/dec using an Al2O3 gate dielectric (\( EOT \sim 3.4 \) nm). Postdeposition annealing of the gate dielectric improves SS, and device passivation using atomic layer deposition can effectively prevent degradation of drain current over time. The clear negative device passivation using atomic layer deposition, and the trend toward NDR in the TFETs confirm that the transport mechanism in these TFETs is interband tunneling.

Index Terms—Heterojunction, indium gallium arsenide, indium phosphide, MOSFETs, nanoelectronics, subthreshold swing (SS), transistors, tunnel field-effect transistor (TFET), tunneling.

I. INTRODUCTION

Tunnel field-effect transistors (TFETs) are under intense investigation for low-power applications because of their potential for low subthreshold swing (SS) and low off-state leakage (\( I_{OFF} \)) [1]. III–V semiconductors with small effective mass and staggered or broken energy band alignments promise high on-current and \( I_{ON}/I_{OFF} \) ratios [2]–[5]. However, how to best configure compound semiconductor TFETs is still an open question due to various constraints in material quality and processing issues. Experimental demonstrations of III–V TFETs have been recently reported employing side gates [6]–[8]. In these reports, the tunneling direction is parallel to the semiconductor–gate interface. Here, we experimentally investigate a new III–V TFET geometry in which the tunneling direction is normal to the gate [9], [10]. This geometry offers an increase in tunneling cross section to enable high \( I_{ON} \) [11]–[13] while offering a lower SS because of the uniform onset of tunneling across the junction [11]. To this end, we successfully developed a gate-first vertical TFET process with a planar gate [12]. In this letter, we report the device performance of vertical n-channel TFETs with passivation using this process, which are fabricated on an n+ In0.53Ga0.47As/n+ In0.53−xGaAs/p+ InP heterojunction. This heterostructure was adopted in this proof-of-concept study due to the relative maturity of InGaAs/InP growth and the availability of highly selective etches between arsenides and phosphides. An \( I_{ON}/I_{OFF} \) ratio of \( 10^4 \) and an \( I_{ON} \) of \( \sim 20 \mu A/\mu m \) with an SS of 130 mV/dec at 300 K and a supply voltage \( V_{DD} \) of 1 V have been achieved. Also investigated are the effects of postdeposition annealing (PDA) of the Al2O3 gate oxide, passivation of etched undercuts and mesas by atomic layer deposition (ALD) oxides, and temperature dependence of device characteristics. Tunnel diodes were also fabricated from the same heterostructure to explore the intrinsic transport in this strained tunnel junction.

II. DEVICE STRUCTURE AND FABRICATION

The n-channel TFET structure (the inset in Fig. 1) was grown by molecular beam epitaxy by IntelliEPI, Richardson, TX, on a p+ InP substrate (Zn \( \sim 1.7 \times 10^{18} \) cm\(^{-3} \)). The device structure, starting from the substrate, consists of a 300-nm p+ InP buffer (Be, \( 5 \times 10^{18} \) cm\(^{-3} \)) and a 12-nm p+ InP source injector (Be, \( 1.2 \times 10^{19} \) cm\(^{-3} \)), followed by 6 nm of n+ InxGa1−xAs, with the In composition \( x \) graded from 1.0 to 0.53, and 9 nm of n+ In0.53Ga0.47As with a 5-nm InP cap layer. Both n+ layers are Si doped to a concentration of \( 1 \times 10^{19} \) cm\(^{-3} \).

Device fabrication started with ALD of a 7-nm-thick Al2O3 gate dielectric (\( EOT \sim 3.4 \) nm) right after removing the InP cap layer in 1HCl : 1H2O. A 3-min 350 °C PDA by rapid thermal annealing in N\(_2\) was applied to one sample in a split-wafer experiment. After blanket deposition of a TiW gate stack and SiN\(_x\) hard mask, the devices were patterned using optical lithography and reactive-ion etching (RIE) with device gates aligned parallel to the [001] and [010] directions. Plasma-enhanced chemical vapor deposition SiN\(_x\) sidewalls were then formed around the gate stack by blanket deposition and anisotropic dry etch, followed by removal of the Al2O3 gate dielectric in the drain contact region using AZ 400K developer as a selective wet etchant. After Ti/Au source metallization (on the back of the wafer) and lift-off of the drain metallization (Ti/Au), the graded InGaAs-to-InAs layer was selectively

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etched in 1H₂SO₄ : 8H₂O₂ : 160H₂O to stop at the p⁺ InP source. The SiNₓ on the gate was then removed by RIE to expose the gate metal (Ti/W), followed by a highly selective InP etch (1HCl:3H₃PO₄) until the InP under the drain and the SiNₓ spacer was removed to form an undercut mesa structure. Finally, the device was passivated with 7 nm of Al₂O₃ and 3 nm of HfO₂ using ALD at 300 °C.

III. RESULTS AND DISCUSSION

Fig. 1 shows a cross-sectional scanning electron micrograph (SEM) of a fabricated vertical TFET, confirming that the tunnel junctions are fully overlapped by the gate electrode. Consequently, the current modulation observed in these TFETs is expected to be entirely due to the gate control. Also shown are the band diagrams under the gate of the vertical TFET. For a given quasi-Fermi level separation (qV_DS) in n-InGaAs and p⁺ InP under reverse bias (V_DS > 0 in TFETs), the conduction band edge of InGaAs is expected to sweep with V_DS from below (on state, band-to-band tunneling allowed) to above the valence band edge (off state) of p⁺ InP. Electrons are collected at the self-aligned drain contact. In this letter, we focus on the first experimental demonstration of this novel TFET.

The drain current in a TFET common-source I–V characteristic results from gate modulation of the Zener tunneling current of the reverse-biased tunnel junction at the source. In order to confirm that band-to-band tunneling is the dominant transport, the I_D–V_DS characteristics at 77 K were measured [Fig. 2(a)]. With the tunnel junction under forward bias (V_DS < 0), an unambiguous trend toward the negative differential resistance (NDR) is observed as the gate bias is increased. Observation of NDR in the TFETs is precluded by the high drain parasitic access resistance present due to unoptimized processing. To gain additional insight, the temperature-dependent I–V characteristics of the tunnel diodes fabricated on the same epitaxial structure were also measured, shown in Fig. 2(b). NDR is distinctly observed under negative V_DS, i.e., forward bias for the p⁺ InP/n⁺ InGaAs tunnel junction. Both the peak and valley currents vary with temperature, with a trend that the current increases with increasing temperature. This leads to a reduced peak-to-valley current ratio at higher temperatures. These observations indicate that the band-to-band tunneling governs the operation of the device.

Fig. 3 shows the measured common-source I_D–V_GS transfer characteristics at 300 K of an n-TFET with PDA and without passivation. Normalized by a gate width of 80 μm, the on-current of 20 μA/μm at V_DS = V_GS = 1 V is comparable to that reported in p⁺-i-n⁺ InGaAs TFETs [6], [8] with tunneling parallel to the gate and at approximately the same bias condition, despite the use of a wide-bandgap InP source, an effective tunneling distance in the ON state of approximately 4 nm [see Fig. 1(b)], and a parasitic access resistance of higher than 13 kΩ·μm. The off-current minimum at V_GS = −1 V is likely due to ambipolar current flow, where holes can be induced in the channel at high negative gate voltages and then initiate an interband tunnel current between the channel and the drain. This explanation is consistent with the bias dependence of the off-current at V_GS = −1 V; however, it is not possible to rule out that defect-assisted tunneling [15] is also contributing to this minimum current. The drain current on/off ratio is ∼10³, while the gate leakage is at least two orders of magnitude smaller than the device channel current over the measured bias range. Fig. 3(b) plots the tangential SS as a function of the gate current. Minimum SS (SS_min) values of 160, 137, and 130 mV/dec were obtained at V_DS = 0.2, 0.5, and 1 V, respectively.
increases the drain access resistance in the areas of etch undercut, thus degrading \( I_{ON} \). Surface oxidation at the tunnel junction sidewall may also introduce midgap states, thus degrading \( SS \). It was observed that devices without passivation exhibited a decrease in drain current over the course of several days after fabrication [Fig. 4(a)]. For the TFET in Fig. 4(a), the drain current decreased by more than two orders of magnitude. On the other hand, it was found that the performance of TFETs with passivation showed no detectable changes over a period of several weeks [Fig. 4(b)]. This indicates that ALD oxide passivation can effectively prevent degradation.

Fig. 5.(a) \( I_{D} - V_{GS} \) showing improved SS in TFETs with PDA. (b) Temperature-dependent \( I_{D} - V_{GS} \) characteristics of a TFET with PDA and passivation. At \( V_{DS} = 0.5 \) V, the minimum point SS \( SS_{\text{min}} \) decreased from 240 mV/dec to 140 mV/dec at 77 K.

IV. CONCLUSION

A new geometry for TFETs with tunneling normal to the gate has been demonstrated experimentally for the first time. Field control of interband tunneling is confirmed by comparison of temperature-dependent measurements. The need for surface passivation of the drain access region and improved SS with PDA is also shown.

REFERENCES