Name: _____

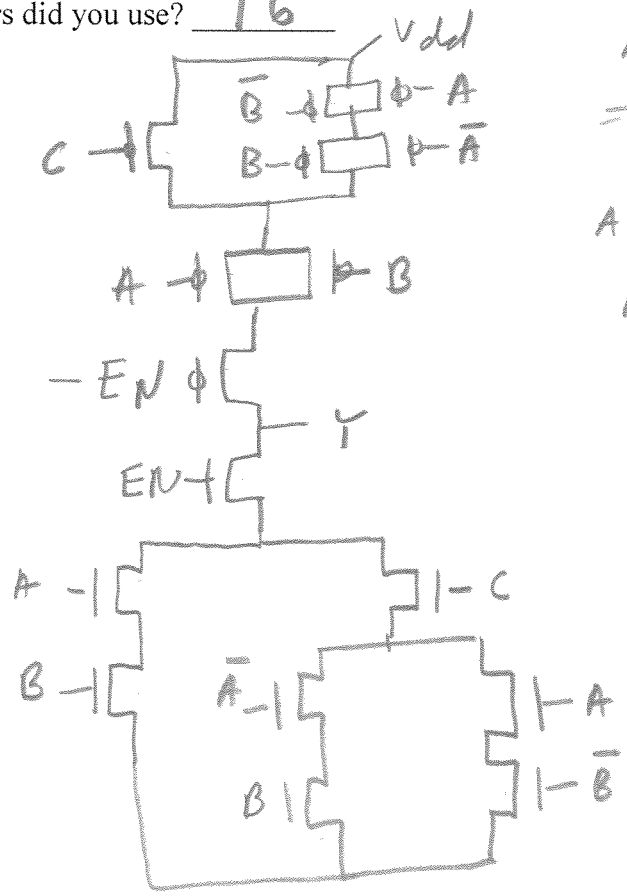
I acknowledge this exam has been taken under all aspects of the ND Honor Code.

CSE 462 VLSI Design: Exam #1
Sept. 24, 2015

Problem	Max Points	Points Off
1	20	
2	20	
3	20	
4	20	
5	20	
6	20	
7	20	
Total	140	

- SIGN YOUR NAME!!!!!!
- This is a take-home exam due back on Tuesday Sept. 29, 2015 no later than 3:15pm to my office 326a Fitzpatrick. You may leave it with Joyce Yeats in the office in 326. ***NO EXCEPTIONS***.
- Open book and notes, but no computer searches, cell phones, or communications with or help from others. The use of a computer for calculations or access to the course web site is allowed. **All** other aspects of the ND Honor code apply.
- Do ***all*** problems.
- Show all you work in the spaces supplied, including equations that you may have used
- Show units on your final answers to numerical questions.
- If you have questions, email me at kogge@cse.nd.edu and I will try to email class the question and answer.

1. (20pt) Draw a transistor diagram for a tri-state enabled gate. When EN is high, the output Y is not(AB + C(A xor B)); when EN is low, the output is "undefined." You may assume the negation of each input signal A, B, C, and EN is available if you need it.
   - How many transistors did you use? 16



$$\overline{AB + C(A \text{ xor } B)}$$

$$= \overline{AB + C(A\bar{B} + \bar{A}B)}$$

ALTERNATIVE

A	B	C	
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

yields

$$\overline{AB + C(A+B)}$$

Name _____

2. (20 pts.) Fill in the best answer for each statement.

1.25mA (2pt) What is the current through a 4K resistor connected to a 5V supply.

10ns (2p) What is the time constant for a 2K resistor in series with a 5pF ($5*10^{-12}$)

b, c (2pt) What happens as we lengthen the channel of a FET (indicate all that may happen) (a) Idsat goes up, (b) Idsat goes down, (c) the gate's capacitance goes up, (d) the gate's capacitance goes down, (e) nothing changes

a, c (2pt) What happens as we lengthen the width of a FET (indicate all that may happen) (a) Idsat goes up, (b) Idsat goes down, (c) the gate's capacitance goes up, (d) the gate's capacitance goes down, (e) nothing changes

b (2 pts) How does the mobility of the carriers for an N vs P type compare? (a) the same, (b) N is normally greater than P, (c) N is normally less than P, (d) it depends.

a, c (2 pts) Which ones of the following effects reduces the peak saturation current: (a)velocity saturation, (b) channel length modulation, (c) body effects, (d) none of the above.

increases V_T

remember $\beta = k \frac{W}{L}$

a, b (2 pts) The minimum feature size is most directly related to: (a) the Numerical Aperture, NA, of the projection lens, (b) the wavelength of the light used to print the line, λ, (c) the cost of the equipment, (d) the size of the wafer.

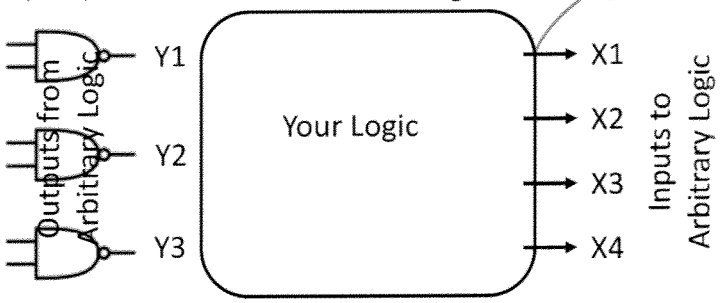
3X (2pt) Assume a transistor with a β of x, what would its β be if you tripled its width?

c (2 pts) Assume we have a CMOS invertor with a peak saturation current for the N type of 200ua, and the P type of 400ua, what do you think of the ratio of the rise to fall times? (a) about equal, (b) the fall is 2 times faster, (c) the rise is 2 time faster, (d) the fall is 4 times faster, (e) the rise is 4 times faster (f) can't tell.

c (2pts) A "Self-Aligned" process refers to (a) a process where each mask has alignment marks to prior masks, (b) the transistor's gate gets fabricated after the source and drain diffusion regions and automatically aligned between the two, (c) the transistor's gate is created first and the source and drain created around them, (d) metal vias are aligned with the contacts on the die's surface by etching through them.

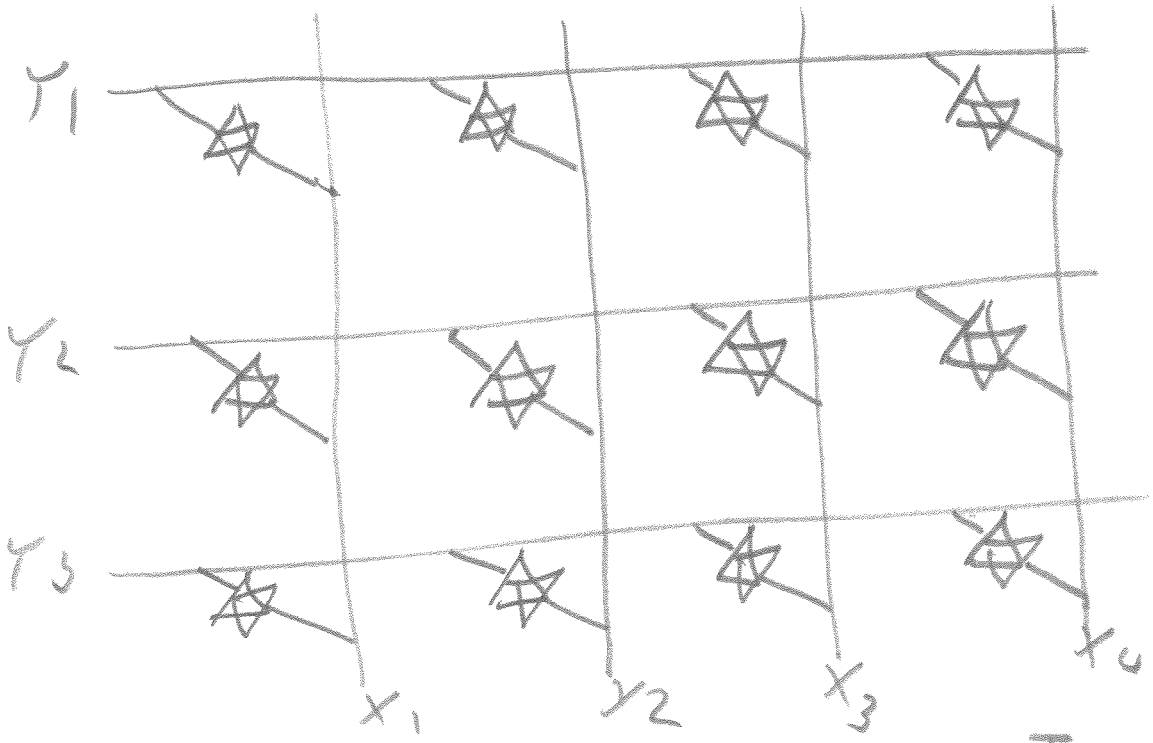
Name _____

3. (20 pt) Consider a circuit where we have 3 outputs Y1, Y2, and Y3 from one set of logic and 4 inputs to other logic gates X1, X2, X3, and X4.



- (10pt) Draw a circuit ***<u>using transmission gates</u>*** that allows any output to be routed to any input. Use some naming convention to label the control signals for the transmission gates. Assume the negation of all control signals is available. How many transistors do you need? 24
- (5pt) Using your naming convention, indicate the value of the control signals needed to connect Y1 to *<u>both</u>* X1 and X3, Y2 to X2, and Y3 to X3.
- (5pt) What would you change if you wanted OR(Y2, Y3) to go to X3 instead of just Y3. (Be clever – can you do this without adding any more logic, just changing control signals).

a)



C_{xy} is control signal for T gate connecting row x to column y

b) Set all C_{xy}'s To 0 but: $C_{11} = C_{13} = C_{22} = C_{33} = 1$

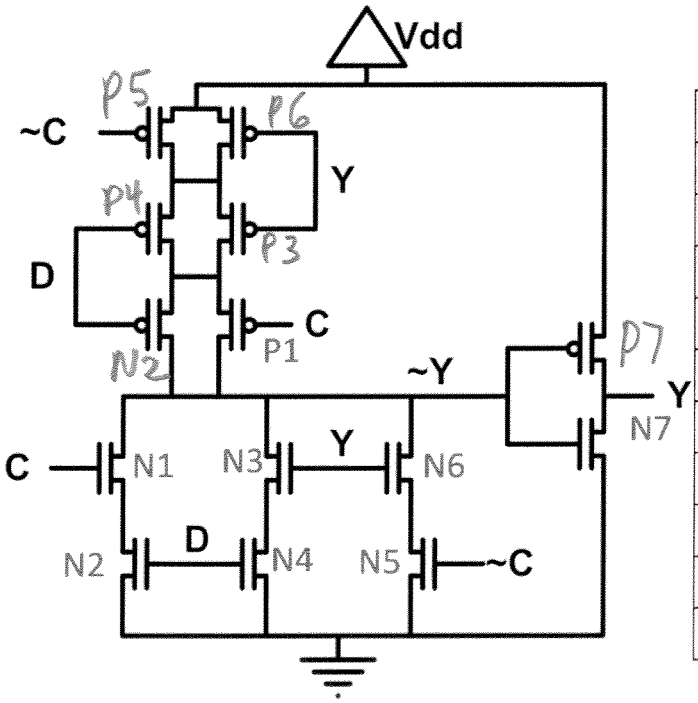
c) Also set C_{23} To 1

Name _____

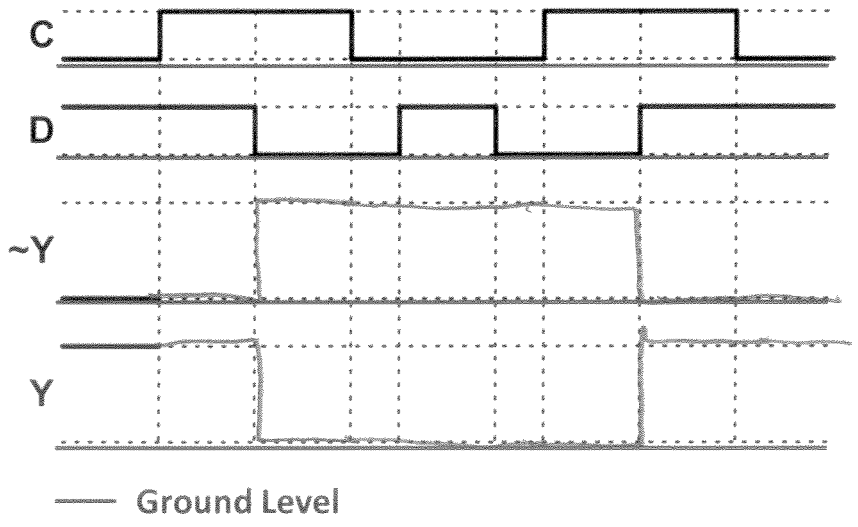
4. (20 pts) Consider the following two-level circuit. "~C" is the complement of C. Note that the output Y goes back to inputs at the first level. Note the naming of the N-type transistors as N1, … N7
   a) Label the P-types in terms of which one is "the complement" of the matching N-type (eg P1 vs N1)
   b) Fill in the table as follows: **"X" if transistor Ni is ON** (Leave blank if off), also **"1" or "0" for ~Y**
   c) What is the function on wire ~Y (Express as a function of C, D, and Y, and their complements)?

CD + DY + YC

   d) Under what conditions does Y NOT change as D changes? C=0
   e) Under what conditions can Y change as D changes? C=1
   f) Complete the timing diagram for the output Y with the given D, C, and initial Y. Pay attention to what happens as an input (C or D) changes; assume that Y changes slowly, so that if the logic computing ~Y changes ~Y, that change is stable before Y changes.

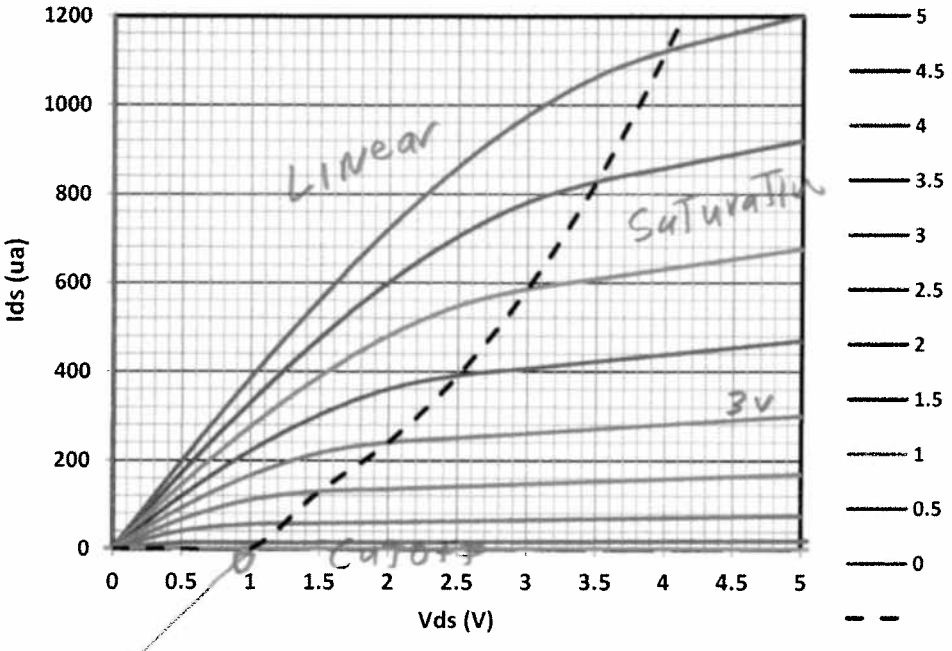


C	0	1	0	1	0	1	0	1
D	0	0	1	1	0	0	1	1
Y	0	0	0	0	1	1	1	1
N1		X		X	X	X	X	X
N2			X	X			X	X
N3		X		X	X	X	X	X
N4			X	X			X	X
N5	X	X	X	X	X		X	
N6		X		X	X	X	X	X
N7	X		X	X	X	X	X	X
~Y	1	1	1	0	0	1	0	0



Name _____

5. (20 pts) The plot below shows an NMOS transistor IV characteristics. The body is connected to the source, ***there is channel modulation***, but no velocity saturation effect. The table below has I_d values from the plot so you do not have to interpret those points on the curves. Also the dashed line is a curve representing the transition between the linear region and the saturation region.



Ids		Vds					
		0	1	2	3	4	5
Vgs	5	0	385	720	975	1120	1200
	4	0	275	480	585	630	675
	3	0	165	240	260	280	300
	2	0	55	60	65	70	75

Hint: Use the Shockley equations combined with the equation for channel length modulation. In calculating the parameters from the table, use one region of operation and try holding one independent variable constant (Vgs or Vds) and varying the other variable to get several equations and then simplify such as taking ratios. Label the points that you use and show your calculations to get partial or full credit.

a) (3pt) Label the regions of the graph.

b) (2 pts) What is the equation for I_d in the saturation region for *this* transistor? $I_d = \frac{\beta}{2}(V_{gs} - V_T)^2(1+\lambda V_{ds})$

c) (10pt) Compute β, V_t, and λ (channel length modulation factor). Hint: you may want to compute λ first. Show how you derived them. (Note: the numbers for this figure were chosen to make calculations simple).

$V_T = 1.0V$

Choose one V_{gs} voltage - say 3V
+ 2 V_{ds} points in saturated region, say 3 + 4V

For $V_{ds} = 3V$, $\beta/2(3-1)^2(1+\lambda 3) = 260\mu A$

For $V_{ds} = 4V$ $\beta/2(3-1)^2(1+\lambda 4) = 280\mu A$

or $\beta(1+\lambda 3) = \frac{260\times 2}{4} = 130$

+ $\beta(1+\lambda 4) = \frac{280\times 2}{4} = 140$

TAKE RATIO $\frac{1+\lambda 3}{1+\lambda 4} = \frac{130}{140}$

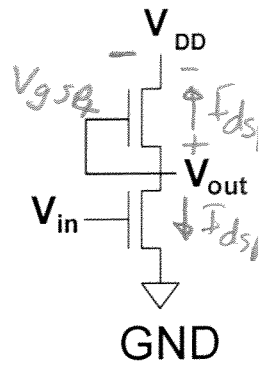
or $140 + 420\lambda = 130 + 520\lambda$

$10 = 100\lambda \Rightarrow \lambda = 0.1$

now
$\beta(1+.1\times 3) = 130$
$\beta(1.3) = 130$
$\beta = \frac{130}{1.3} = 100$

Name _____

6. (20pt) Consider the circuit below where the P-type transistor has its gate connected to its drain (i.e. the same as the output of the inverter and the drain of the N-type). In this case, the P-type is always "on," and functions much like a (non-linear) resistor pullup in an NMOS-like inverter. The characteristics of each transistor are on the next page. Do the following:



a) (1pt) Write an equation for the relationship between V_{dsp} and V_{out}: $V_{DD} + V_{dsp} = V_{OUT}$ or $V_{DSP} = V_{out} - V_{dd}$

b) (1pt) Write an equation for V_{gsp} $V_{gsp} = V_{out} - V_{dd}$

c) (1pt) Write an equation for the relationship between I_{dsn} and I_{dsp} $I_{dsp} = -I_{dsN}$

d) (3pt) Using the figure for the P-type device, fill in the table below for columns V_{dsp}, V_{gsp}, I_{dsp}, and I_{dsn}.

e) (5pt) On the figure for the N-type, use the table's points computed above to draw the equivalent of a load line as presented by the P-type (Circle points corresponding to your table to make it easy for me to grade).

f) (5pt) Now using this load line, fill in the last column of the table with the values of V_{out} as a function of Vin.

g) (1pt) What is the minimum V_{out} value that this inverter puts out? 1V

h) (2pt) If that value were fed into a second inverter of the same design, what would be V_{out}? 5

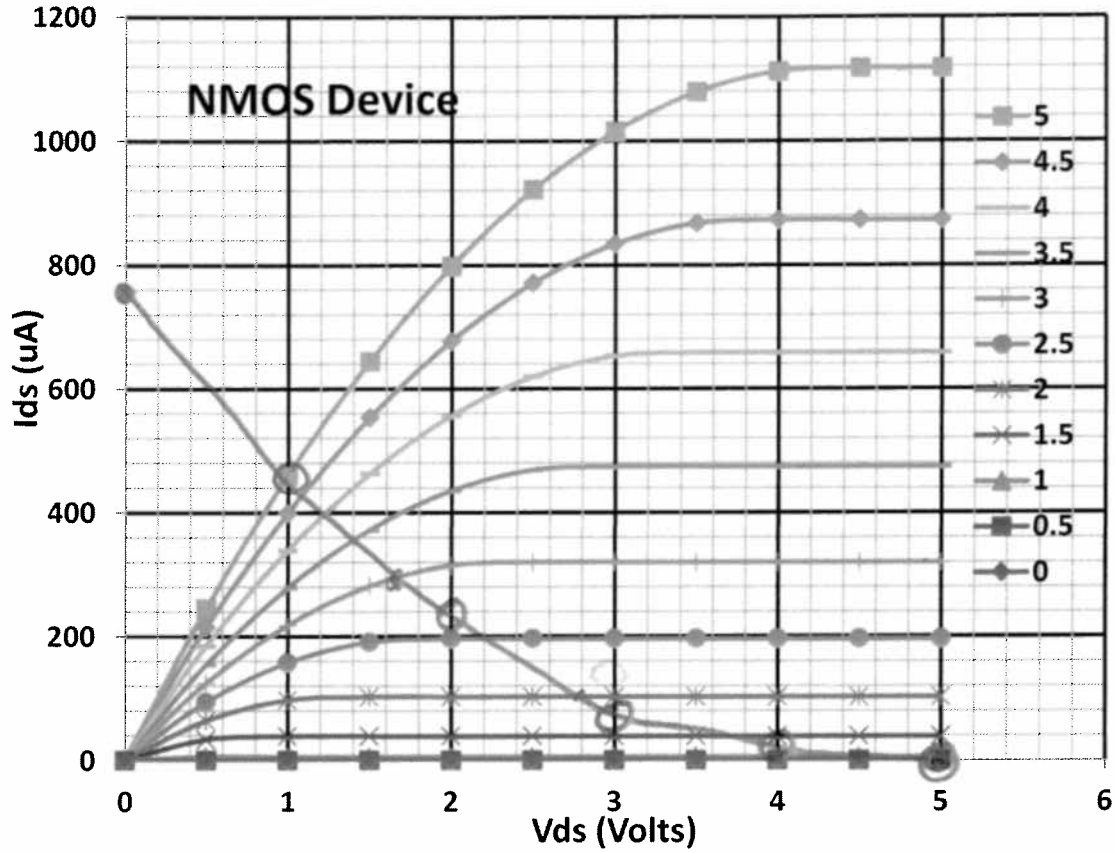
i) (1pt) What is the static power drawn by this gate if $V_{in} = V_{dd} = 5V$. 5V × 450μa = 2.25 mw

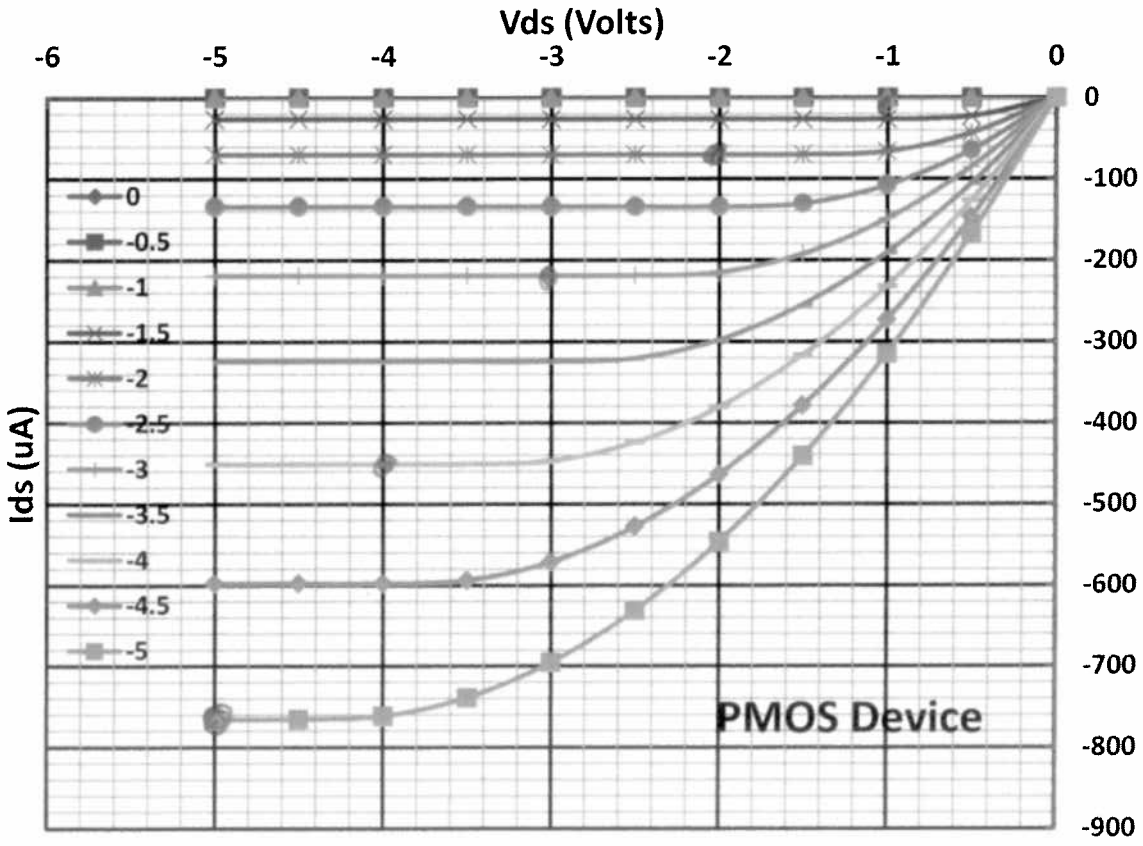
$V_{out} = V_{dsN}$	V_{dsp}	V_{gsp}	I_{dsp}		V_{in}	V_{out}
5V	0	0	0	0	5V	1
4V	-1	-1	-10	10	4V	1.2
3V	-2	-2	-70	70	3V	1.6
2V	-3	-3	-220	220	2V	2.8
1V	-4	-4	-450	450	1V	4-5
0	-5	-5	-760	760	0	5

add I_{dsp}

Note: yes, several of these answers are trivial.

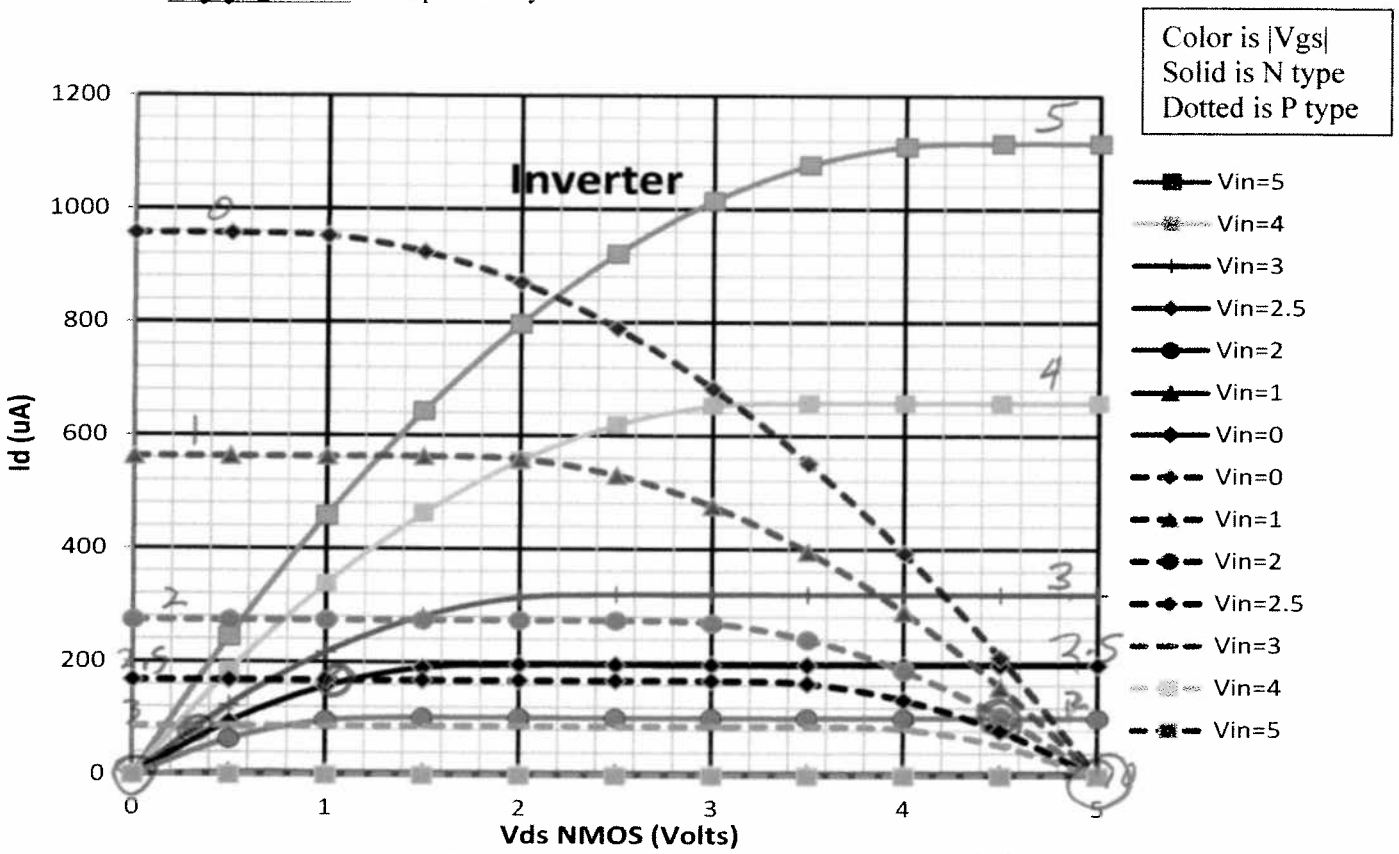
Name _____


NMOS Device
Ids (uA)
Vds (Volts)
1200
1000
800
600
400
200
0
0
1
2
3
4
5
6
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0


Vds (Volts)
Ids (uA)
PMOS Device
-6
-5
-4
-3
-2
-1
0
0
-100
-200
-300
-400
-500
-600
-700
-800
-900
0
-0.5
-1
-1.5
-2
-2.5
-3
-3.5
-4
-4.5
-5

Name _____

7. (20pt) Consider a CMOS inverter from the AMI 0.6um process where the P type is 2.5X wider than the N type. The following is an overlay of the N and P type IVs from the spreadsheet.
   a) (5pt) Fill in the Vout vs Vin characteristics. (Circle the points on the graph you used to get these)
   b) (5pt) Fill in the table of Ids vs Vin characteristics
   c) (4pt) What is the value of β_p in terms of β_n? _____
   d) (3pt) What is the max current? 160 uA
   e) (3pt) Estimate the value of Vin that represents the dividing point between a "1" and a "0" ~2.2 V Explain why.



Vin	Vout	Ids
0	5	0
1	5	0
2	4.5	100
2.5	1	160
~~5~~		
3	.4	80
4	0	0
5	0	0

$\beta_p = \frac{960}{1120}\beta_n = .857 = \frac{6}{7}$