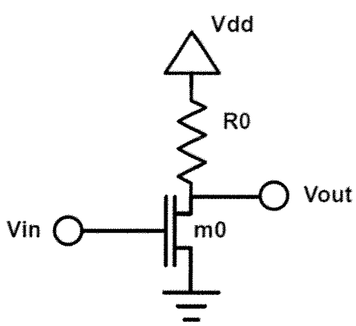
CSE 40462/CSE 60462/EE 40462/EE 60462
VLSI Design

Note that solutions to odd problems as stated in the W&H book are available at http://www.cmosvlsi.com/solutionsodd.pdf.

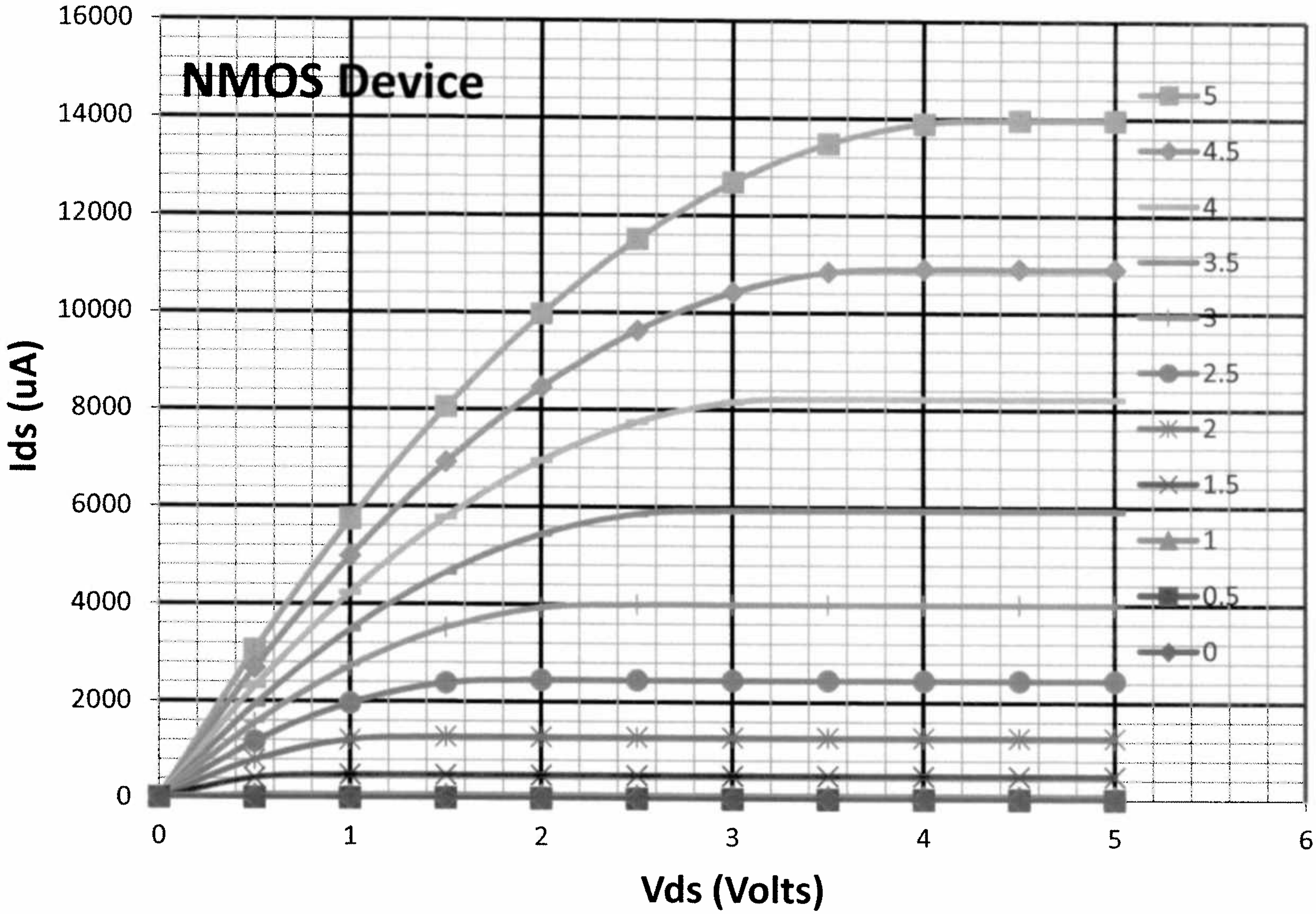
1. For a 0.5 µm process NMOS transistor: W = 5 µm, L = 0.5 µm, tox = 8 nm, and the electron mobility is 350 cm^2/Vs. The threshold voltage is 0.7 V. Plot I_D vs. V_{DS} for V_{GS} = 0, 1, 2, 3, 4 and 5V. (This is similar to W&H problem 2.1.) (You might try Excel for this.)
2. W&H problem 2.2.
3. W&H problem 2.4.
4. Repeat W&H 2.4 using a gate dielectric of HfO_2 which has a relative permittivity, !r, of 25, and a dielectric thickness of 5 nm. (Hafnium dioxide is one of several new high permittivity gate dielectrics being used in sub-90 nm processes to increase gate thickness.)
5. Consider the following circuit:

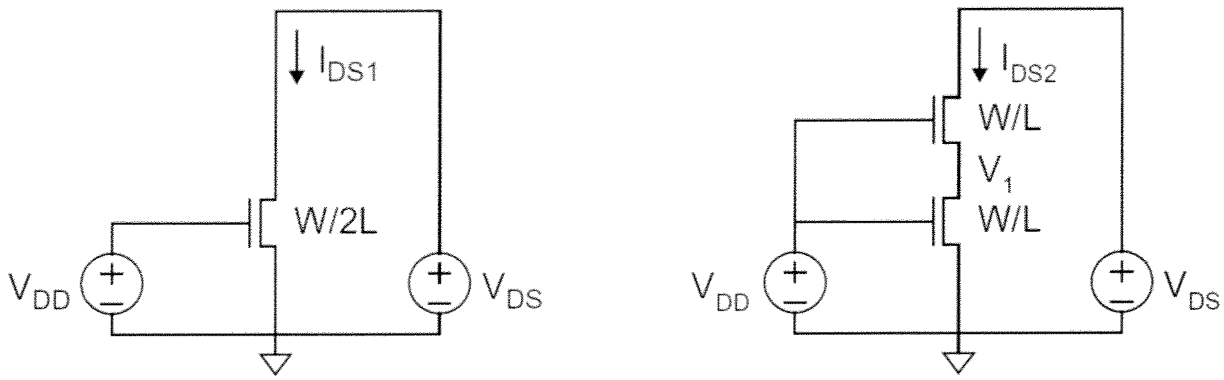


Assume that transistor m0 has characteristics of the 0.18 microns CMOS transistor shown in class, i.e. L = 0.18 microns W = 1 micron and Vdd = 1.8 V. (The class notes will be on the class web site so you can print additional copies of the transistor characteristics.) R0 is a 3.6 kohms resistor.

a. Plot Vout versus Vin.
b. Plot I_D versus Vin.
c. At what Vin is the peak current?
d. What is the minimum output voltage?

This uses 8 nm = 80 Å





(a) (b)

2.2 In (a), the transistor sees V_{gs} = V_{DD} and $V_{ds} = V_{DS}$. The current is

$$I_{DS1} = \frac{\beta}{2}\left(V_{DD} - V_t - \frac{V_{DS}}{2}\right)V_{DS}$$

(a)s transistor is 2X length of (b)s. Thus β(a) is ½ β(b)

In (b), the bottom transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_1$. The top transistor sees $V_{gs} = V_{DD} - V_1$ and $V_{ds} = V_{DS} - V_1$. The currents are

$$I_{DS2} = \beta\left(V_{DD} - V_t - \frac{V_1}{2}\right)V_1 = \beta\left((V_{DD} - V_1) - V_t - \frac{(V_{DS} - V_1)}{2}\right)(V_{DS} - V_1)$$

Bottom Transistor   Top Transistor

get this far for 90%

Solving for V_1, we find

$$V_1 = (V_{DD} - V_t) - \sqrt{(V_{DD} - V_t)^2 - \left(V_{DD} - V_t - \frac{V_{DS}}{2}\right)V_{DS}}$$

Substituting V_1 indo the I_{DS2} equation and simplifying gives $I_{DS1} = I_{DS2}$.

Note: V1 != VDS/2, even when VDD = VDS (KEY QUESTION – WHY????)

Examples for 65nm tech:

VDD	1	VDD	1.3
VDS	1	VDS	1
Vt	0.3	Vt	0.3
V1	0.161484	V1	0.292893
IDS1/Beta	0.1	IDS1/Beta	0.25
IDS2Lower/Beta	0.1	IDS2Lower/Beta	0.25
IDSUpper/Beta	0.1	IDSUpper/Beta	0.25

$C = \varepsilon_r \varepsilon_0 L/t_{ox} W$

-"per micron" is per μ of width $= \varepsilon_r \varepsilon_0 L/t_{ox}$

2.3, 2.4 H&W 2.2

$C_{permicron} = \varepsilon_r \varepsilon_0 L/t_{ox}$

Remember the units!

$e_0 = 8.85\times10^{-14}$ F/cm

$10A^{\circ} = 1nm = 0.001um$

$1fF = 10^{-15}F$

	2.3	2.4
L	90	90 nm
tox	1.6	5 nm
permittivity	3.9	25
Cpermicron	1.94E-15	3.98E-15 F/micron
Cpermicron	1.94	3.98 fF/micron
e0	8.85E-14 F/cm	

$= 8.85E^{-18}$ F/μm

~~$3.9 \times 8.85\times10^{-14}$ F/cm $\times 90\times10^{-7}$ cm / $16A = 1.6nm = 1.6\times10^{-7}$ cm~~

Need to place L and t_{ox} in same units so they cancel & e_0 in F/μ or fF/μ is more typical

#2 $3.9 \times 8.85E^{-18}$ F/μm $\times \frac{90nm}{1.6nm}$

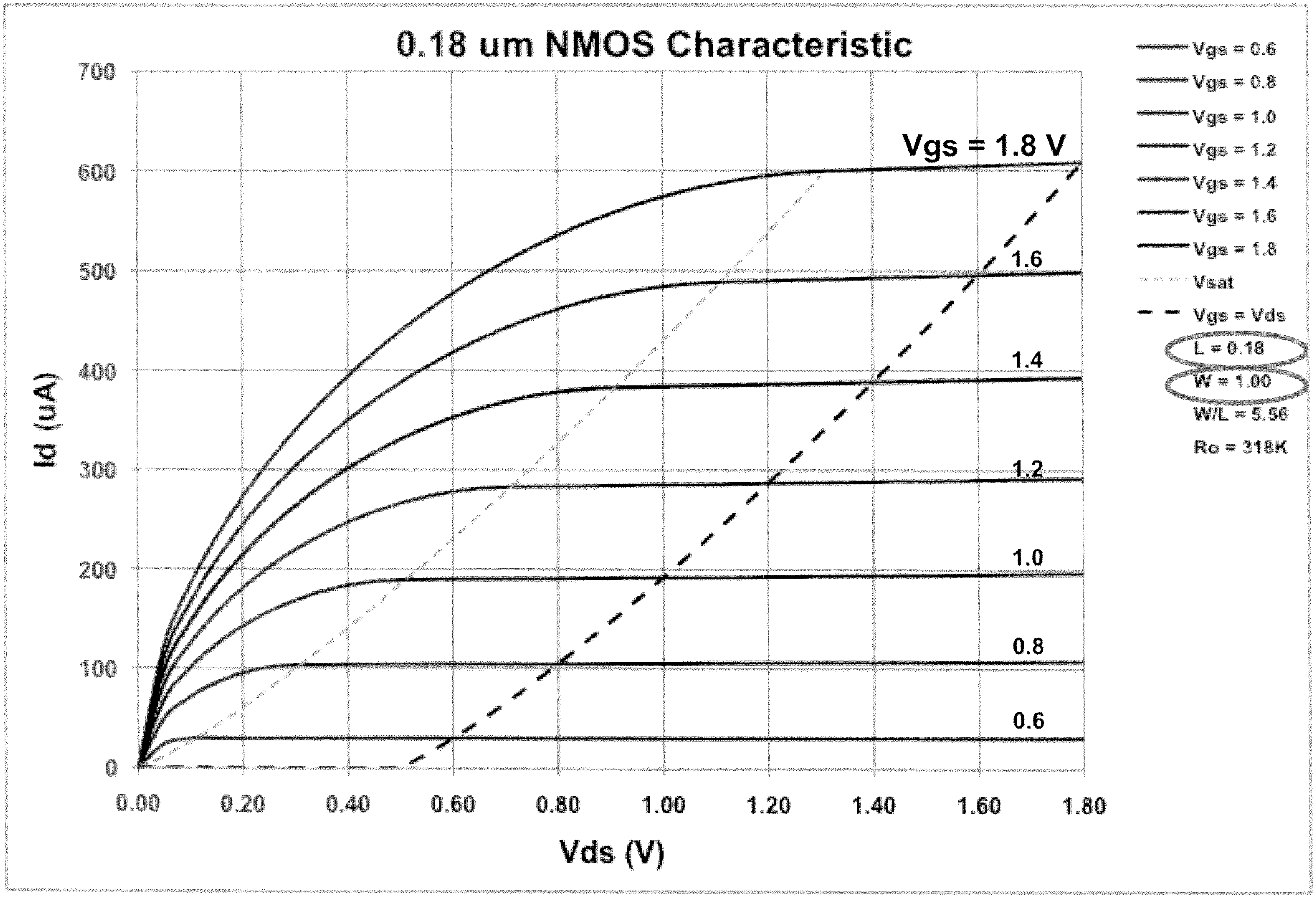
$= 1,941 E^{-18}$ F/μm $= \underline{1.941 E^{-15} \text{ F/μm}}$

or $\underline{1.94 \text{ fF/μm}}$

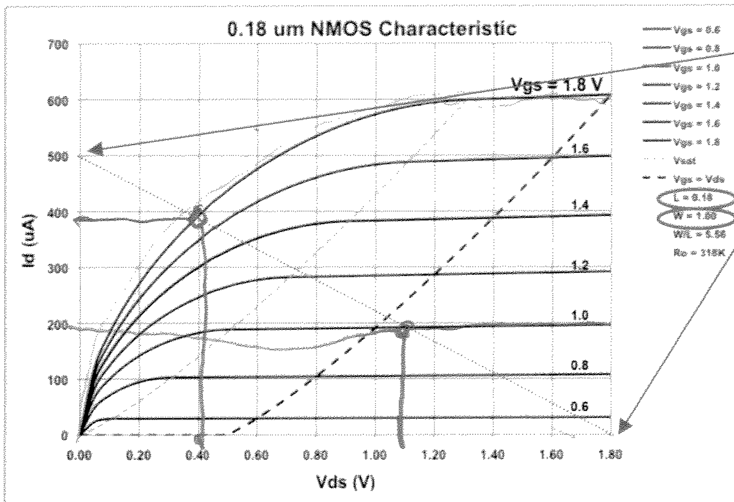
#3 $t_{ox} = 5nm$ $e_r = 25$

$25 \times 8.85E^{-3}$ fF/μm $\times \frac{90nm}{5nm}$

$= 3.98$ fF/μm


0.18 um NMOS Characteristic
Vgs = 1.8 V
1.6
1.4
1.2
1.0
0.8
0.6
Id (uA)
700
600
500
400
300
200
100
0
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vds (V)
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 0.18
W = 1.00
W/L = 5.56
Ro = 318K

2.5



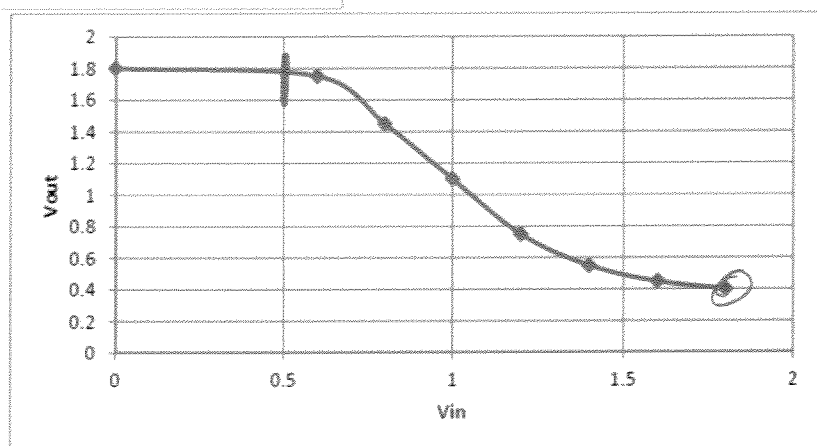
At Vds = 0, 1.8V dropped over 3.6K R.

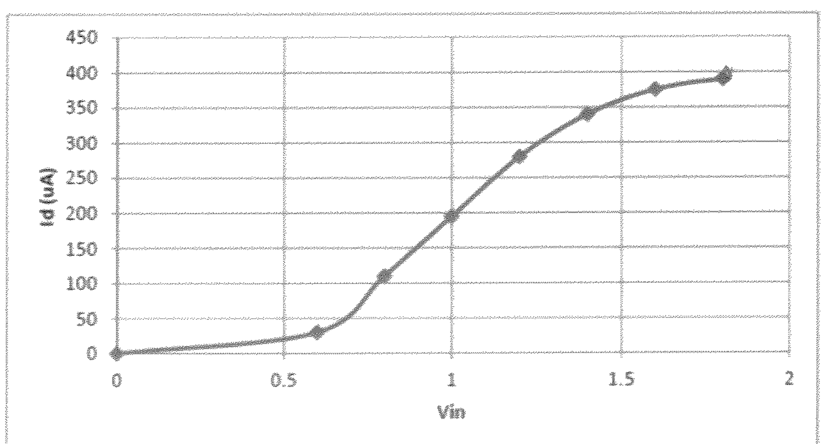
Ids = 1.8/3.6 = 0.5ma

At Vds = 1.8, no drop across R. Ids = 0.

Vds and Ids MUST! Be on red line.

Vin	Vout	ID
0	1.8	0
0.6	1.75	30
0.8	1.45	110
1	~~1.1~~	195
1.2	0.75	280
1.4	0.55	340
1.6	0.45	375
1.8	0.4	390





2c. Max current at Vin = Vdd = 1.8V = 390 μA

2d. Min Vout at same Vin = ~0.4V ~ 0.4V