HW6-Memory and Delay

1. (10) Book 12.1, except 8192 72-bit words

72 bits = 9 bytes. There are a total of 8192*72 = 589824 bits. A square of bits is 768x768 this is not a power of two. Several cases:

- 512x1152 = 512 rows by 144B, or 512 rows by 16 words. Column mux needs 4 bits
- 1024 rows by 576 columns or 1024 rows of 72B or 1024 rows by 8 words. Column mux needs 3 bits

2. (10) Book 12.2

The dimensions are (128 columns * 1.3 μm/col* 1.1) x (128 rows * 1.44 μm/row*1.1) = 183 μm x 203 μm
3. Fig. 12.18 (Note the original said 12.8) shows a 2-port SRAM bit (1 read and 1 write). Draw a transistor schematic and then a stick figure for a 3-port SRAM bit (2 reads, 1 write), and estimate the area. You need not try to be superoptimal, only understand the “complexity” of getting a dense design.

Rough area 9x8 high by 16x8 wide = 200λ²
The rising delay is \((R/2)*2C + R*(5C+5hC) = (6+5h)RC\) and the falling delay is \(R*(5C+5hC) = (5+5h)RC\).

\[
\text{Rise: } B = \phi, \quad A \cdot 1 = \phi
\]

\[
\text{Delay: } = \frac{R}{2} \times 2C + R \times (5+5h)C = (6+5h)RC
\]

The output node has $3nC$. Each internal node has $2nC$. The resistance through each pMOS is $R/n$. Hence, the propagation delay is

$$t_{pd} = R(3nC) + \sum_{i=1}^{n-1} \left( \frac{iR}{n} \right)(2nC) = \left( n^2 + 2n \right) RC$$
6. (20) Fig. 1.18 in book (page 12) shows a compound gate. Do the same for this circuit as for Book 4.4. It may help to draw stick figure to ensure you are counting everything.

Worst case falling is $A=C=1$, $D=0$, $B:0\Rightarrow1$

Worst case rising: $B=1$, $A=0$, $C:1\Rightarrow0$

$A=1, B=D=0, C=1, D=1 \Rightarrow \emptyset$

Red is capacitance in units of $1\times1$ gate

Falling: Draw to match stick

$$\frac{R}{2} \times C + \left(\frac{R}{2} + \frac{R}{2}\right) 20C = 20.5RC$$
The text reads:

# 6 rising  A = 1, B = 0, C = 1, D = 1 → 0

The diagram shows a circuit with resistors and capacitors. The equation is:

\[(R/2)(12C) + (R/2 + R/2)10C = 16RC\]
7. (20) Build an Elmore model for both rise and fall times for a 3-input NAND as described in Fig. 4.7 on page 148 driving 10 inverters sized as in Fig. 4.6 (i.e. for each inverter, p has a k of 2, n-type has a k of 1)

Each inverter has an input capacitance of (1+2)C. Thus 10 of them adds 30C to Y. You could then look at Example 4.7 and replace the 5h by 30.

The falling delay is then \( \frac{R}{3}(3C) + (\frac{R}{3}+\frac{R}{3})3C + (\frac{R}{2}+\frac{R}{3}+\frac{R}{3})39C = RC+2RC+39RC = 42RC \)

The rising delay is \( (3C + 3C + 39C)R = 45RC \)