HW5: MOSFETs, Verilog

1. (10)Book Problem 2.2
2. (10)Book problem 2.10a
3. (10)Book problem 2.20a – i.e. develop using the Long Channel Model the IV equation for two identican NMOS transistors in parallel.
4. (10)Using the Excel spreadsheet on the class website, the ND technology, an NMOS invertor where the width is 4λ, and a Vdd of 4V, what is the resistor value you would need to have a Vgs of 2V give a Vds of 2V as output. What is the maximum on current when Vgs=4V.
5. (20)Again using the Excel spreadsheet for a CMOS invertor where the NMOS is as in the above problem, what is the PMOS width you would need so that Ain = 2V gives Aout of 2V? What is the max current for an input of 4V; What is it for an input of 0V?
6. (10)Book Problem A2 page 776 (Verilog)
7. (10)Book Problem A16
8. (10)Write down Verilog code for a behavioral model for a 2-input exclusive or gate using just "&", "|", and "~". Then using this module, develop a structural module for an 8 bit parity generator – 1.e. there are 8 dAta inputs which should be combined by 3 l3v3ls of xors to compute the odd parity of the data bits. This parity should be output.
9. (20)Write the behavioral code for a module named "grey" that implements a 4-bit "Grey code" (see https://en.wikipedia.org/wiki/Gray_code) counter with the following characteristics:

    1. An input CLk that is the clock
    2. An input Reset that when high resets the counter to 0000 when the Clk goes from low to high
    3. An input Count that when high, and when the Clk goes from low to high (while Reset is low) advances the counter to the next Grey code value. When Count is low, the outputs stay unchanged.