Homework 7: Logical Effort

1. (50pts) Consider an N-input NOR gate with an on-resistance 1/4th that of a NOR gate with unit n-type transistors. Following along as the book does for an N-input NAND gate compute each of the following as a function of N? Justify as necessary. (You may get slightly different answers for N even or N odd)
    1. (10) Draw a stick figure (you may have to have different figures for N even or odd) and use those figures for the following
    2. (5) What are the widths of the transistors
    3. (5) What is the input capacitance
    4. (5) What is the output diffusion capacitance
    5. (5) What is the normalized parasitic delay (show Elmore Model – don't just use book's estimate of diffusion to gate cap.) See Fig. 4.23 for n-input NAND case. Duplicate that for n-INPUT NOR
    6. (5) What is the logical effort
    7. (5) What is the effort delay if you are driving h identical copies of your gate
    8. (5) What is the drive?
    9. (5) For h=10 and a 65nm technology, what is the delay thru your NOR in pico seconds.
2. (15pt) Assume you want to create a 9-input NOR function by having 3 3-input NORs each driving one input of a 3-input NAND, whose output drives an inverter, and whose output of that invertor driving 10 unit inverters.
    1. (10) What size transistors might you use in the NORs, NAND, and inverter for minimum delay/ What is that delay?
    2. (5) What would have been the delay if you had built one giant 9-input NOR gate using your computations from problem 2?
3. (35pt) Given the study you did on your selected microprocessor, in retrospect what might you have done differently or in more detail for that level of study? Then walk through the steps you would take if your job was to create a real chip (say for ND's technology). In particular how would you attack the problem of selecting transistor widths to speed up your design? I'm not expecting details or actual calculations, just some sentences or bullet points that indicate you understand the process.