CSE 40462 VLSI Design
Homework 1
See website for due date.

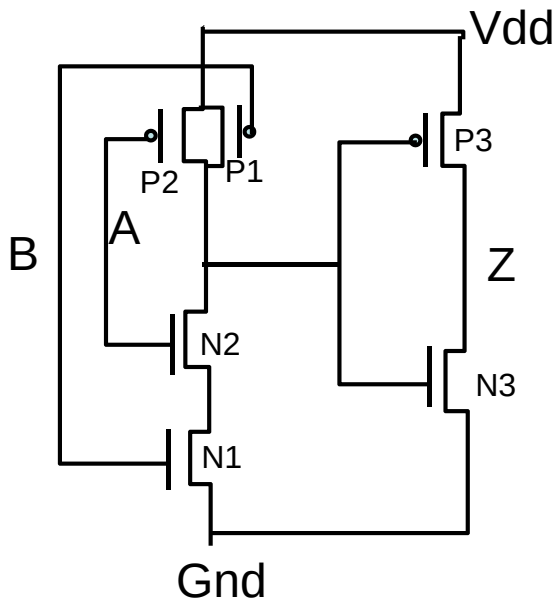
Note that solutions to odd problems as stated in the book are available at http://www.cmosvlsi.com/solutionsodd.pdf.

Do the following problems based on Chapter 1 in Weste & Harris:

1. 1.5 – change to a 5 input NAND gate
2. 1.6 – this should be a transistor diagram of a single gate, not a combination of simpler NAND/NOR gates.
3. 1.8 – ABC + AB'C' + A'BC' + A'B'C. Implement as one gate that gives the negation of the desired function that then drives an inverter.
4. Draw a transistor diagram for a tri-state 2 input NAND, with 3 inputs labeled A, B, and EN. *You can assume you have not(EN).*
5. Draw a transistor diagram for a 4-input inverting multiplexor **using transmission gates**. Count the number of transistors. Estimate how many transistors you would need if you only used 2 or 1 input gates as in slide 18 of lecture "Circuits-c", or if you built a compound mux as in slide 20 (give both estimates and a rationale).
6. Draw a diagram like Fig. 1.32(b) for a positive-edge-triggered-sensitive JK flip flop where J and K are inputs and the flip flop has functions as follows. Also count the total number of transistors you would need.

J input	K input	Q next
0	0	Q
0	1	0
1	0	1
1	1	~Q

7. Simple CMOS Circuits. Fill in the table below, indicating for each input combination which transistors are "ON" or "OFF." If "Hi" is a logic 1 and "Low" is a logic 0, show the logic output. What is the logic function?



A	B	N1	N2	N3	P1	P2	P3	Z
Hi	Hi							
Hi	Low							
Low	HI							
Low	Low							

8. Design a 3-input inverting multiplexer with data inputs A, B, and C and control inputs S0 and S1 that select inputs as defined in the table below, with two implementations:

S0	S1	Y=Output
0	0	~B
0	1	~B
1	0	~C
1	1	~A

- As a set of transmission gates with an inverter on the output
- As a single complementary gate (i.e. a set of Ntypes at bottom and p-types at top)

Assume both ~S0 and ~S1 are available.

9. Estimate the number of transistors needed for 4-bit adders in each of the following:

    1. A 4-bit ripple adder based on Fig. 11.11
    2. A 4-bit adder using generates and propagates based on Fig. 11.14
    3. A 4-bit carry-skip adder based on Fig. 11.20

For each case, indicate how you decided to estimate each block, i.e. converted each logic gate as shown into an equivalent CMOS gate (you may need extra inverters), or converted various collections of logic gates into specially designed complementary circuits. For now don't worry about delay (later). A valid answer is a correct answer – however, I'll tabularize the results of different designs so we can see who came up with the "minimal" design.

10. Design a barrel shifter for 4-bit numbers that can shift 0, 1, 2, or 3 places optionally either left or right and optionally either 0 fill or circular shift, and estimate the number of transistors. Try to find a design with a minimal number of transistors. Assume as inputs:

    - A_3, A_2, A_1, and A_0 are input bits
    - Y_3, Y_2, Y_1, and Y_0 are output bits
    - S_1, and S_0 are the shift values
    - D is 1 for left and 0 for right
    - F is 0 for fill with 0s and 1 for circular fill

The negations of all control signals are available if needed. You *may* (but don't have to) want to consider using the 3 input mux of the prior problem. Any valid answer is a correct answer.