Final Exam Topics VLSI 2018

Exam distributed: 10:30am – 12:30pm Wed. Dec. 12, 356a Fitz. In class: Open book and notes
Due back Thursday 5pm my office or Dept. mailbox
Following is intended to guide your review, not guaranteed to be inclusive.

Questions from prior exams with some difficulties:

- Elmore models
- Long-channel-model and IV curves
- Difference between Dennard and Constant Voltage scaling
- Verilog (sufficiently covered by other work)

New material since last exam:

1. (Niemier presentation) Intro to some nano devices (in Multiple choice)
2. (531) Flash memory (again probably just multiple choice /short answer)
3. Delay: Chap. 4.1-4.3 (repeated from last exam)
    1. (141) Definitions of delay
    2. Identifying diffusion capacitance in a circuit
    3. (146) Relationship of R and C values with transistor widths
    1. (147) Drawing equivalent RC circuits for rise and fall times
    2. (152) Definition of FOn
    3. (150) Drawing and using Elmore model to compute delay estimate
    4. Determining combination of input transitions that maximize/minimize a single logic gate's delay

4. Logical Effort: Chap. 4.4-4.5
    5. (155)The linear delay model d = f + p, where f = gh
    6. Be able to compute the p and g terms for a logic circuit
    7. (159) Definition of drive and relationship to delay
    8. (159) Extracting delay information from a Datasheet
    9. Normalized delay
    10. Be able to compute h for a particular circuit
    11. Be able to compute branching factors
    12. Be able to compute overall minimum delay for a multi-level circuit
    13. Be able to determine optimal logical effort delay per stage as $GBH^{(1/N)}$, and use that to go backwards and identify logic gate input capacitance
    14. Be able to use logic gate input capacitance to compute scale factor for internal transistor widths