Introduction to CMOS VLSI Design

VLSI Design Rules

Peter Kogge
University of Notre Dame
Fall 2011, 2012, 2015, 2018

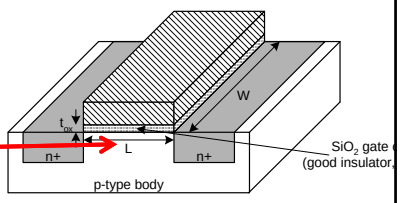
Based on material from
Prof. Jay Brockman, Joesph Nahas, University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- Overview
- Determining Design Rules and Mask Biases
- Design Rules
- Circuit Interconnect Layout

Layout Overview

- *Minimum dimensions* of mask features determine:
  - transistor size and die size
  - hence speed, cost, and power
- "Historical" *Feature size f* = gate length (in nm)
  - Set by *minimum width* of polysilicon
  - Other minimum feature sizes tend to be 30 to 50% bigger.
- *Design* or *Layout Rules*: rules for designing masks based on minimum feature sizes
- Rules often "normalized" for portability across generations

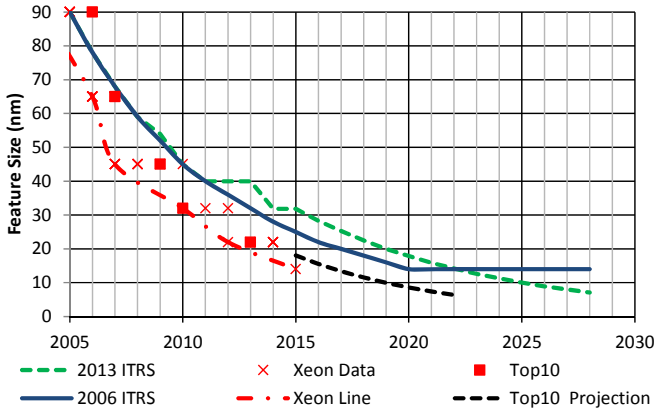


What Are Typical Rules

- Length & Width of Transistor gate
- Separation between 2 wires on same level
- Width of wires
- Contact pad for Vias
- Cross section of Vias
- Size of Wells
- …

Feature Size

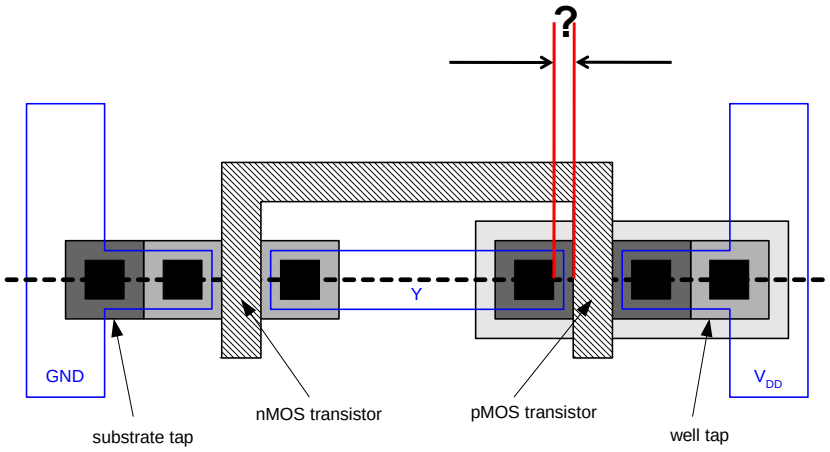
- Feature size improves 30% every 2 years or so
  - 1/√2 = 0.7 reduction factor every "generation"
  - from 1 μm (1000 nm) in 1990 to 14 nm in 2015.
  - 10 generations in 20 years
    - 1000, 700, 500, 350, 250, 180, 130, 90, 65, 45, 32, 22, 14, 10 nm



Determining a Design Rule and a Mask Bias

Determining a Design Rule

- What is the minimum spacing between a poly gate and a contact? What does it depend on?

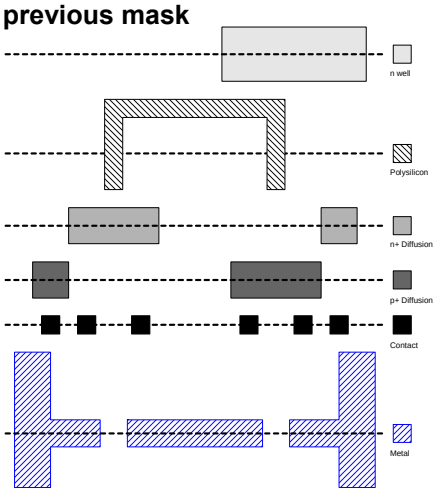


Factors Determining a Design Rule

- Mask alignment accuracy
  - How accurate is one mask aligned to another mask?
- Process variation
  - If cutting a hole, how much do sides of the cut vary?
  - If implanting dopants, how much does the width of the diffusion vary?
- How conservative do you need to be to assure good process yield?
  - 30 to 40 mask levels
  - 5 to 10 process steps per mask level

Mask Sequence

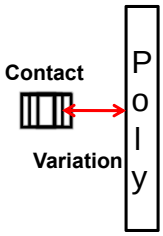
- Align each mask to the previous mask
  1. n-well
  2. Polysilicon
  3. n+ active (diffusion)
  4. p+ active (diffusion)
  5. Contact
  6. Metal



Alignment Marks

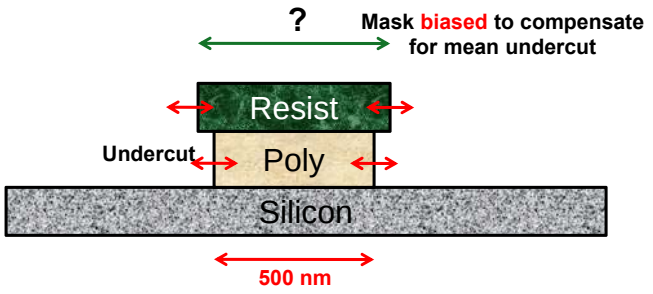
- Alignment Marks:

- How close can one mask be aligned to another in a 0.5 µm process?
- Example:
  - Mean: 0 nm
  - Standard Deviation: 50 nm
    - 1σ = 50 nm = 84%
    - 2σ = 100 nm = 98%
    - 3σ = 150 nm = 99.87%
- But alignment is not direct
  - Contact aligns to P+active
  - P+active aligns to N+active
  - N+active aligns to poly
- How much variation is the alignment from Contact to Poly?



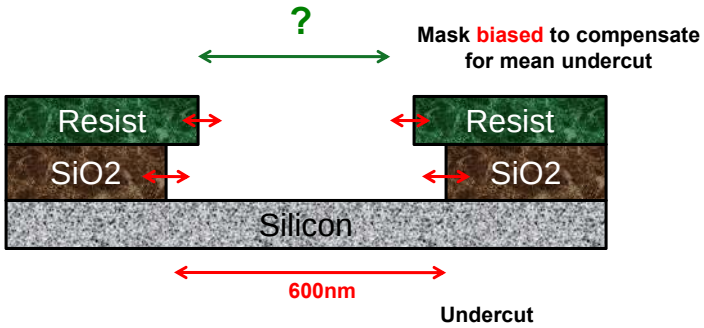
Poly Variation

- How much does the width of the poly vary with processing?
- Example: (Again 0.5 μm)
  - Mean (one side) = - 60 nm (undercut)
  - Standard Deviation (one side) = 30 nm
  - 3σ = 90 nm



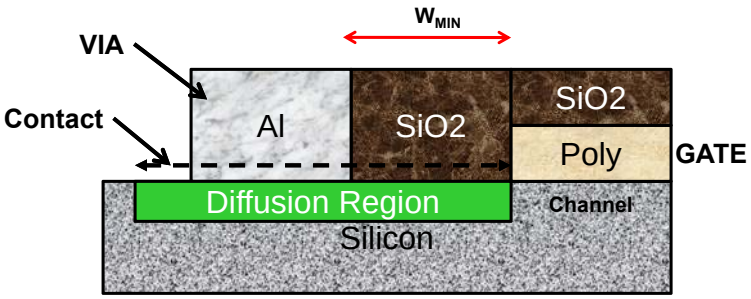
Contact Hole Variation

- How much does the size of the contact hole vary?
- Example:
  - Mean = + 50 nm
  - Standard Deviation = 40 nm
  - 3σ = 120 nm



Minimum Oxide Width

- Cannot have source or drain short to the gate.
  - What is minimum spacing with variation?
  - Example: 200 nm



Design Rule Summary

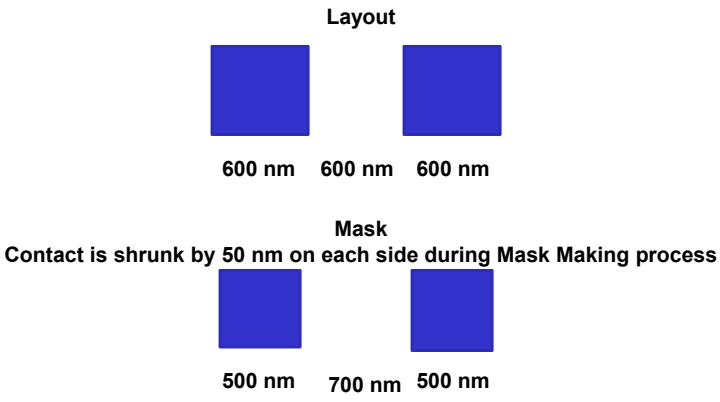
- Mask Alignment
  - 3σ variation is √3 * 150 nm = 260 nm
- Poly Variation
  - 3σ = 90 nm
- Contact Variation
  - 3σ = 120 nm
- Minimum Contact-to-Poly Breakdown Space
  - 200 nm
- If we simply sum the minimum and variations:
  - 670 nm
- Is this the "correct" value for the rule? What is "correct"?
- Design Rule:
  - nm
- Why?

How can the rule be improved?

- Change alignment sequence.
  - Align poly to n-well
  - Align n+active to poly
  - Align p+active to poly
  - Align contact to poly
  - Align metal to contact
- Change alignment from t3 to t1
  - Alignment variation reduces from 260 nm to 150 nm
- Design Rule changes from 500 nm to 400 nm

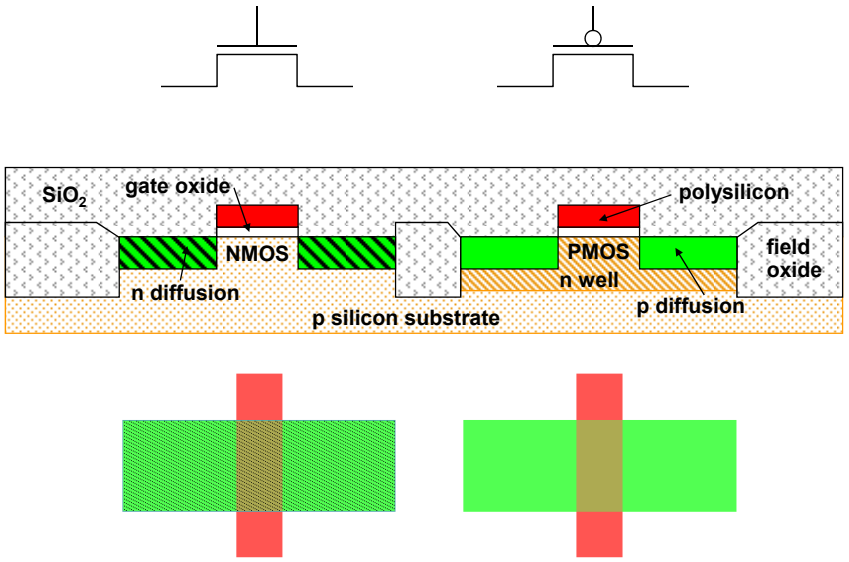
What do you do with Biases?

- Layout is done without biases.
- Biases are added post layout in mask processing.
- Example: Contacts

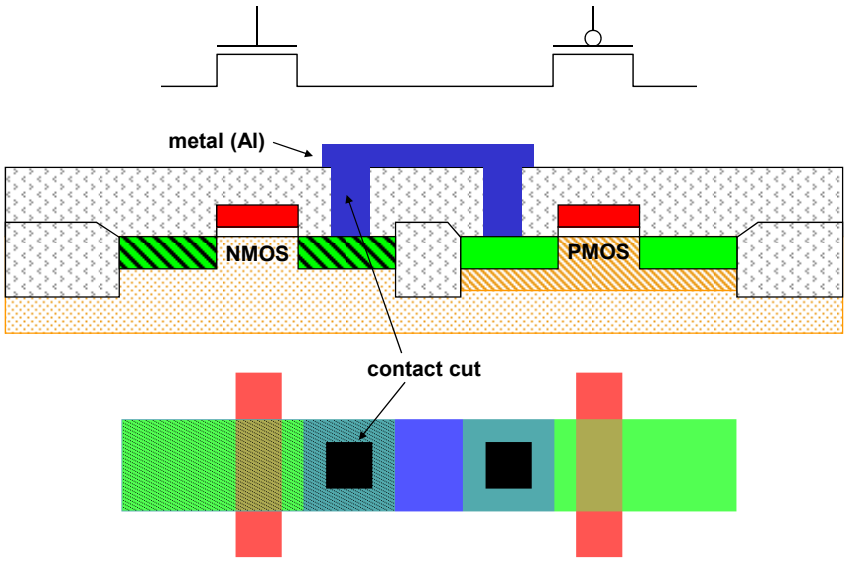


Circuit Interconnect Layout

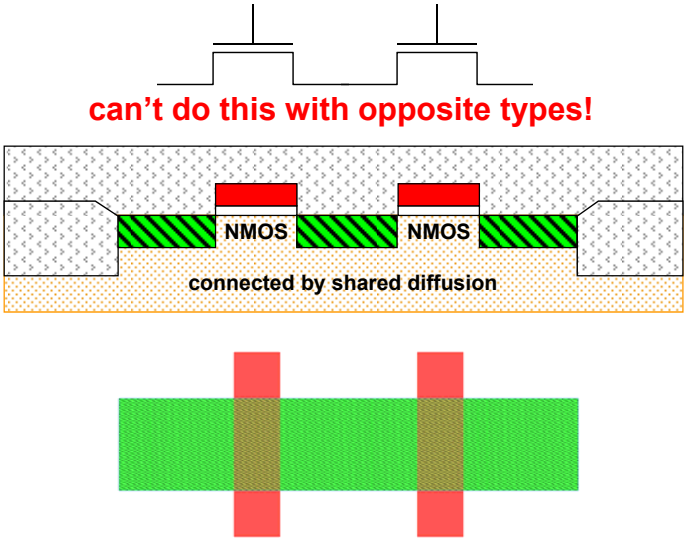
Simplified CMOS Process



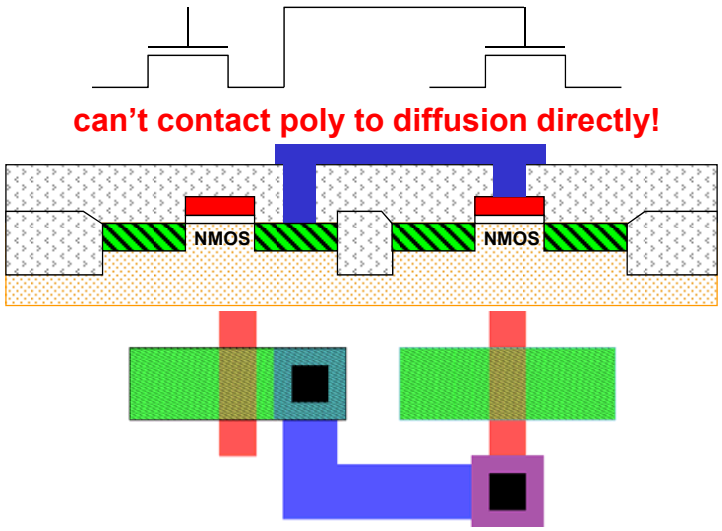
Wiring with Metal and Contacts



Transistors of Same Type in Series

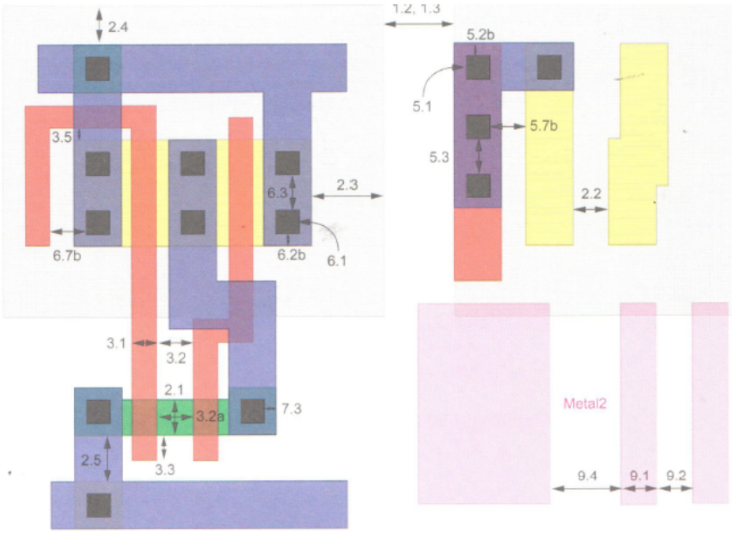


Connecting Poly and Diffusion

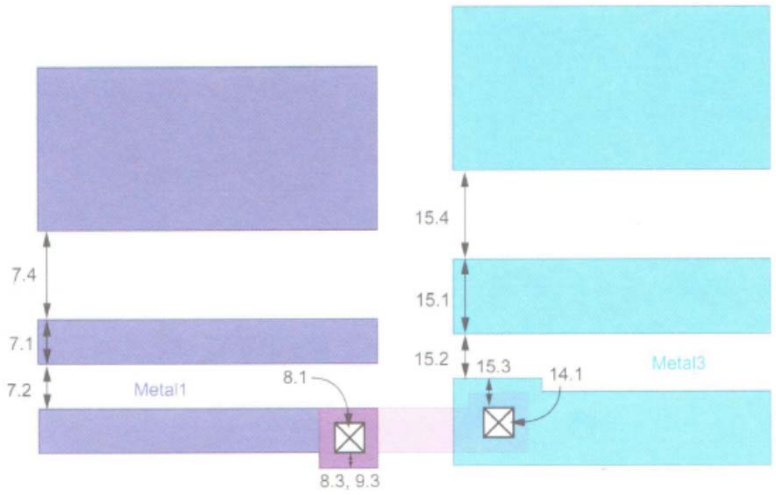


The Book's 65nm Process

The Book's 65nm Process - Up to Metal 2



The Book's 65nm Process - Metals



65nm Design Rules (Page 1)

	Rule	Description	65nm (nm)
Well	1.1	Width	500
	1.2	Space to well at different potential	700
	1.3	Space to well at same potential	700
Active (diffusion)	2.1	Width	100
	2.2	Spacing to active	120
	2.3	Source/drain surround by well	150
	2.4	Substrate/well contact surround by well	150
	2.5	Spacing to active of opposite type	250
Poly (i.e. Gate)	3.1	Width	65
	3.2	Spacing to poly over field oxide	100
	3.2a	Spacing to poly over active	100
	3.3	Gate extension beyond active	100
	3.4	Active extension beyond poly	100
	3.5	Spacing of poly to active	70
Select (n or p)	4.1	Spacing from substrate/well to gate	150
	4.2	Overlap by poly or active	120
	4.3	Overlap of substrate/well contact	120
	4.4	Spacing to select	200

65nm Design Rules (Page 2)

	Rule	Description	65nm (nm)
Contact (to poly or active)	5.1, 6.1	Width (exact)	80
	5.2b, 6.26	Overlap by poly or active	10
	5.3, 6.3	Spacing to contact	100
	5.4, 6.4	Spacing to gate	70
	5.5b	Spacing of poly contact to other contact	
	5.7b, 6.7b	Spacing to active/poly for mult. Contacts	
	6.8b	Spacing of active contact to poly contact	
Metal1	7.1	Width	90
	7.2	Spacing to same layer of metal	90
	7.3,8.3	Overlap of contact or via	10
	7.4	Spacing to metal for lines wider than 10λ	300
Metal2	9.1....	Width	100
	9.2, ...	Spacing to same layer of metal	100
	9.3, ...	Overlap of contact or via	10
	9.4, ...	Spacing to metal for lines wider than 10λ	300
Metal3	15.1	Width	100
	15.2	Spacing to metal3	100
	15.3	Overlap of via2	10
	15.4	Spacing to metal for lines wider than 10λ	300
Metal 8-9	15.1	Width	400
	15.2	Spacing to metal3	400
	15.3	Overlap of via2	100
	15.4	Spacing to metal for lines wider than 10λ	500
Via1 Via2	8.1,14.1	Width (exact)	100
	8.2.14.2	Spacing to via on same layer	100
Via 3...6	8.1,14.1	Width (exact)	100
	8.2.14.2	Spacing to via on same layer	100
Via 7,8	8.1,14.1	Width (exact)	200
	8.2.14.2	Spacing to via on same layer	200

A Simplified Rule System
λ Rules

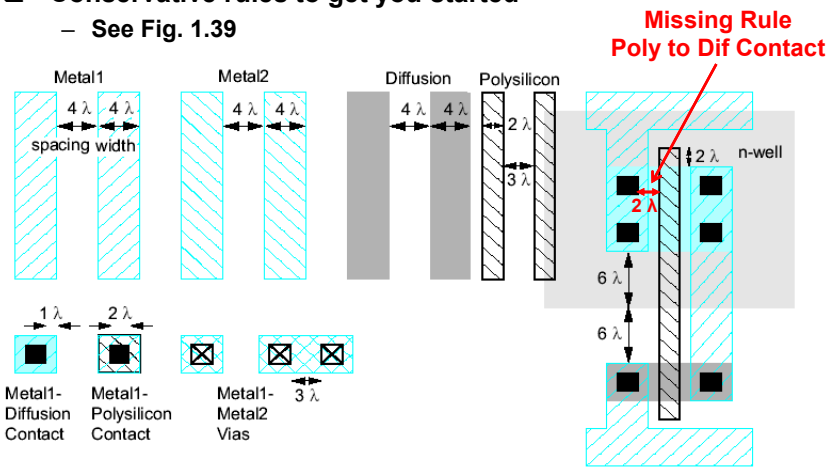
λ Rules

A simplified, technology generations independent design rule system:

- Express rules in terms of **λ = f/2**
  - E.g. λ = 0.3 mm in 0.6 mm process
- Called "Lambda rules"
- Lambda rules NOT used in commercial applications
  - Lambda rules need to be very conservative and thus waste space.
- Lambda rules good for education!
  - MOSIS SCMOS SUMB Rules
  - See Book Front Inside Cover

Simplified Design Rules

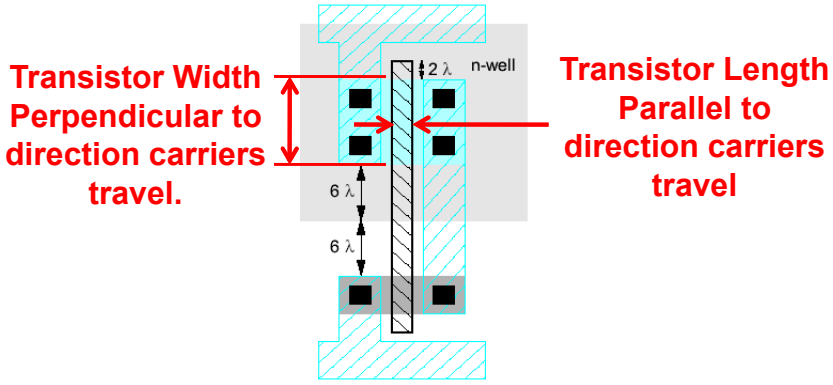
- Conservative rules to get you started
  - See Fig. 1.39



http://www.cse.nd.edu/courses/cse60462/www/links.html

Transistor Width and Length

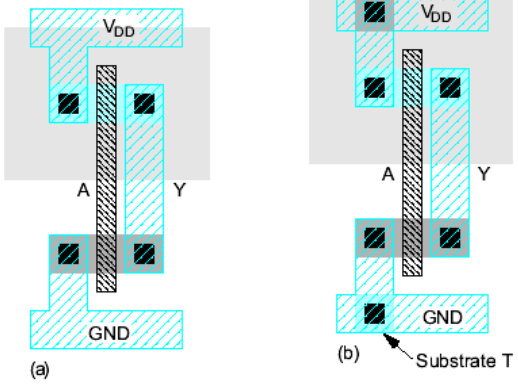
Dimensions of Gate over Source/Drain Diffusion
This is the active area of a transistor.



Typically Width >> Length

Substrate and Well Taps

- Substrate needs to be tied to Ground.
  - Why?
- N-well needs to be tied to V_{DD}.
  - Why?



λ Rules (compared to 65 nm)

				Lambda Rules										
	Rule	Description	65nm (nm)	Eqvt 65nm	in λ	180	130	90	65	45	32	28	22	10
Well	1.1	Width	500	390	12	1080	780	540	390	270	192	168	132	60
	1.2	Space to well at different potential	700	585	18	1620	1170	810	585	405	288	252	198	90
	1.3	Space to well at same potential	700	195	6	540	390	270	195	135	96	84	66	30
Active (diffusion)	2.1	Width	100	98	3	270	195	135	98	68	48	42	33	15
	2.2	Spacing to active	120	98	3	270	195	135	98	68	48	42	33	15
	2.3	Source/drain surround by well	150	195	6	540	390	270	195	135	96	84	66	30
	2.4	Substrate/well contact surround by well	150	98	3	270	195	135	98	68	48	42	33	15
	2.5	Spacing to active of opposite type	250	130	4	360	260	180	130	90	64	56	44	20
Poly (i.e. Gate)	3.1	Width	65	65	2	180	130	90	65	45	32	28	22	10
	3.2	Spacing to poly over field oxide	100	98	3	270	195	135	98	68	48	42	33	15
	3.2a	Spacing to poly over active	100	98	3	270	195	135	98	68	48	42	33	15
	3.3	Gate extension beyond active	100	65	2	180	130	90	65	45	32	28	22	10
	3.4	Active extension beyond poly	100	98	3	270	195	135	98	68	48	42	33	15
	3.5	Spacing of poly to active	70	33	1	90	65	45	33	23	16	14	11	5
Select (n or p)	4.1	Spacing from substrate/well to gate	150	98	3	270	195	135	98	68	48	42	33	15
	4.2	Overlap by poly or active	120	65	2	180	130	90	65	45	32	28	22	10
	4.3	Overlap of substrate/well contact	120	33	1	90	65	45	33	23	16	14	11	5
	4.4	Spacing to select	200	65	2	180	130	90	65	45	32	28	22	10

Green: lambda rules significantly smaller
Red: lambda rules significantly larger

λ Rules (compared to 65 nm)

	Rule	Description	65nm (nm)	Eqvt 65nm	in λ	180	130	90	65	45	32	28	22	10
Contact (to poly or active)	5.1, 6.1	Width (exact)	80	65	2	180	130	90	65	45	32	28	22	10
	5.2b, 6.26	Overlap by poly or active	10	33	1	90	65	45	33	23	16	14	11	5
	5.3, 6.3	Spacing to contact	100	98	3	270	195	135	98	68	48	42	33	15
	5.4, 6.4	Spacing to gate	70	65	2	180	130	90	65	45	32	28	22	10
	5.5b	Spacing of poly contact to other contact		163	5	450	325	225	163	113	80	70	55	25
	5.7b, 6.7b	Spacing to active/poly for mult. Contacts		98	3	270	195	135	98	68	48	42	33	15
	6.8b	Spacing of active contact to poly contact		130	4	360	260	180	130	90	64	56	44	20
Metal1	7.1	Width	90	98	3	270	195	135	98	68	48	42	33	15
	7.2	Spacing to same layer of metal	90	98	3	270	195	135	98	68	48	42	33	15
	7.3,8.3	Overlap of contact or via	10	33	1	90	65	45	33	23	16	14	11	5
	7.4	Spacing to metal for lines wider than 10λ	300	195	6	540	390	270	195	135	96	84	66	30
Metal2	9.1....	Width	100	98	3									
	9.2, ...	Spacing to same layer of metal	100	98	3									
	9.3, ...	Overlap of contact or via	10	33	1									
	9.4, ...	Spacing to metal for lines wider than 10λ	300	195	6									
Metal3	15.1	Width	100	163	5	450	325	225	163	113	80	70	55	25
	15.2	Spacing to metal3	100	98	3	270	195	135	98	68	48	42	33	15
	15.3	Overlap of via2	10	65	2	180	130	90	65	45	32	28	22	10
	15.4	Spacing to metal for lines wider than 10λ	300	195	6	540	390	270	195	135	96	84	66	30
Metal 8-9	15.1	Width	400			0	0	0	0	0	0	0	0	0
	15.2	Spacing to metal3	400			0	0	0	0	0	0	0	0	0
	15.3	Overlap of via2	100			0	0	0	0	0	0	0	0	0
	15.4	Spacing to metal for lines wider than 10λ	500			0	0	0	0	0	0	0	0	0
Via1 Via2	8.1,14.1	Width (exact)	100	65	2	180	130	90	65	45	32	28	22	10
	8.2.14.2	Spacing to via on same layer	100	98	3	270	195	135	98	68	48	42	33	15
Via 3...6	8.1,14.1	Width (exact)	100			0	0	0	0	0	0	0	0	0
	8.2.14.2	Spacing to via on same layer	100			0	0	0	0	0	0	0	0	0
Via 7,8	8.1,14.1	Width (exact)	200			0	0	0	0	0	0	0	0	0
	8.2.14.2	Spacing to via on same layer	200			0	0	0	0	0	0	0	0	0