Introduction to CMOS VLSI Design

Stick Diagrams: Euler Paths

Peter Kogge
University of Notre Dame
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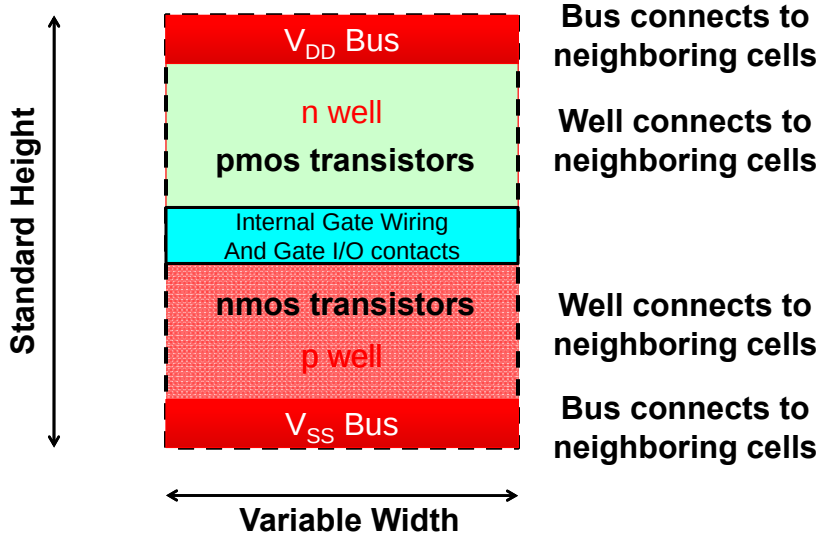
Based on material from
Prof. Jay Brockman, Joseph Nahas, University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Standard Cell Layout



Bus connects to neighboring cells

Well connects to neighboring cells

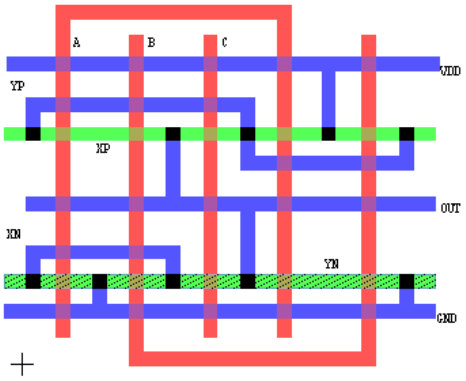
Well connects to neighboring cells

Bus connects to neighboring cells

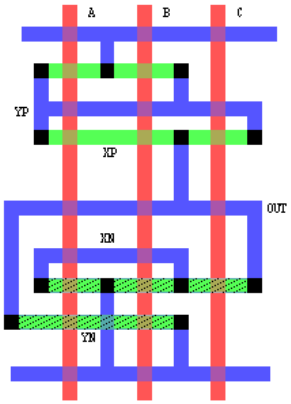
Audience Question: Why is "connecting to neighbors" a good thing?

Complex Circuit Layouts

$\overline{C\,(A+B) + AB}$



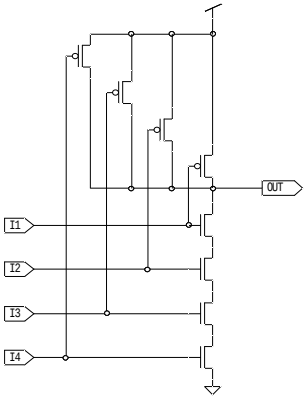
Single diffusion runs



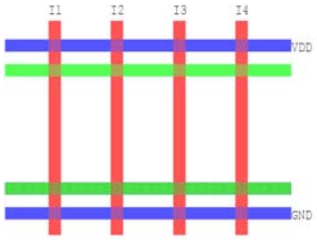
Multiple Diffusion runs

4-Input NAND Gate "Sticks" Layout

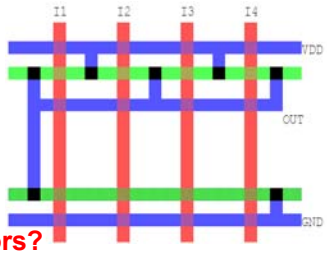
Complementary transistor pairs share common gate connection.



Step 1: order gate wires on poly

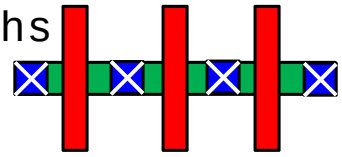


Step 2: interconnect



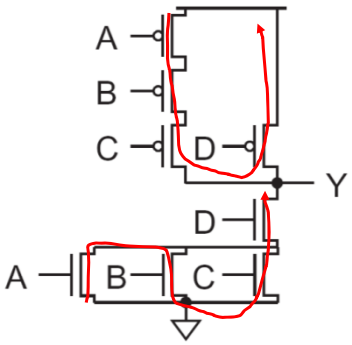
If pmos are 8/2, what are the nmos transistors?

Euler Paths

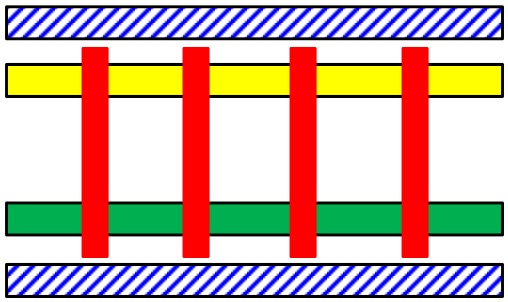


- We start off with
  - diffusion as one row, no breaks!
  - Poly runs vertically
- Each transistor must "touch" electrically ones next to it
- Question:
  - How can we order the relationship between poly and input
  - So that "touching" matches the desired transistor diagram
  - Metal may optionally be used
- Approach:
  - Start with some transistor & "trace" path thru rest of that type
  - May require trial and error, and/or rearrangement

Finding Gate Ordering: Euler Paths

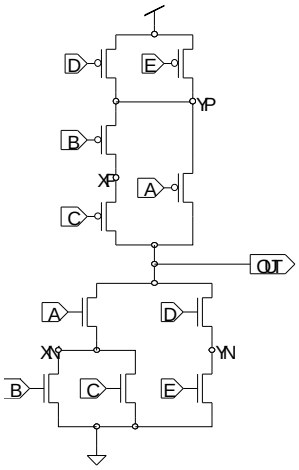


- See if you can "trace" transistor gates in same order, crossing each gate once, for N and P networks independently
  - Where "tracing" means path from source/drain of one to source/drain of next
  - Without "jumping" connections
- ABCD works here



A More Complex Example

$\overline{A(B+C) + DE}$



- See if you can "trace" transistor gates in same order, crossing each gate once, for N and P networks independently
  - Where "tracing" means a path from source/drain of one to source/drain of next
  - Without "jumping"
  - ordering CBADE works for N, not P
  - ordering CBDEA works for P, not N
  - ordering BCADE works for both!

A More Complex Example

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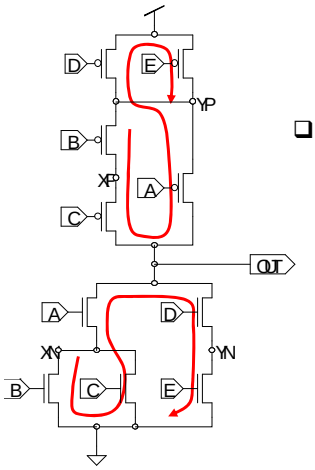
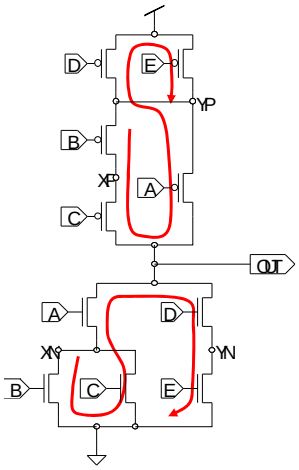
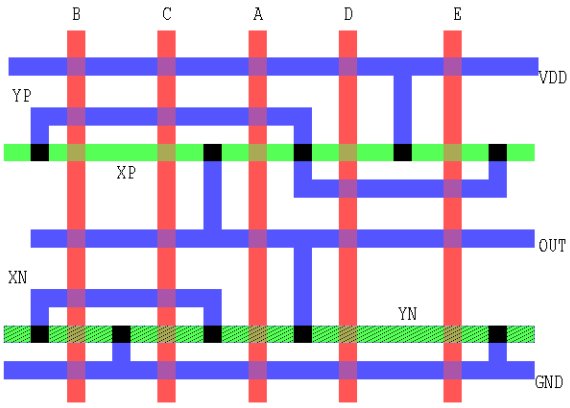


- Trace interconnected gates in SAME order, crossing each gate once, for N,P networks
  - ordering CBADE works for N, not P
  - ordering CBDEA works for P, not N
  - ordering BCADE works for both!

Sticks Layout

$\overline{A(B+C) + DE}$

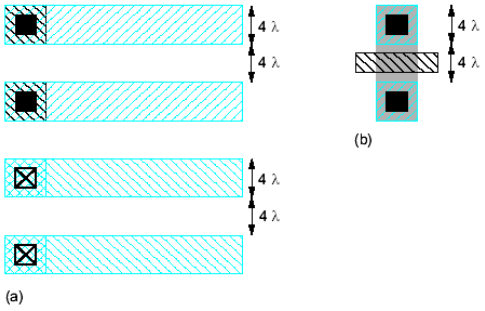




Wiring Tracks and Spacing and Area Estimation

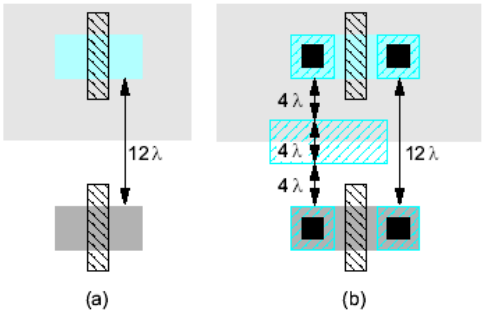
Review: Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ *pitch*
- Transistors also consume one wiring track (WHY?)



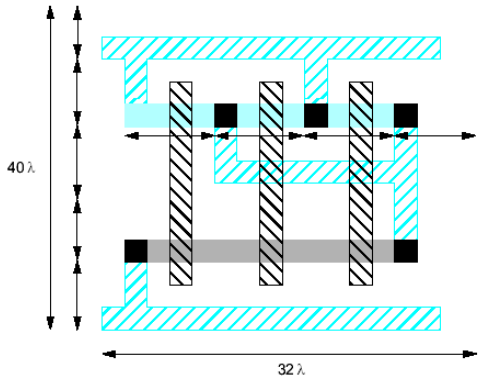
Review: Well spacing

- Wells must surround transistors by 6 λ
  - Implies minimum of 12 λ between opposite transistor flavors
  - Leaves room for one wire track "for free"



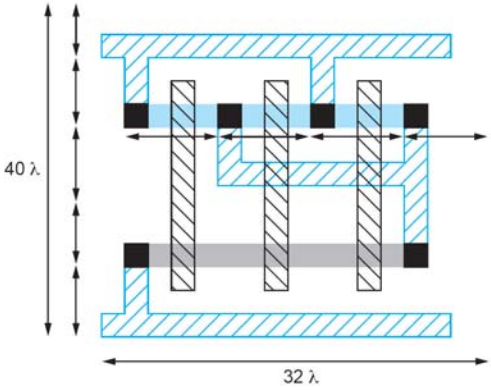
First Cut Area Estimation

- Estimate area by counting required metal wiring tracks
  - Multiply by 8 to express in λ
  - Where does the "8" come from?



Example: NAND3

- Horizontal n-active and p-active strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND/V_{SS} rail at bottom
- 32 λ by 40 λ



Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

$$Y = \overline{(A + B + C)D}$$

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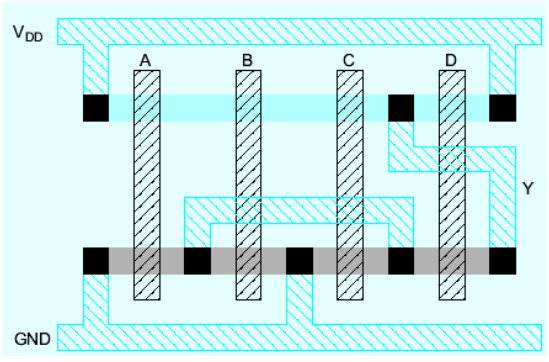
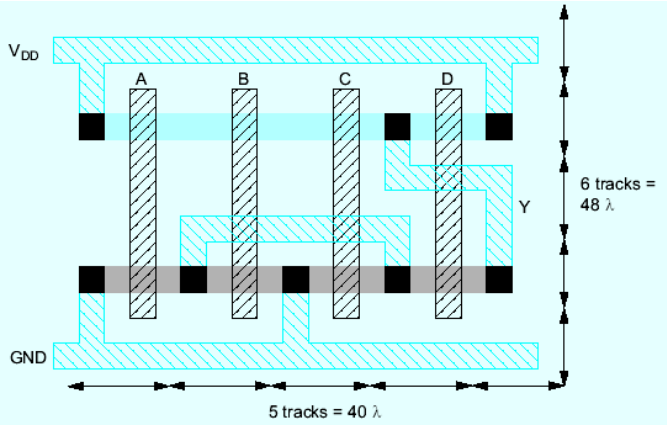


Example: O3AI

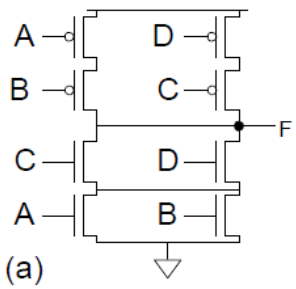
- **Sketch a stick diagram for O3AI and estimate area**

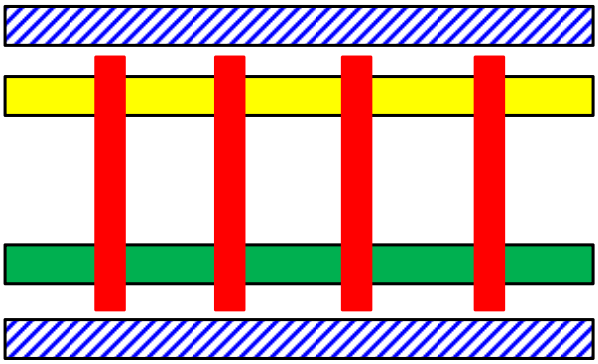
$$Y = \overline{(A+B+C)D}$$



Another Example Question 1.17

- **Consider F= ~((A+B) (C+D))**
  - **Sketch transistors**
  - **Sketch stick diagram**
  - **Estimate area**





Typical Layout Densities (Table 1.10)

Element	Area (in λ^2)
Random Logic	1000-1500/transistor
Datapath	250-750/transistor
SRAM	1000/bit
DRAM	100/bit
ROM	100/bit