**Introduction to CMOS VLSI Design**

**Stick Diagrams: Euler Paths**

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Prof. Jay Brockman, Joseph Nahas, University of Notre Dame  
Prof. David Harris, Harvey Mudd College  
http://www.cmosvlsi.com/coursematerials.html

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**Standard Cell Layout**

- **$V_{DD}$ Bus**: Bus connects to neighboring cells
- **n well**: Well connects to neighboring cells
- **pmos transistors**: Well connects to neighboring cells
- **nmos transistors**: Well connects to neighboring cells
- **$V_{SS}$ Bus**: Bus connects to neighboring cells
- **Internal Gate Wiring**
- **And Gate I/O contacts**

*Audience Question: Why is “connecting to neighbors” a good thing?*
**Complex Circuit Layouts**

\[ C(A+B) + AB \]

- Single diffusion runs
- Multiple Diffusion runs

**4-Input NAND Gate “Sticks” Layout**

Complementary transistor pairs share common gate connection.

**Step 1:** order gate wires on poly

**Step 2:** interconnect

If pmos are 8/2, what are the nmos transistors?
We start off with:
- diffusion as one row, no breaks!
- Poly runs vertically

Each transistor must “touch” electrically ones next to it

Question:
- How can we order the relationship between poly and input
- So that “touching” matches the desired transistor diagram
- Metal may optionally be used

Approach:
- Start with some transistor & “trace” path thru rest of that type
- May require trial and error, and/or rearrangement

Finding Gate Ordering: Euler Paths
- See if you can “trace” transistor gates in same order, crossing each gate once, for N and P networks independently
  - Where “tracing” means path from source/drain of one to source/drain of next
  - Without “jumping” connections
- ABCD works here
A More Complex Example

- See if you can “trace” transistor gates in same order, crossing each gate once, for N and P networks independently
  - Where “tracing” means a path from source/drain of one to source/drain of next
  - Without “jumping”
  - ordering CBDAE works for N, not P
  - ordering CBDEA works for P, not N
  - ordering BCADE works for both!

A More Complex Example

- Trace interconnected gates in SAME order, crossing each gate once, for N,P networks
  - ordering CBDAE works for N, not P
  - ordering CBDEA works for P, not N
  - ordering BCADE works for both!
Sticks Layout

A (B+C) + DE

Wiring Tracks and Spacing and Area Estimation
Review: Wiring Tracks

- A wiring track is the space required for a wire
  - 4\( \lambda \) width, 4\( \lambda \) spacing from neighbor = 8\( \lambda \) pitch
- Transistors also consume one wiring track (WHY?)

Review: Well spacing

- Wells must surround transistors by 6\( \lambda \)
  - Implies minimum of 12\( \lambda \) between opposite transistor flavors
  - Leaves room for one wire track “for free”
First Cut Area Estimation

- Estimate area by counting required metal wiring tracks
  - Multiply by 8 to express in $\lambda$
  - Where does the “8” come from?

Example: NAND3

- Horizontal n-active and p-active strips
- Vertical polysilicon gates
- Metal1 $V_{DD}$ rail at top
- Metal1 GND/$V_{SS}$ rail at bottom
- $32 \lambda$ by $40 \lambda$
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C)D \]
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C)D \]

Another Example Question 1.17

- Consider \( F = \overline{(A+B)(C+D)} \)
  - Sketch transistors
  - Sketch stick diagram
  - Estimate area
## Typical Layout Densities (Table 1.10)

<table>
<thead>
<tr>
<th>Element</th>
<th>Area (in $\lambda^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Logic</td>
<td>1000-1500/transistor</td>
</tr>
<tr>
<td>Datapath</td>
<td>250-750/transistor</td>
</tr>
<tr>
<td>SRAM</td>
<td>1000/bit</td>
</tr>
<tr>
<td>DRAM</td>
<td>100/bit</td>
</tr>
<tr>
<td>ROM</td>
<td>100/bit</td>
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</tbody>
</table>