Exam 2 Topics: You should be able to:

- From the intro to FET operation (W&H Chap. 2)
  - (2.1) MOS voltages: $V_{gs}$, $V_{ds}$, $V_{t}$, $V_{sat}$, $I_{ds}$, $I_{sat}$ and where measured in pMOS vs nMOS circuits
  - (2.2) Use the long channel model to compute the IV curves for a transistor
  - (2.3.1) MOS capacitance and resistance and how they change with changes to $W$, $L$, $tox$
  - Identify the different regions (cutoff, linear, and saturation) of a transistor’s IV curves, and what that means in terms of current flow in the channel
  - Compute $\beta$ from either physical parameters or I-V curves
  - Compute $C_{ox}$ from the process characteristics
  - Find, either graphically or thru the model, $V_{sat}$, $I_{sat}$
  - Understand the differences in characteristics between an N and P type (esp. mobility and width) and how that affects their IV curves.
  - Computing $V_{gs}$ in real circuits where the transistor’s source is not ground
  - Load lines: be able to find voltages and currents in simple circuits
    - Transistor + resistor
    - 2 transistors (same type) in series
    - Inverter (2 transistors of different types)
  - (2.4) Real World effects:
    - Velocity saturation
    - Channel Length Modulation, including computing $\lambda$
    - Body Effect

- Memory Array Structures: W&H 12.1-12.4, 12.6-12.7
  - What are the different kinds of memory: read-only/read-write/read-mostly, volatile/non-volatile, random-access/block-oriented/content-addressable
  - What are the major logic blocks in an array structure: row decoder, array, sense amps, column decoder
  - Implementing a row decoder
  - What are major wires thru an array and how do they interact with a bit cell: word lines, bit-columns
  - Different cell types: ROM, DRAM, SRAM, including transistor diagrams.
  - Programming a ROM (dot diagram)

- Delay: Chap. 4.1-4.3, 4.4.1-4.4.3
  - (141) Definitions of delay
  - (147) Identifying diffusion capacitance in a circuit
  - (146) Relationship of $R$ and $C$ values with transistor widths
  - (147) Drawing equivalent RC circuits for rise and fall times
  - (152) Definition of “Fan out of $h$”
  - (154) Determining Effective Resistance
  - (150) Drawing and using Elmore model to compute delay estimate
  - Determining combination of input transitions that maximize/minimize a logic gate’s delay