Introduction to CMOS VLSI Design

MOSFETs Lecture B

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Fall 2015, 2018

Based on material from
Prof. Jay Brockman, Joseph Nahas: University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- **Lecture A**
  - IEEE Notation and IV curves
  - MOS Gate
  - Water Model
  - nMOS Ideal Long Channel I-V Model
  - Supplementary Material – More Careful Computation

- **Lecture B**
  - Reading the I-V Curves
  - Sample Technologies
  - Load Lines and an NMOS Inverter
  - A CMOS Inverter

- **Lecture C**
  - DC Transfer Curves for an Inverter
  - Ideal vs Real
  - Real-World Effects
Reading the IV Curve

Summary: Long Channel Model

William Shockley 1st order transistor models
1952 A Unipolar Field Effect Transistor

\[
I_{ds} = \begin{cases} 
0, & V_{gs} \leq V_t, \text{Cutoff} \\
\beta(V_{GT} - V_{ds}/2) \cdot V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\
\beta V_{GT}^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} 
\end{cases}
\]

Where:
- \( C_{ox} = \epsilon_{ox} / t_{ox} \)
- \( \beta = (\epsilon_{ox} \cdot \mu / t_{ox}) \cdot (W/L) = C_{ox} \cdot \mu \cdot W/L \)
- \( V_{GT} = V_{gs} - V_t \)
- \( V_{dsat} = V_{GT} \)

[Diagram of MOSFET with parameters labeled]
FIGURE 2.16 Comparison of \( \alpha \)-power law model with simulated transistor behavior.

pMOS Curve is in Opposite Quadrant

Characteristic Curves for pMOSFET

http://www.physics.csbsju.edu/trace/ipMOSFET5.plot.gif
Reading The Graph

<table>
<thead>
<tr>
<th>Vgs(V)</th>
<th>Vds(V)</th>
<th>Ids(uA)</th>
<th>Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0</td>
<td></td>
<td>?</td>
</tr>
<tr>
<td>0.8</td>
<td>0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>0.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8</td>
<td>650</td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td>0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

• $\beta = 242$
• $V_t = 0.7$

Understanding The I-V Graph: Fixed $V_{gs}$

- AMI 600nm example
  - $t_{ox} = 100 \text{ Å} = 10 \text{ nm}$
  - $\mu = 350 \text{ cm}^2/\text{V} \cdot \text{s}$
  - $V_t = 0.7 \text{ V}$
- If we fix $V_{gs}$, the device looks like a non-linear resistor
  - E.g. $V_{gs} = 4 \text{ V}$
  - In saturated region: $\approx 1.25 \text{ mA}$ constant current
  - In linear region: $\approx 2.5V/0.00125 \text{ mA} = 2K\Omega$
Let's Check the Equation:  
**Fixed** $V_{gs}$

\[
I_{ds} = \begin{cases} 
0, & V_{gs} < V_t \text{ Cutoff} \\
\beta(V_{gs} - V_t - V_{ds}/2) \cdot V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\
(-\beta/2)\cdot V_{ds}^2 + \beta(V_{gs} - V_t) \cdot V_{ds}, & V_{ds} > V_{dsat} \text{ Saturation} \\
\beta((V_{gs} - V_t)^2)/2, & V_{ds} > V_{dsat} \text{ Saturation} \\
\end{cases}
\]

Understanding The I-V Graph:  
**Fixed** $V_{ds}$

- Same technology as before
- If we fix $V_{ds}$, then $I_{ds}$ is a function of $V_{gs}$

<table>
<thead>
<tr>
<th>$V_{gs}$ (V)</th>
<th>0</th>
<th>0.5</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
<th>3</th>
<th>3.5</th>
<th>4</th>
<th>4.5</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ds}$ (uA)</td>
<td>0</td>
<td>0</td>
<td>11</td>
<td>77</td>
<td>204</td>
<td>391</td>
<td>628</td>
<td>870</td>
<td>1111</td>
<td>1353</td>
<td>1595</td>
</tr>
</tbody>
</table>

Interesting Region: almost linear voltage to current conversion
Let’s Check the Equation:
Fixed $V_{ds}$

$$I_{ds} = \begin{cases} 
0, & V_{gs} < V_t \text{ Cutoff} \\
\beta(V_{gs} - V_t - V_{ds}/2)V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\
\beta((V_{gs} - V_t)^2/2), & V_{ds} > V_{dsat} \text{ Saturation} \\
= (\beta/2)V_{gs}^2 - (\beta V_t)V_{gs} + (\beta/2)V_t^2 
\end{cases}$$

Knobs for Designers to Change

- Typically logic designer has no control over
  - $\varepsilon_{ox}$: thin ox permittivity
  - $t_{ox}$: thickness of oxide
  - $\mu$: mobility
  - $V_t$: threshold voltage

- Only knobs left to change
  - Overall $V_{dd}$: but usually selected at system level
  - $L$: length – but there is a minimum ($2\lambda$)

- $W$: width
Example: Doubling W Approximately Doubles Current

Sample Technologies
Approximating the ND Process

- $L = 2000\text{nm}$
- $W/L = 10$
- $t_{ox} = 2\text{Å} = 20\text{nm}$
- $\mu = 350\text{cm}^2/\text{V}\cdot\text{s}$
- $V_t = 0.5\text{V}$
- $\varepsilon_r = 3.9$

Real devices seem to have extra “Source Resistance” of about 120 ohms. Explains the difference.

600nm AMI Semiconductor

- $t_{ox} = 100\text{Å} = 10\text{nm}$
- $\mu = 350\text{cm}^2/\text{V}\cdot\text{s}$
- $V_t = 0.7\text{V}$
- $\varepsilon_r = 3.9$
- $\varepsilon_0 = 8.85\cdot10^{-14}\text{F/cm}$
- $W/L = 4/2$

$$\beta = \frac{\mu W}{t_{ox}} = \frac{350 \cdot 8.85 \cdot 10^{-14}}{10 \cdot 10^{-3}} \frac{W}{L} = 120 \frac{W}{L} \left( \frac{\mu A}{V^2} \right)$$
180 nm NMOS Characteristics

\[ I_{d} = 0.24 \left( V_{gs} - V_{t} \right)^2 \left( \frac{m_{A}}{V_{T}} \right) \]

- **Vgs = 5 V**
- **Vgs = 4 V**
- **Vgs = 3 V**
- **Vgs = 2 V**
- **Vgs = 1 V**

- \( I_{ds} (mA) \)
- \( V_{ds} (V) \)

180 nm pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility \( \mu_p \) is determined by holes
  - Typically 2-3x lower than that of electrons \( \mu_n \)
  - 120 cm²/Vs in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume \( \frac{\mu_n}{\mu_p} = 2 \)
The 65nm Process from p.67

- $t_{ox} = 10.5 \text{ Å} = 1.05 \text{ nm}$
- $\mu_N = 80 \text{ cm}^2/\text{V}\cdot\text{s}$;
- $V_t = 0.3 \text{ V}$
- $W/L = 2$
- $\varepsilon_r = 3.9$

Load Lines and An NMOS Inverter
An NMOS and a Resistor

- Basic Resistor: $V_R = R \cdot I_R$
- But in the Circuit:
  - $I_d = I_R$
  - $V_R = V_{DD} - V_{ds}$
- Thus: $I_d = \frac{(V_{DD} - V_{ds})}{R}$

$V_{ds}$ $I_d$ $V_{dd}/R$

$\text{Id}$, $V_{ds}$ MUST be on this line, Regardless of $V_{gs}$

Finding The Circuit I-V

To compute how circuit responds:
- Overlay resistor on transistor IV
- For each $V_{gs}$, find intersection

<table>
<thead>
<tr>
<th>$V_{gs}$</th>
<th>$I_d$ (uA)</th>
<th>$V_{ds}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>11</td>
<td>4.978</td>
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<td>1.5</td>
<td>77</td>
<td>4.846</td>
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<td>2</td>
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<td>4.5</td>
<td>1400</td>
<td>2.2</td>
</tr>
<tr>
<td>5</td>
<td>1550</td>
<td>1.9</td>
</tr>
</tbody>
</table>

NMOS Device with R Pullup

R=2000 Ω
What is interesting about $V_{gs}$, $V_{ds} = 2.5V$?

R = $V_{dd}/(2I_{ds})$

$V_{gs}$ | $V_{ds}$ | Ids (uA) |
--- | --- | --- |
0   | 5   | 0.7  |
5   | 0.7 | 5    |

R = 6.4K

2.5V/391nA = 6.4K

R = 1.5K

R = 25K

Picking a Resistor Value
What Is the $V_{gs} = “1”$ Current?

This represents a static power of ~3mW for just one gate!

A CMOS Inverter
Now We Have 2 Transistors: Questions

- Do we need load lines to determine output voltages if input is:
  - Either “0” (Ground)
  - Or “1” (Vdd)?
- Is there any static power if input is either “0” or “1”? Why then do we care about size (W/L) of each transistor?

A CMOS Inverter in Context

- Downstream circuits look like a capacitor on inverter output:
  - All connected transistor gates
  - Wiring
  - Other (addressed later)
- Thus Y looks like RC circuit:
  - With P-type the “pull-up” R
  - And N-type the “pull-down” R
- To make rise and fall times approximately symmetric:
  - Want $I_{dsat}$ of N & P types to be equal
Let's Look at the Equations

- $V_{dd} = V_{gsp} - V_{gsn}$
- $V_{dd} = V_{dsn} - V_{dsp}$
- To make currents equal: $I_{dp} = -I_{dn}$

Let's Connect the N and P I-V Curves

Tough to find where equations satisfied.
To Match Equations: Flip P-type IV and Move Right

- Above is for identically sized N and P transistors
- Remember: N and P mobility different

What If We Make P type Wider by Same Factor as Mobility Difference
Rule of Thumb

- To equalize currents, make average $I_{dsat}$ for Pull-Down and Pull Up networks equal
- Average difference in mobility is ~2
- Thus for inverter:
  - Make P-type twice as wide as N