Introduction to CMOS VLSI Design

MOSFETs Lecture B

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Based on material from
Prof. Jay Brockman, Joseph Nahas: University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- Lecture A
  - IEEE Notation and IV curves
  - MOS Gate
  - Water Model
  - nMOS Ideal Long Channel I-V Model
  - Supplementary Material – More Careful Computation
- *Lecture B*
  - *Reading the I-V Curves*
  - *Sample Technologies*
  - *Load Lines and an NMOS Inverter*
  - *A CMOS Inverter*
- Lecture C
  - DC Transfer Curves for an Inverter
  - Ideal vs Real
  - Real-World Effects

Reading the IV Curve

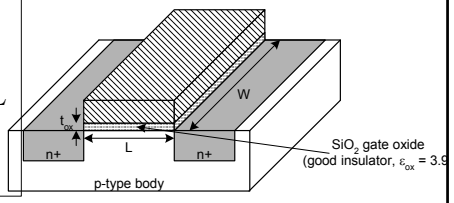
Summary: Long Channel Model

William Shockley 1st order transistor models
1952 *A Unipolar Field Effect Transistor*

$$I_{ds} = \begin{cases} 0, & V_{gs} < V_t \text{ Cutoff} \\ \beta(V_{GT} - V_{ds}/2)*V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\ \beta V_{GT}^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} \end{cases}$$

Where:

- $C_{ox} = \varepsilon_{ox} / t_{ox}$
- $\beta = (\varepsilon_{ox}*\mu/t_{ox})*(W/L) = C_{ox}*\mu*W/L$
- $V_{GT} = V_{gs} - V_t$
- $V_{dsat} = V_{GT}$



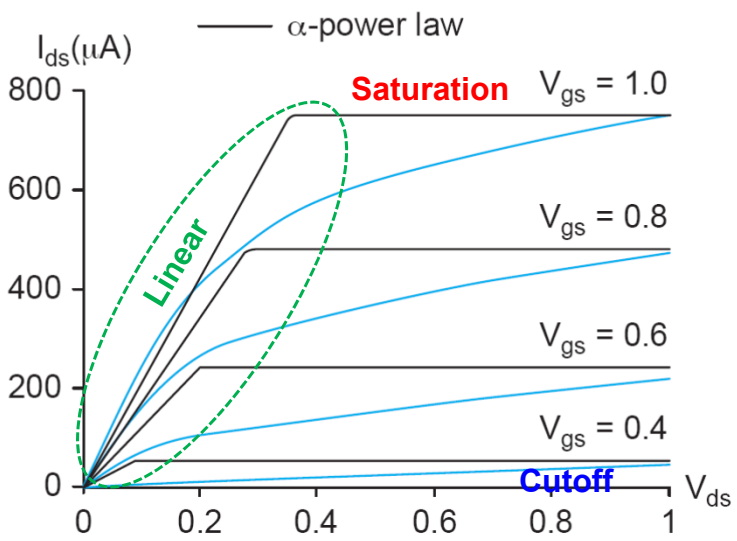
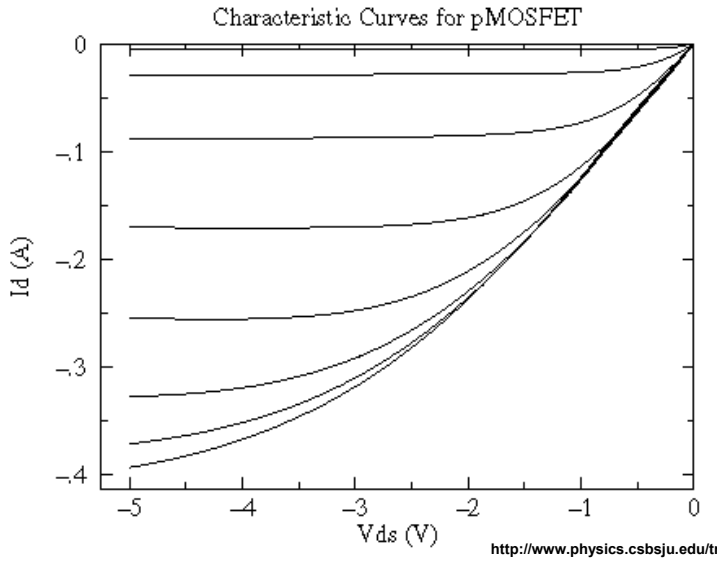


FIGURE 2.16 Comparison of α-power law model with simulated transistor behavior

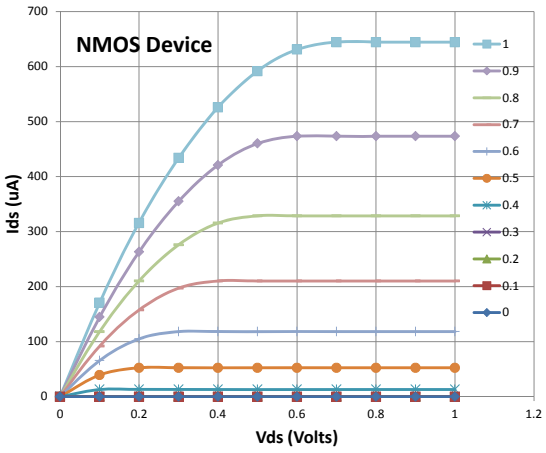
pMOS Curve is in Opposite Quadrant



http://www.physics.csbsju.edu/trace/i/pMOSFET5.plot.gif

Reading The Graph

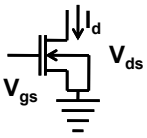
Vgs(V)	Vds(V)	Ids(uA)	Region ?
0.8	0		
0.8	0.2		
0.8	0.4		
0.8	0.6		
0.8	1		
	0.8	650	
	0.8	110	
0.1	0.2		
0.1	1		

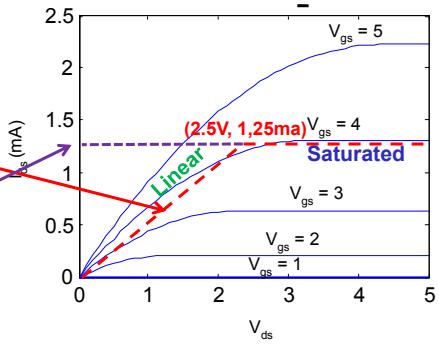


- β = 242
- V_t = 0.7

Understanding The I-V Graph: Fixed V_{gs}

- AMI 600nm example
  - t_{ox} = 100 Å = 10 nm
  - μ = 350 $cm^2/V*s$
  - V_t = 0.7 V
- If we fix V_{gs}, the device looks like a non-linear resistor
  - E.g. V_{gs} = 4V
  - In saturated region: ~ 1.25ma constant current
  - In linear region: ~2.5V/0.00125 ma = 2KΩ





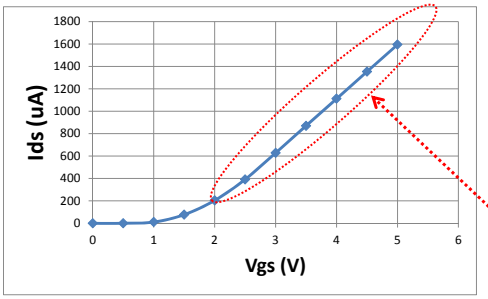
Let's Check the Equation: Fixed V_{gs}

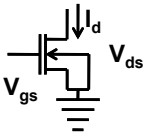
$$I_{ds} = \begin{cases} 0, & V_{gs} < V_t \text{ Cutoff} \\ \beta(V_{gs} - V_t - V_{ds}/2)*V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\ = (-\beta/2)* V_{ds}^2 + \beta(V_{gs} - V_t) *V_{ds} & \\ = -121*V_{ds}^2 + (242V_{gs} - 169) *V_{ds} & \\ \beta((V_{gs} - V_t)^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} \\ = \text{a constant} & \end{cases}$$

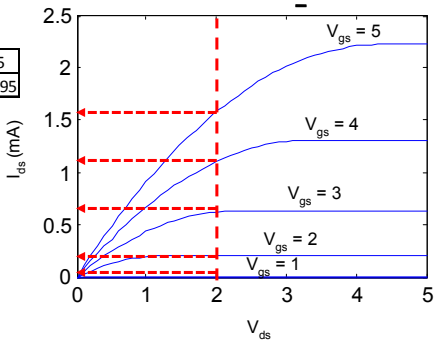
Understanding The I-V Graph: Fixed V_{ds}

- Same technology as before
- If we fix V_{ds}, then I_{ds} is a function of V_{gs}

Vgs (V):	0	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5
Ids (uA):	0	0	11	77	204	391	628	870	1111	1353	1595







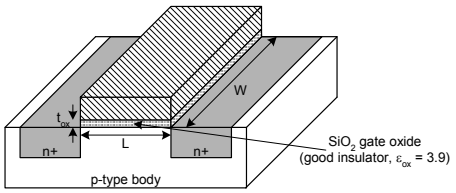
Interesting Region: almost linear voltage to current conversion

Let's Check the Equation: Fixed V_{ds}

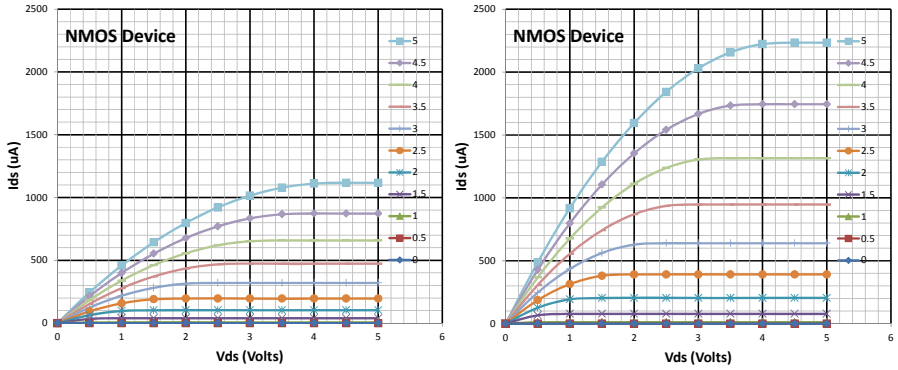
$$I_{ds} = \begin{cases} 0, & V_{gs} < V_t \text{ Cutoff} \\ \beta(V_{gs} - V_t - V_{ds}/2)*V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\ = (\beta * V_{ds})*V_{gs} - (V_t + V_{ds}/2)*V_{ds} & \\ \beta((V_{gs} - V_t)^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} \\ = (\beta/2)V_{gs}^2 - (\beta V_t) V_{gs} + (\beta/2)V_t^2 & \end{cases}$$

Knobs for Designers to Change

- Typically logic designer has no control over
  - ε_{ox} : thin ox permittivity
  - t_{ox}: thickness of oxide
  - μ: mobility
  - V_t : threshold voltage
- Only knobs left to change
  - Overall V_{dd}: but usually selected at system level
  - L: length – but there is a *minimum* (2λ)
  - **W: width**



Example: Doubling W Approximately Doubles Current



W = Length

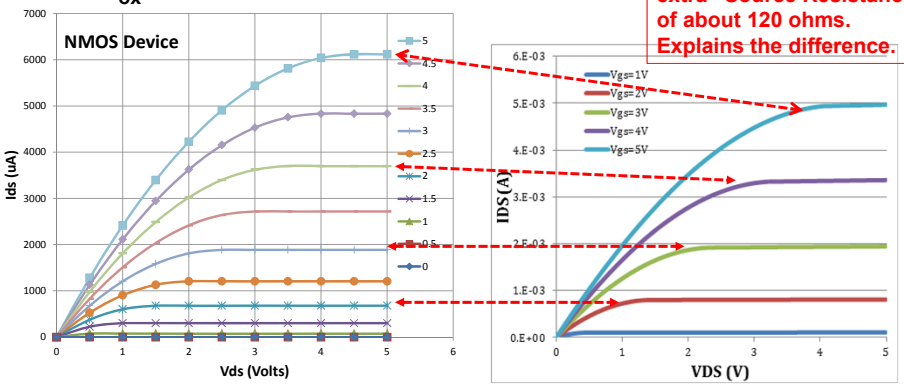
W = 2* Length

Sample Technologies

Approximating the ND Process

- L = 2000nm
- W/L = 10
- t_{ox} = 2Å = 20 nm
- μ = 350 $cm^2/V*s$
- V_t = 0.5 V
- ε_r = 3.9

Real devices seem to have extra "Source Resistance" of about 120 ohms. Explains the difference.

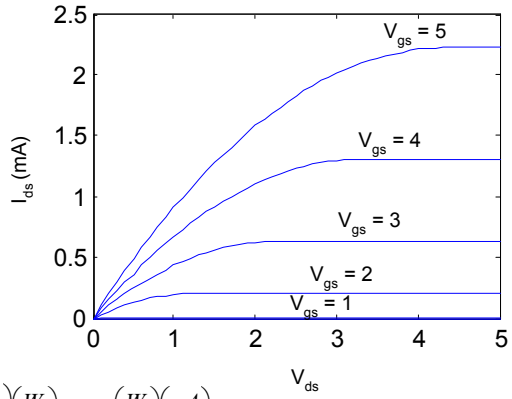


The Model Output

Spice Run from Prof. Snider

600nm AMI Semiconductor

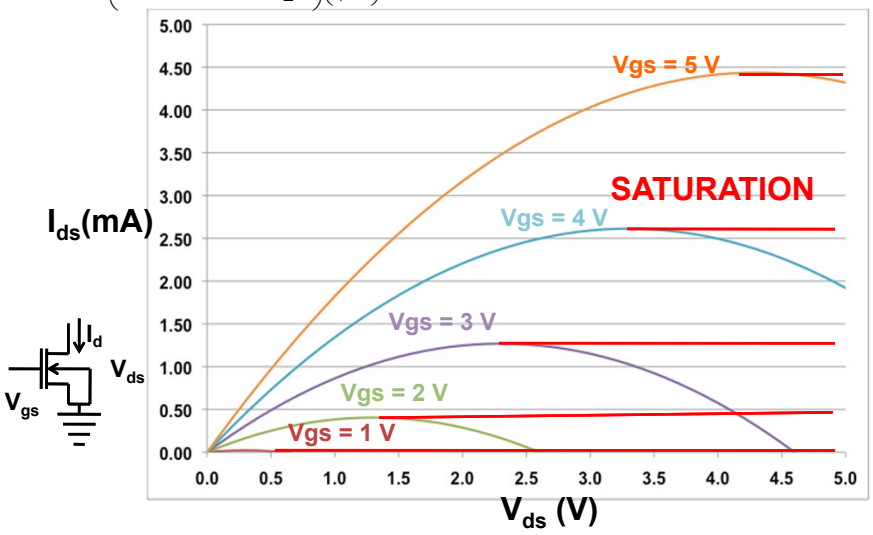
- t_{ox} = 100 Å = 10 nm
- μ = 350 $cm^2/V*s$
- V_t = 0.7 V
- ε_r = 3.9
- ε_0 = 8.85·10^{-14} F/cm
- W/L = 4/2



$$\beta = \frac{\mu\varepsilon W}{t_{ox}L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{10 \cdot 10^{-7}}\right)\left(\frac{W}{L}\right) = 120\left(\frac{W}{L}\right)\left(\frac{\mu A}{V^2}\right)$$

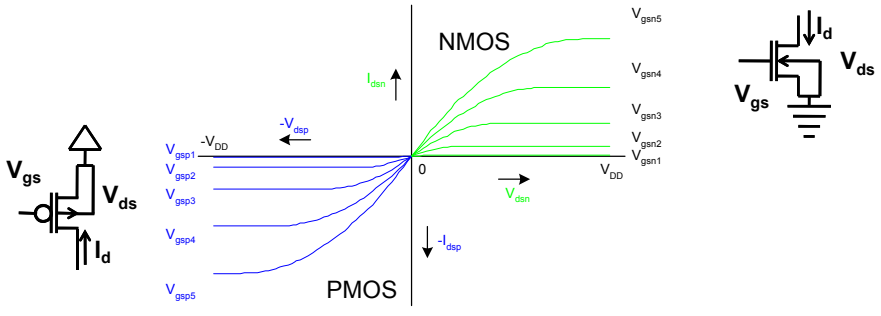
180 nm NMOS Characteristics

$$I_{ds} = 0.24\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]\left(\frac{mA}{V^2}\right)$$



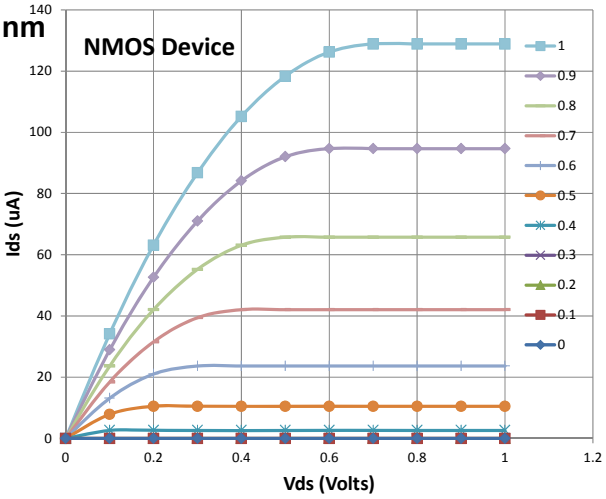
180 nm pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 cm²/V*s in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$



The 65nm Process from p.67

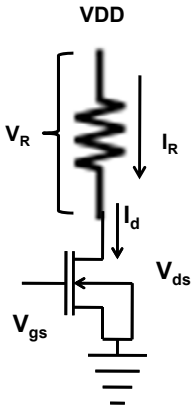
- t_{ox} = 10.5 Å = 1.05 nm
- μ_N = 80 cm²/V*s;
- V_t = 0.3 V
- W/L = 2
- ε_r = 3.9

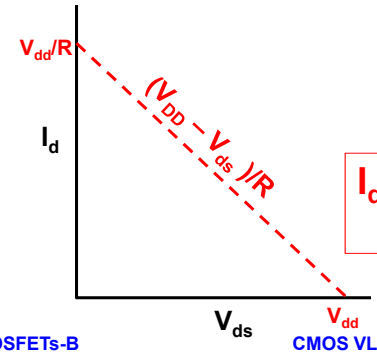


Load Lines and An NMOS Inverter

An NMOS and a Resistor

- Basic Resistor: $V_R = R*I_R$
- But in the Circuit:
  - $I_d = I_R$
  - $V_R = V_{DD} - V_{ds}$
- **Thus: $I_d = (V_{DD} - V_{ds})/R$**



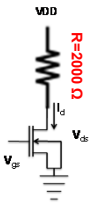


I_d, V_{ds} MUST be on this line, Regardless of V_{gs}

Finding The Circuit I-V

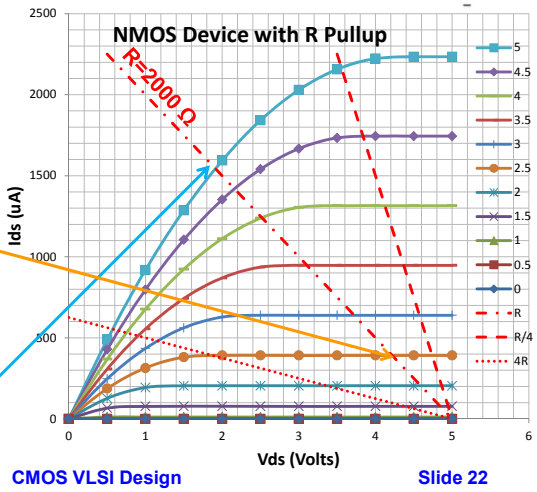
To compute how circuit responds:

- Overlay resistor on transistor IV
- For each V_{gs}, find intersection

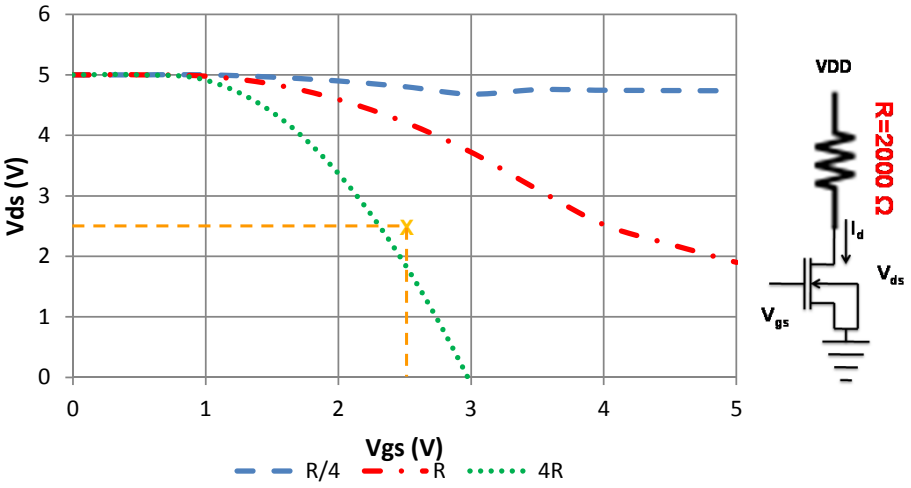


R=2000 Ω

Vgs	Ids (uA)	Vds (V)
0	0	5
0.5	0	5
1	11	4.978
1.5	77	4.846
2	204	4.592
2.5	391	4.218
3	639	3.722
3.5	947	3.106
4	1238	2.524
4.5	1400	2.2
5	1550	1.9



Plotting The Results

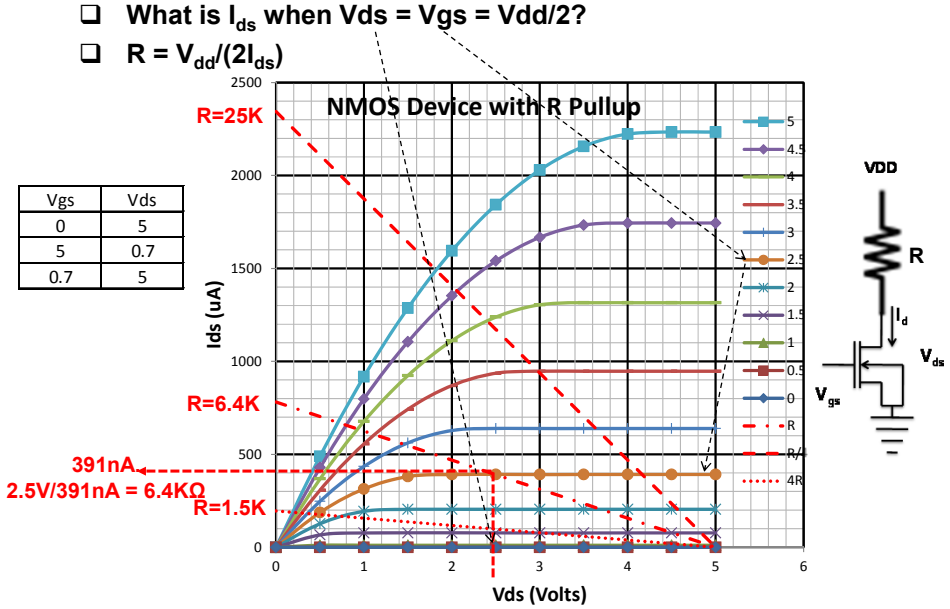


What is interesting about V_{gs}, V_{ds} = 2.5V?

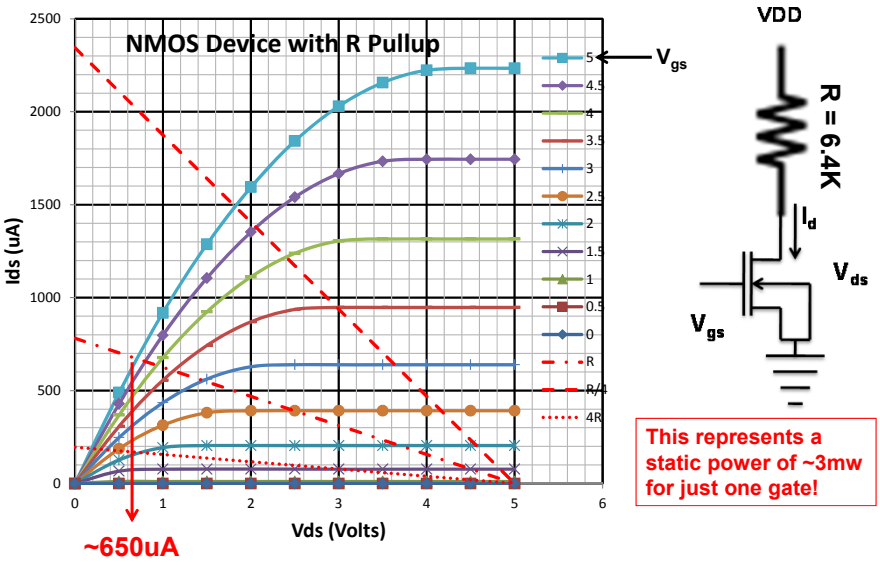
Picking a Resistor Value

- What is I_{ds} when Vds = Vgs = Vdd/2?
- $R = V_{dd}/(2I_{ds})$

Vgs	Vds
0	5
5	0.7
0.7	5



What Is the Vgs = “1” Current?

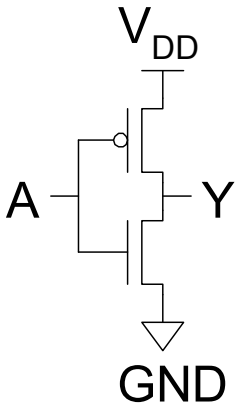


This represents a static power of ~3mw for just one gate!

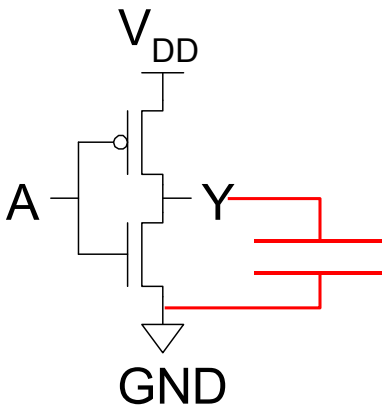
A CMOS Inverter

Now We Have 2 Transistors: Questions

- Do we need load lines to determine output voltages if input is
  - Either "0" (Ground)
  - Or "1" (Vdd)?
- Is there any static power if input is either "0" or "1"?
- Why then do we care about size (W/L) of each transistor?

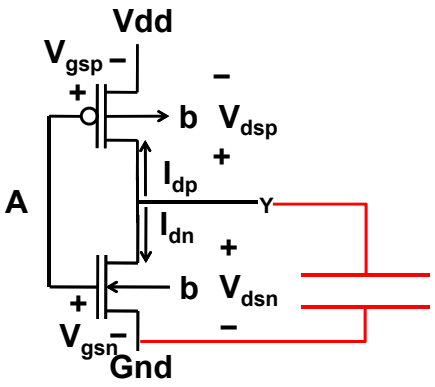


A CMOS Inverter in Context



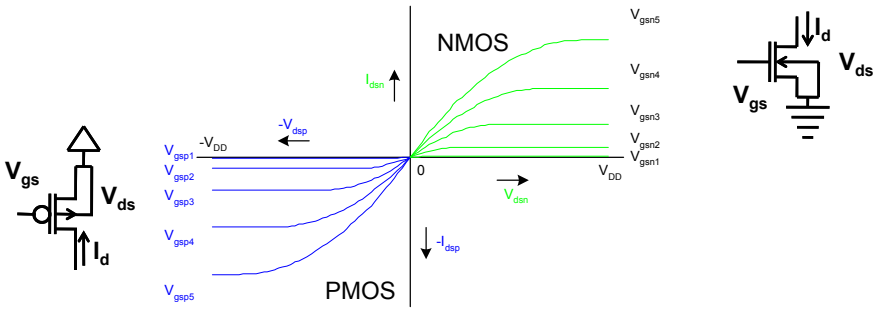
- Downstream circuits look like a capacitor on inverter output
  - All connected transistor gates
  - Wiring
  - Other (addressed later)
- Thus Y looks like RC circuit
  - With P-type the "pull-up" R
  - And N-type the "pull-down" R
- To make rise and fall times approximately symmetric:
  - Want I_{dsat} of N & P types to be equal

Let's Look at the Equations



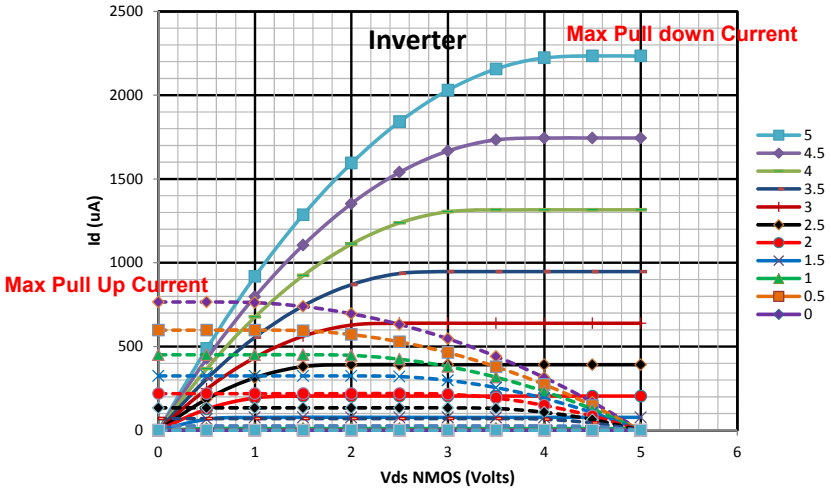
- $V_{dd} = V_{gsp} - V_{gsn}$
- $V_{dd} = V_{dsn} - V_{dsp}$
- To make currents equal: $I_{dp} = -I_{dn}$

Let's Connect the N and P I-V Curves



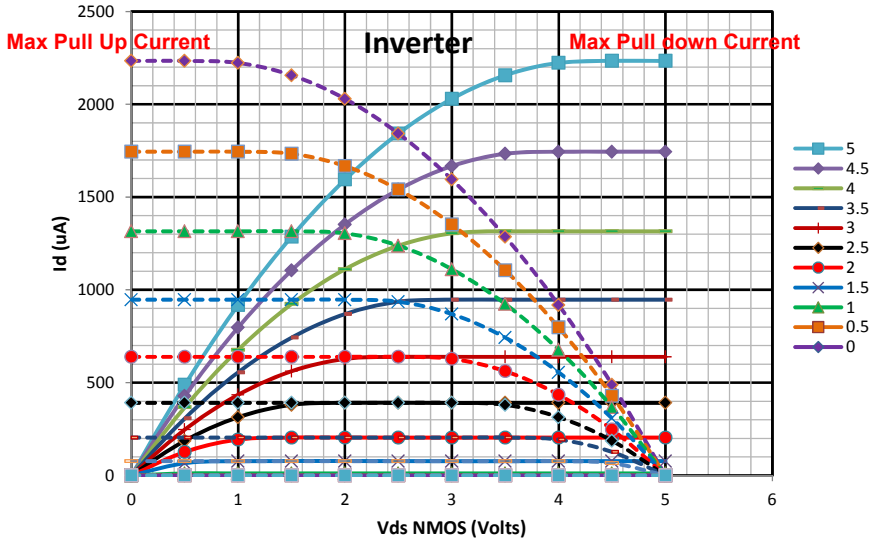
Tough to find where equations satisfied.

To Match Equations: Flip P-type IV and Move Right



- Above is for identically sized N and P transistors
- Remember: N and P mobility <u>different</u>

What If We Make P type Wider by Same Factor as Mobility Difference



Rule of Thumb

- To equalize currents, make average I_{dsat} for Pull-Down and Pull Up networks equal
- Average difference in mobility is ~2
- Thus for invertor:
  - Make P-type twice as wide as N