Introduction to CMOS VLSI Design

MOSFETs Lecture 3: Real World Effects

Peter Kogge
University of Notre Dame
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Based on material from
Prof. Jay Brockman, Joseph Nahas: University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- Lecture A
  - IEEE Notation and IV curves
  - MOS Gate
  - Water Model
  - nMOS Ideal Long Channel I-V Model
  - Supplementary Material – More Careful Computation
- Lecture B
  - Reading the I-V Curves
  - Sample Technologies
  - Load Lines and an NMOS Inverter
  - A CMOS Inverter
- Lecture C
  - DC Transfer Curves for an Inverter
  - Ideal vs Real
  - Real-World Effects
Summary: Long Channel Model

William Shockley 1st order transistor models
1952 A Unipolar Field Effect Transistor

\[ I_{ds} = \begin{cases} 
0, & V_{gs} < V_t \text{ Cutoff} \\
\beta(V_{GT} - V_{ds}/2)^*V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\
\beta V_{GT}^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} 
\end{cases} \]

Where:
- \( C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \)
- \( \beta = (\varepsilon_{ox} \mu_{ox})^*W/L = C_{ox} \mu^*W/L \)
- \( V_{GT} = V_{gs} - V_t \)
- \( V_{dsat} = V_{GT} \)

DC Transfer Characteristics
“Perfect” digital circuits have I/O = 0V or \( V_{dd} \)

What if \( V_{in} \) between 0 and \( V_{dd} \)? What is \( V_{out} \)?

Assume \( \beta \)s same for N and P (P is wider)

Approach:
- Overlay IV curves as before
- For each \( V_{GS} = V_{in} \), follow P and N curves until they intersect
- Record the \( I_{ds} \) and \( V_{ds} \)

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**From The Book (Fig. 2.26)**

<table>
<thead>
<tr>
<th>Region</th>
<th>Input</th>
<th>P</th>
<th>N</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>( 0 &lt; V_{in} &lt; V_{th} )</td>
<td>Saturated</td>
<td>Cutoff</td>
<td>( V_{dd} )</td>
</tr>
<tr>
<td>B</td>
<td>( V_{th} &lt; V_{in} &lt; V_{dd}/2 )</td>
<td>Saturated</td>
<td>Linear</td>
<td>( &gt;V_{dd}/2 )</td>
</tr>
<tr>
<td>C</td>
<td>( V_{in} \approx V_{dd}/2 )</td>
<td>Linear</td>
<td>Linear</td>
<td>Drops sharply</td>
</tr>
<tr>
<td>D</td>
<td>( V_{dd}/2 &lt; V_{in} &lt; V_{dd}-</td>
<td>V_{tp}</td>
<td>)</td>
<td>Linear</td>
</tr>
<tr>
<td>E</td>
<td>( V_{in} &gt; V_{dd} -</td>
<td>V_{tp}</td>
<td>)</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>
Let's Do It

<table>
<thead>
<tr>
<th>Vin</th>
<th>Ids (uA)</th>
<th>Vds (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1.5</td>
<td>80</td>
<td>4.8</td>
</tr>
<tr>
<td>2</td>
<td>200</td>
<td>4.6</td>
</tr>
<tr>
<td>2.5</td>
<td>400</td>
<td>2.5</td>
</tr>
<tr>
<td>3</td>
<td>200</td>
<td>0.5</td>
</tr>
<tr>
<td>3.5</td>
<td>80</td>
<td>0.2</td>
</tr>
<tr>
<td>4.0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5.0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Graphing This

<table>
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<th>P</th>
<th>N</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0 &lt; Vin &lt; Vtn</td>
<td>Linear</td>
<td>Cutoff</td>
<td>Vdd</td>
</tr>
<tr>
<td>B</td>
<td>Vtn &lt; Vin &lt; Vdd/2</td>
<td>Linear</td>
<td>Saturated</td>
<td>&gt;Vdd/2</td>
</tr>
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<td>C</td>
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<td></td>
<td>Vtp</td>
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MOSFETs-C  CMOS VLSI Design  Slide 7

MOSFETs-C  CMOS VLSI Design  Slide 8
What If $\beta$s Not Same? (Fig. 2.28)

![Graph showing the relationship between $V_{in}$ and $V_{out}$ for different values of $\beta_p/\beta_n$.]

- $\beta_p = 0.1$
- $\beta_p = 1$
- $\beta_p = 2$
- $\beta_p = 10$

Noise Margin

- $V_{IH} = $ min high input voltage
- $V_{IL} = $ max low input voltage
- $V_{OH} = $ min high output voltage
- $V_{OL} = $ max low output voltage
- $NML = V_{IL} - V_{OL}$
- $NMH = V_{OH} - V_{IH}$

![Diagram illustrating noise margin with output characteristics and input characteristics.]

- Logical High Output Range
- Logical Low Output Range
- Logical High Input Range
- Logical Low Input Range
- Indeterminate Region
Pass Transistor Drops (Fig. 2.31)

(a) $V_{DD} \quad V_{DD} \quad V_s = V_{DD} - V_{in}$

(b) $V_s = |V_{gs}|$

(c) $V_{DD} \quad V_{DD} \quad V_{DD} \quad V_{DD} - V_{in}$

(d) $V_{DD} \quad V_{DD} - V_{in}$

Ideal vs Real
**Ideal nMOS I-V Plot**

- 180 nm TSMC process
- Ideal Models
  - $\beta = 155(W/L) \mu A/V^2$
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V

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**Ideal vs Real**

- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?

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**Ideal 180 nm nmos**

**Real Device (Spice Model)**
**What’s Different?**

- Less ON current
- No square law
- Current increases in saturation

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**Ideal 180 nm nmos**

![Ideal 180 nm nmos](image1)

**Real Device (Spice Model)**

![Real Device (Spice Model)](image2)

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**Lets Vary L and W With Constant W/L**

**0.18 um PMOS Characteristic**

![0.18 um PMOS Characteristic](image3)
Real World Effects
Modifications to Model

- Velocity Saturation
- Channel Length Modulation
- The Body Effect

Velocity Saturation

- We assumed carrier velocity is proportional to E-field
  - \( v = \mu E_{\text{lat}} = \mu V_{ds}/L \)

- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches \( v_{\text{sat}} \) at some \( E_{\text{lat}} = E_{\text{sat}} \)
    - Electrons: 6-10 \( \times 10^6 \) cm/s
    - Holes: 4-8 \( \times 10^6 \) cm/s
  - Better model

\[
\frac{v_{\text{sat}}}{v} = \mu \frac{E_{\text{lat}}}{E_{\text{lat}} + E_{\text{sat}}} \]

When \( E_{\text{lat}} \) is small, denominator \( \sim 1 \) and \( v \sim \mu E_{\text{lat}} \)

When \( E_{\text{lat}} \) is large

\[
\mu E_{\text{lat}} \quad \mu E_{\text{sat}} \quad \mu E_{\text{sat}} / 2
\]

Slope = \( \mu \)

Proportional

Velocity Saturated
### Vel Sat I-V Effects

- Ideal transistor ON current increases with $V_{DD}^2$
  \[ I_d = \mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T \right)^2 = \frac{\beta}{2} \left( V_{gs} - V_T \right)^2; \]

- Velocity-saturated ON current increases with only $V_{DD}$
  \[ I_d = C_{ox} W \left( V_{gs} - V_T \right) v_{max}; \]

- Result: lower currents than ideal model
- Real transistors are partially velocity saturated
  - Approximate with $\alpha$-power law model
  - $I_{ds} \propto V_{DD}^\alpha$
  - $1 < \alpha < 2$ determined empirically

### $\alpha$-Power Model

\[ I_d = \begin{cases} 
0 & V_g < V_T \text{ cutoff} \\
\frac{V_{ds}}{V_{d_{sat}}} & V_{ds} < V_{d_{sat}} \text{ linear} \\
I_{d_{sat}} & V_{ds} > V_{d_{sat}} \text{ saturation} 
\end{cases} \]

\[ I_{d_{sat}} = P_v \frac{\beta}{2} \left( V_{gs} - V_T \right) \alpha; \]

\[ V_{d_{sat}} = P_v \left( V_{gs} - V_T \right)^{\alpha/2}; \]

Velocity Saturation compresses current characteristics.
Channel Length Modulation

- Reverse-biased p-n junctions form a depletion region
  - Region between n and p with no carriers
  - Width of depletion \( L_d \) region grows with reverse bias
  - \( L_{\text{eff}} = L - L_d \)
- Shorter \( L_{\text{eff}} \) gives more current
  - \( I_{ds} \) increases with \( V_{ds} \)
  - Even in saturation

\[ \lambda = \text{channel length modulation coefficient} \]
- not feature size
- Empirically fit to I-V characteristics

\[ I_d = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \]
- Compute as “slope” of curve in saturation = \( \Delta I / \Delta V \)
Body Effect

- $V_t$: gate voltage necessary to invert channel
- Increase if source-to-body voltage increases because source is connected not to ground but drain of another transistor
  - Effective source-to-body increases
- Increase in $V_t$ with $V_{SB}$ is called the body effect

![Diagram showing body effect](image)

$V_t$ of this transistor is “higher” because its source is not at ground

Body Effect Model

$$V_t = V_{t0} + \gamma \left( \sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

- $\phi_s$ = surface potential at threshold
  - $\phi_s = 2V_t \ln \frac{N_A}{n_i}$
  - Depends on doping level $N_A$
  - And intrinsic carrier concentration $n_i$
- $\gamma$ = body effect coefficient
  - $\gamma = \frac{t_{ox}}{C_{ox}} \sqrt{2q\varepsilon_i N_A}$
  - $\varepsilon_i = 1.45 \times 10^{10}$ cm$^{-3}$ for Silicon
  - $n_i = 1.45 \times 10^{10}$ cm$^{-3}$ for Silicon

$$\nu_T = \frac{kT}{q} = 26\text{mV} \text{ at } 300\text{K}$$

Key Point: transistors with source NOT at ground are harder to turn on.
Question

Assume
• One input changes only infrequently
• Other changes frequently
Which input drives which transistor for faster gate?

Ground