Introduction to CMOS VLSI Design

MOSFETs Lecture 3: Real World Effects

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Based on material from
Prof. Jay Brockman, Joseph Nahas: University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

- Lecture A
  - IEEE Notation and IV curves
  - MOS Gate
  - Water Model
  - nMOS Ideal Long Channel I-V Model
  - Supplementary Material – More Careful Computation
- Lecture B
  - Reading the I-V Curves
  - Sample Technologies
  - Load Lines and an NMOS Inverter
  - A CMOS Inverter
- *Lecture C*
  - *DC Transfer Curves for an Inverter*
  - *Ideal vs Real*
  - *Real-World Effects*

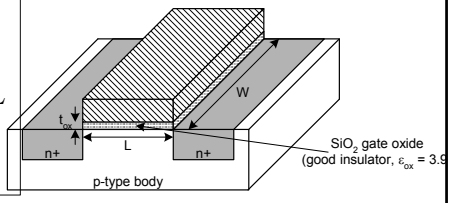
Summary: Long Channel Model

William Shockley 1st order transistor models
1952 *A Unipolar Field Effect Transistor*

$$I_{ds} = \begin{cases} 0, & V_{gs} < V_t \text{ Cutoff} \\ \beta(V_{GT} - V_{ds}/2)*V_{ds}, & V_{gs} > V_t \text{ and } V_{ds} < V_{dsat} \text{ Linear} \\ \beta V_{GT}^2 / 2, & V_{ds} > V_{dsat} \text{ Saturation} \end{cases}$$

Where:

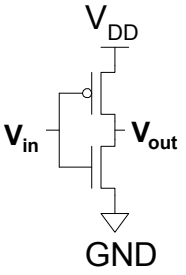
- $C_{ox} = \varepsilon_{ox} / t_{ox}$
- $\beta = (\varepsilon_{ox}*\mu/t_{ox})*(W/L) = C_{ox}*\mu*W/L$
- $V_{GT} = V_{gs} - V_t$
- $V_{dsat} = V_{GT}$

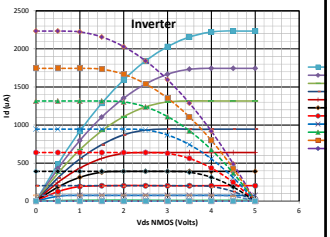


DC Transfer Characteristics

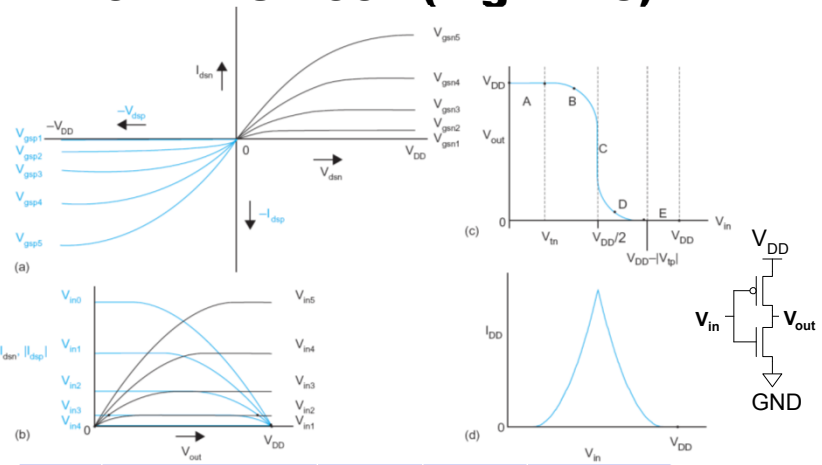
Static Inverter DC Characteristics

- "Perfect" digital circuits have I/O = 0V or V_{dd}
- What if V_{in} between 0 and Vdd? What is V_{out}?
- Assume βs same for N and P (P is wider)
- Approach:
  - Overlay IV curves as before
  - For each V_{GS} = V_{in}, follow P and N curves until they intersect
  - Record the I_{ds} and V_{ds}



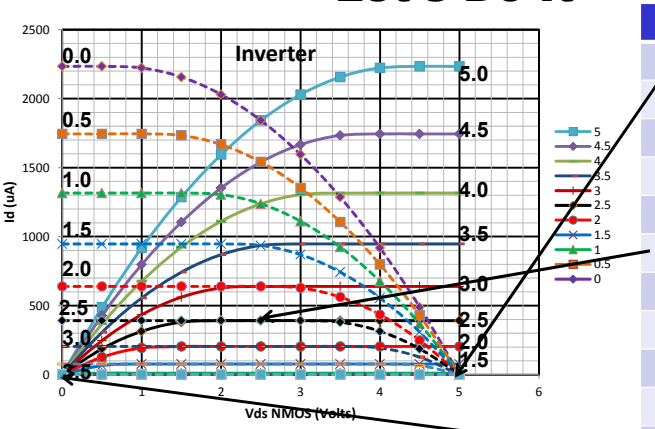


From The Book (Fig. 2.26)



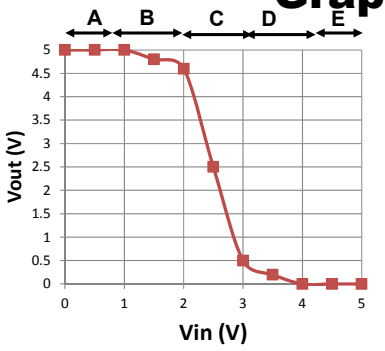
Region	Input	P	N	Output
A	$0 < V_{in} < V_{tn}$	Saturated	Cutoff	Vdd
B	$V_{tn} < V_{in} < Vdd/2$	Saturated	Linear	>Vdd/2
C	$V_{in} \sim Vdd/2$	Linear	Linear	Drops sharply
D	$Vdd/2 < V_{in} < Vdd-\|V_{tp}\|$	Linear	Saturated	<Vdd/2
E	$V_{in} > Vdd - \|V_{tp}\|$	Cutoff	Saturated	0

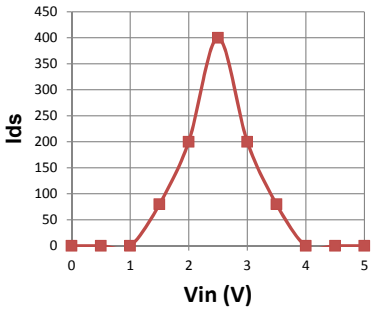
Let's Do It



Vin	Ids	Vds
0	0	5
0.5	0	5
1	0	5
1.5	80	4.8
2	200	4.6
2.5	400	2.5
3	200	0.5
3.5	80	0.2
4.0	0	0
4.5	0	0
5.0	0	0

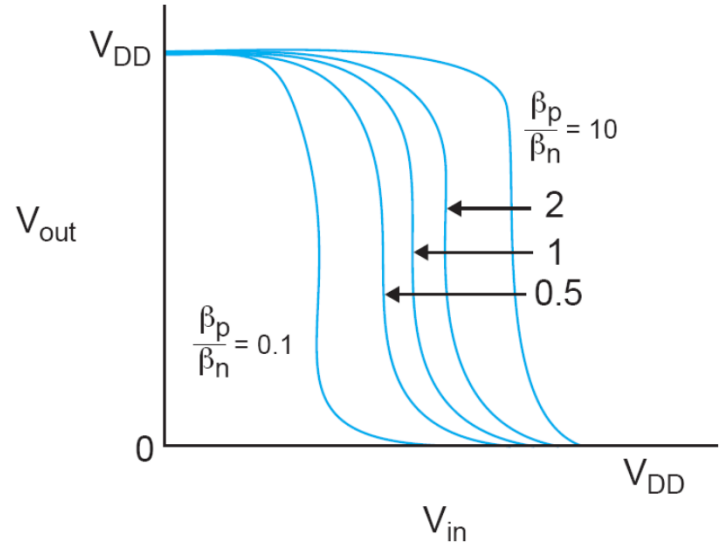
Graphing This



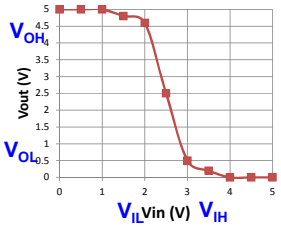


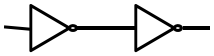
Region	Input	P	N	Output
A	0 < Vin < Vtn	Linear	Cutoff	Vdd
B	Vtn < Vin < Vdd/2	Linear	Saturated	>Vdd/2
C	Vin ~ Vdd/2	Saturated	Saturated	Drops sharply
D	Vdd/2 < Vin < Vdd-|Vtp|	Saturated	Linear	<Vdd/2
E	Vin > Vdd - |Vtp|	Cutoff	Linear	0

What If βs Not Same? (Fig. 2.28)

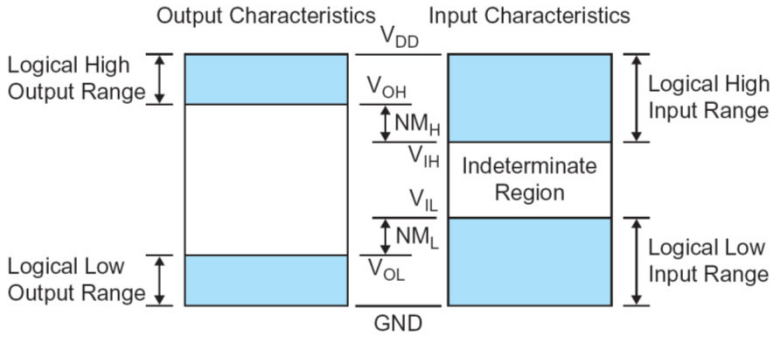


Noise Margin

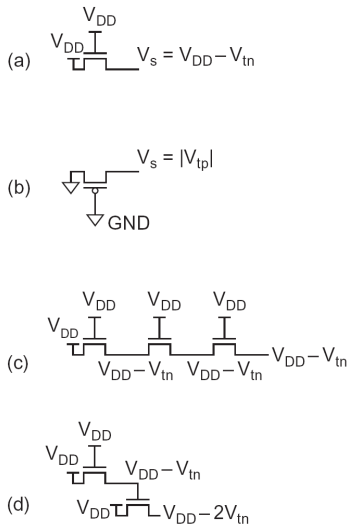




V_{IH} = min high input voltage
V_{IL} = max low input voltage
V_{OH} = min high output voltage
V_{OL} = max low input voltage
$NM_L = V_{IL} - V_{OL}$
$NM_H = V_{OH} - V_{IH}$



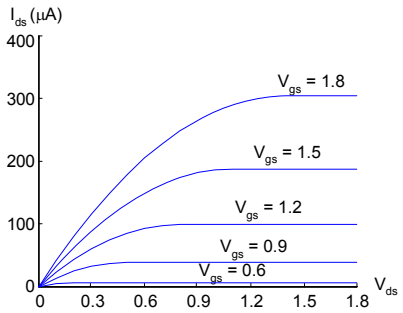
Pass Transistor Drops (Fig. 2.31)



Ideal vs Real

Ideal nMOS I-V Plot

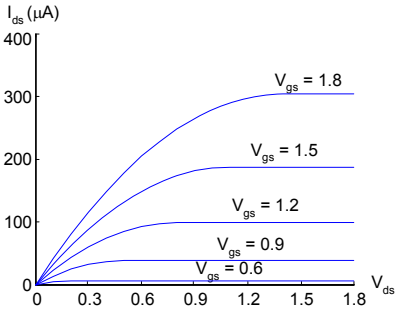
- 180 nm TSMC process
- Ideal Models
  - $\beta = 155(W/L)\ \mu A/V^2$
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V



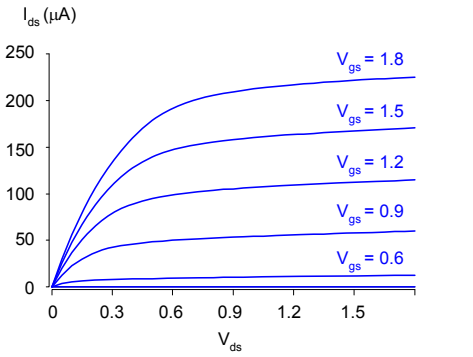
Ideal vs Real

- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?

Ideal 180 nm nmos



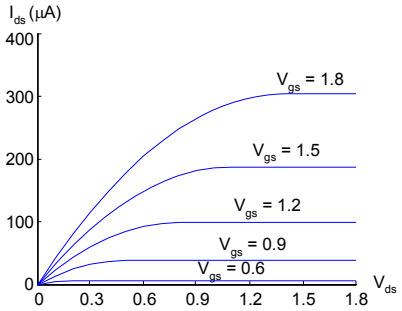
Real Device (Spice Model)



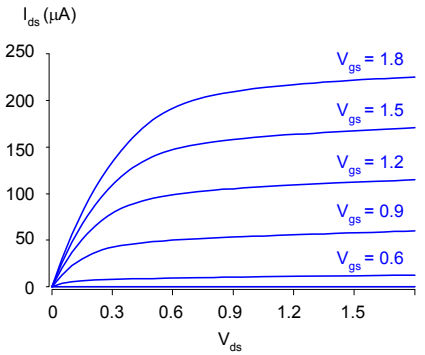
What's Different?

- ❑ Less ON current
- ❑ No square law
- ❑ Current increases in saturation

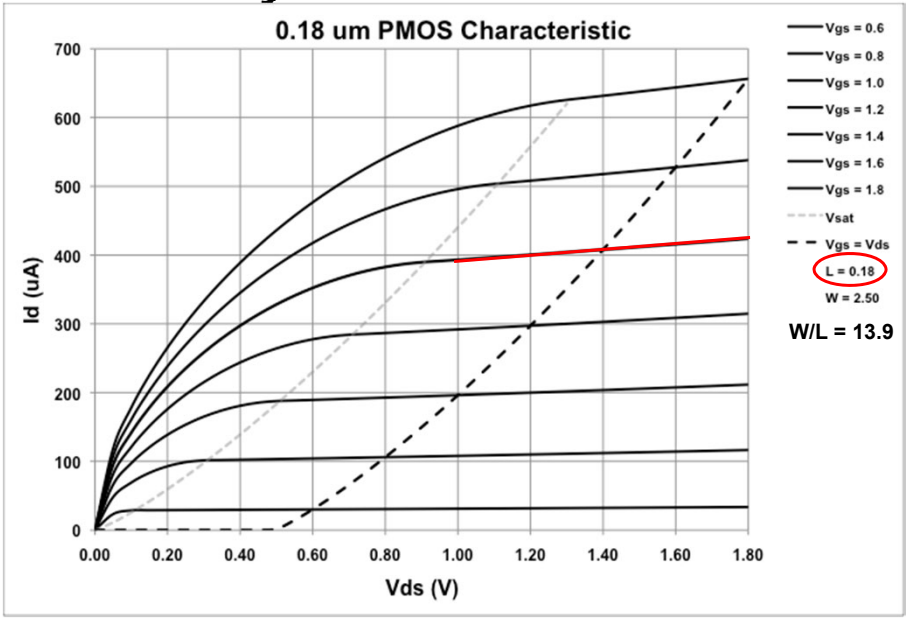
Ideal 180 nm nmos



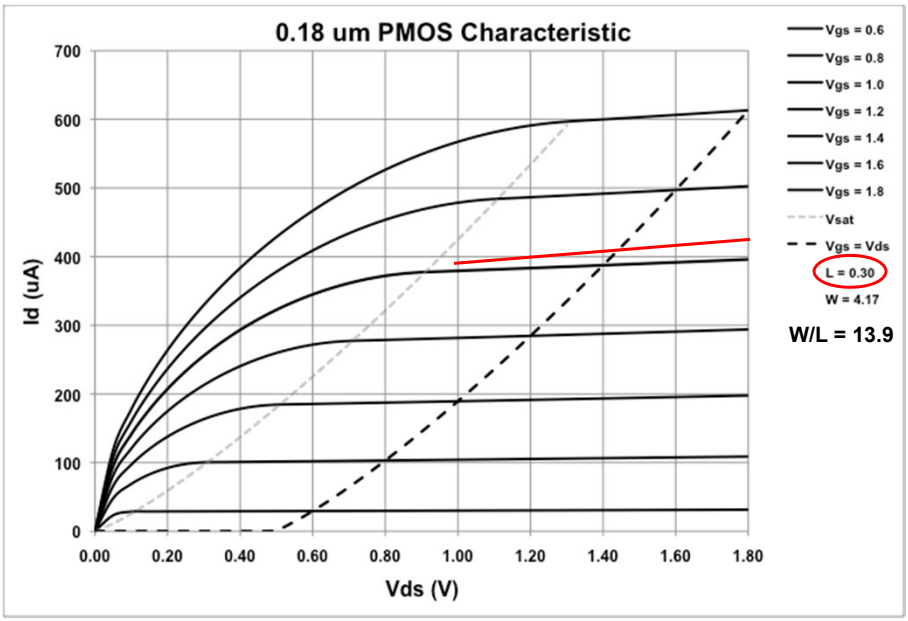
Real Device (Spice Model)

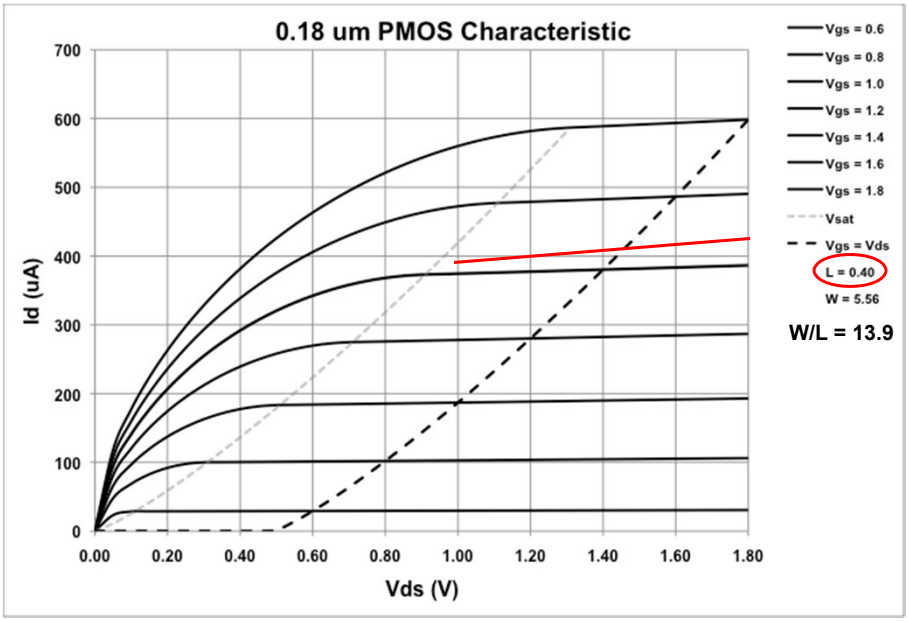


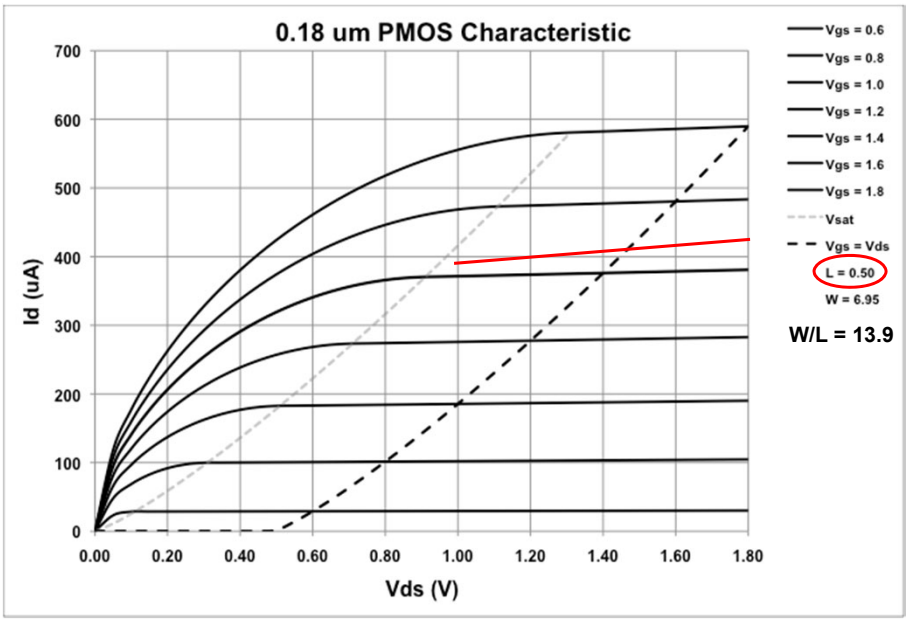
Lets Vary L and W With Constant W/L

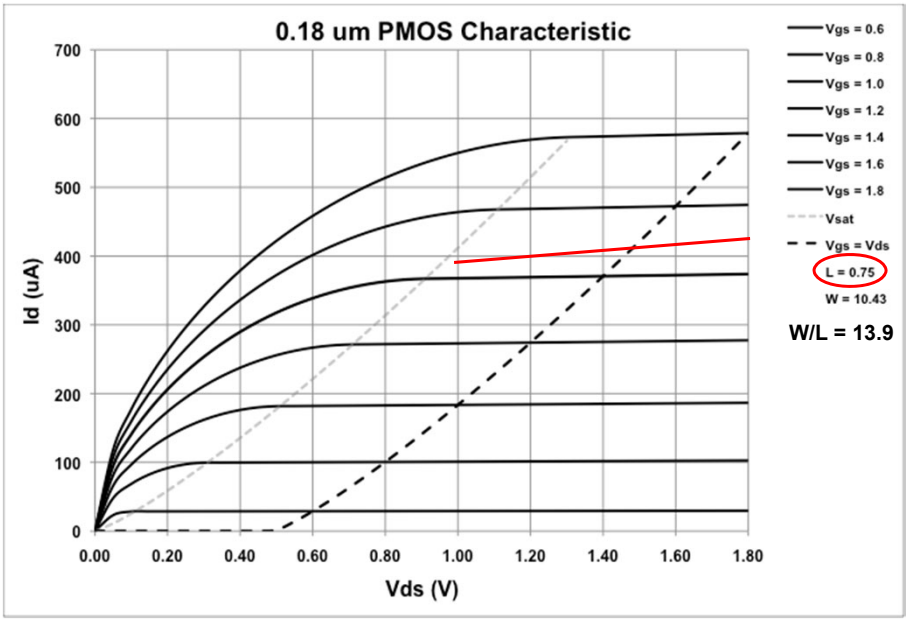


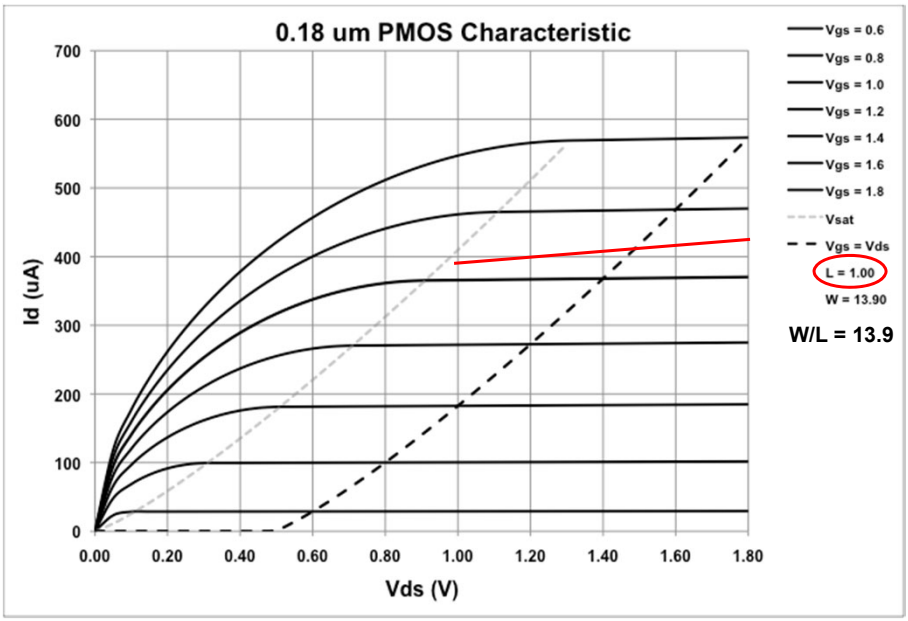
W/L = 13.9

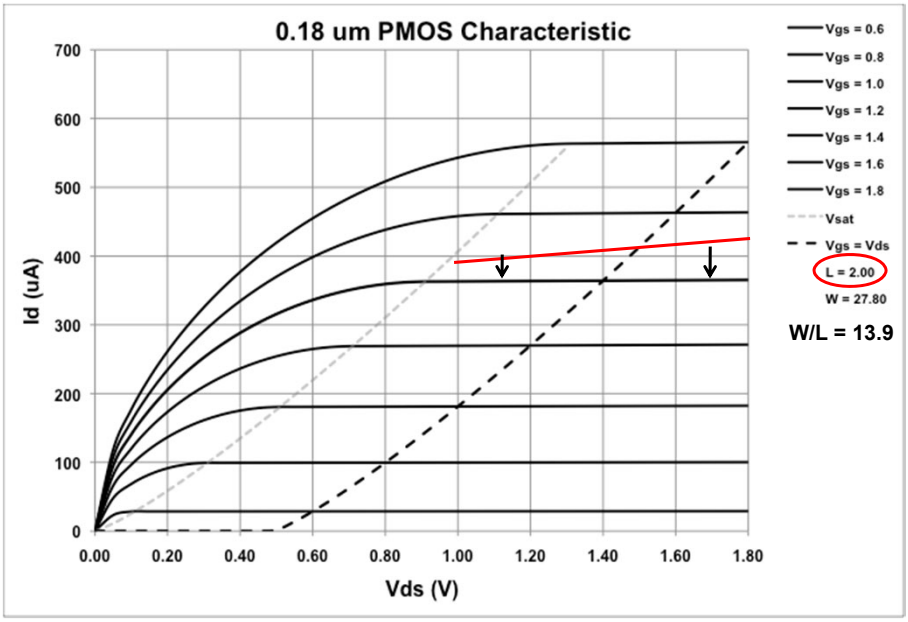

0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 0.30
W = 4.17
W/L = 13.9

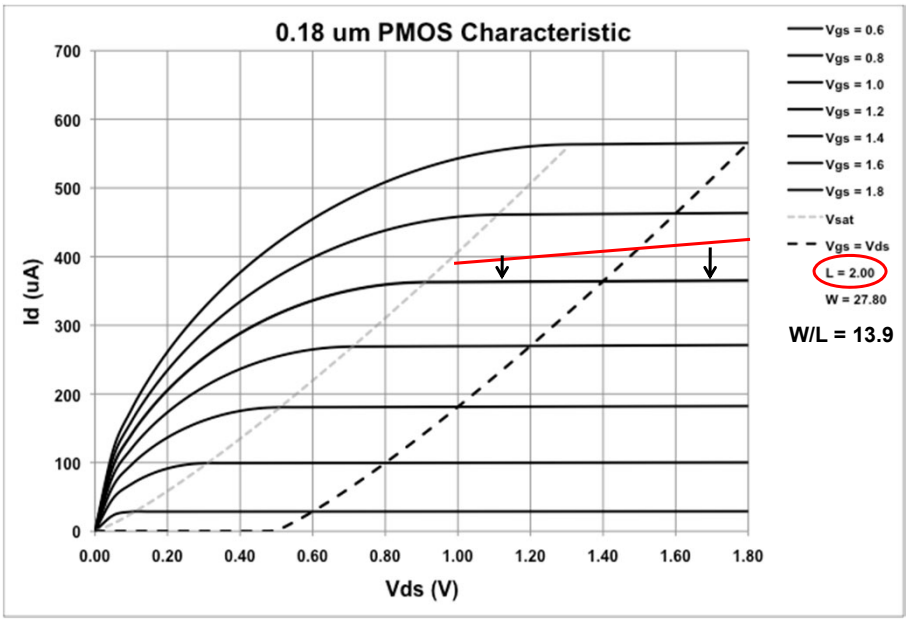

0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 0.40
W = 5.56
W/L = 13.9


0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 0.50
W = 6.95
W/L = 13.9


0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 0.75
W = 10.43
W/L = 13.9


0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 1.00
W = 13.90
W/L = 13.9


0.18 um PMOS Characteristic
Id (uA)
Vds (V)
0
100
200
300
400
500
600
700
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vgs = 0.6
Vgs = 0.8
Vgs = 1.0
Vgs = 1.2
Vgs = 1.4
Vgs = 1.6
Vgs = 1.8
Vsat
Vgs = Vds
L = 2.00
W = 27.80
W/L = 13.9



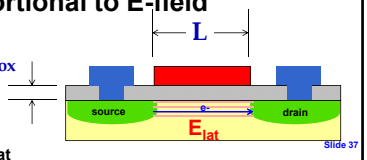
Real World Effects

Modifications to Model

- Velocity Saturation
- Channel Length Modulation
- The Body Effect

Velocity Saturation

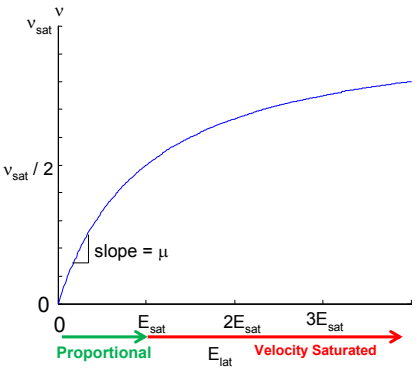
- We assumed carrier velocity is proportional to E-field
  - $v = \mu E_{lat} = \mu V_{ds}/L$
- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches v_{sat} at some $E_{lat} = E_{sat}$
    - Electrons: 6-10 x 10^6 cm/s
    - Holes: 4-8 x 10^6 cm/s
  - Better model



$$v = \frac{\mu E_{lat}}{1 + \frac{E_{lat}}{E_{sat}}} \Rightarrow v_{sat} = \mu E_{sat}$$

When E_{lat} is large

When E_{lat} is small, denominator ~ 1 and $v \sim \mu E_{lat}$



Vel Sat I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_d = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

- Velocity-saturated ON current increases with only V_{DD}

$$I_d = C_{ox} W (V_{gs} - V_t) v_{max}$$

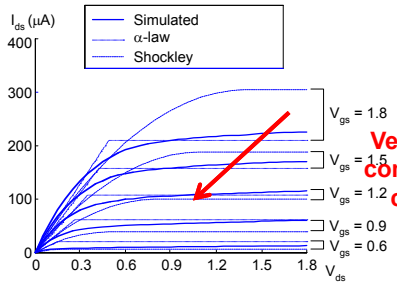
- Result: lower currents than ideal model
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically

α-Power Model

$$I_d = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat} \frac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$I_{dsat} = P_c \frac{\beta}{2}(V_{gs} - V_t)^{\alpha}$$

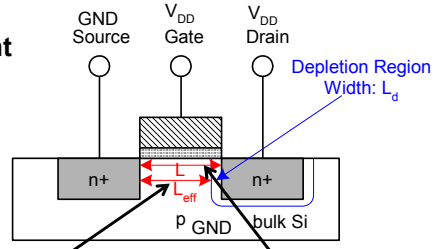
$$V_{dsat} = P_v (V_{gs} - V_t)^{\alpha/2}$$



Velocity Saturation compresses current characteristics.

Channel Length Modulation

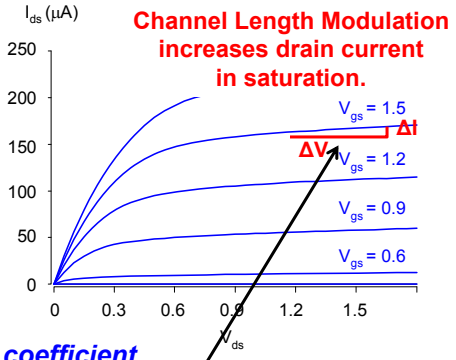
- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



L_{eff} = "Effective Length"
Typically less than $L_{physical}$

Chan Length Mod I-V

$$I_d = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$

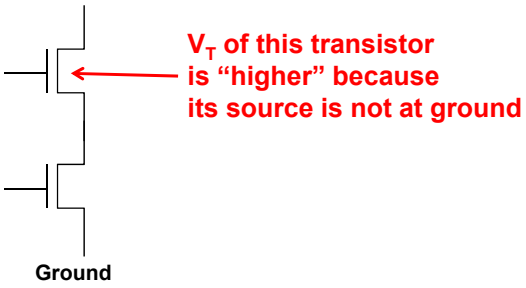


Channel Length Modulation increases drain current in saturation.

- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics
- Compute as "slope" of curve in saturation = ΔI/ΔV

Body Effect

- V_t: gate voltage necessary to invert channel
- Increases if source-to-body voltage increases because source is connected not to ground but drain of another transistor
  - Effective source-to-body increases
- Increase in V_t with V_{SB} is called the *body effect*



Body Effect Model

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- ϕ_s = *surface potential* at threshold

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i

$$v_T = \frac{kT}{q} = 26mv \quad \text{at } 300°K$$

n_i = 1.45 X 10^{10} cm^{-3} for Silicon

- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Key Point: transistors with source NOT at ground are *harder* to turn on.

Question

Assume

- **One input changes only infrequently**
- **Other changes frequently**

Which input drives which transistor for faster gate?