Introduction to
CMOS VLSI
Design

VLSI Circuit Layout: Standard Cells

Peter Kogge
University of Notre Dame
Fall 2015, 2018

Based on material from
Prof. Jay Brockman, Joseph Nahas, University of Notre Dame
Prof. David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

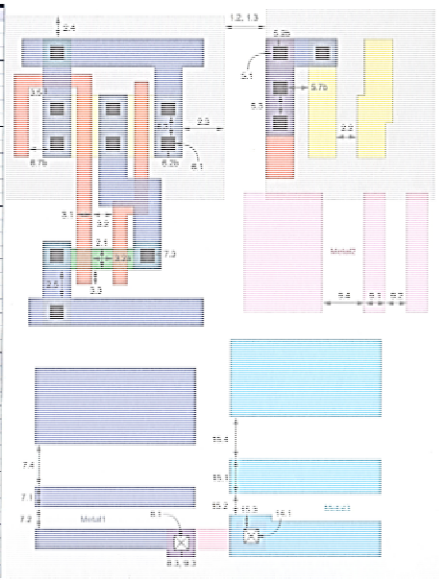
- Design Rule Review
- Layout Styles
- Standard Cell Layouts
- Wiring Tracks
- Stick Diagrams
- Euler Paths
- Tracks and Spacing's
- Area Estimation

Audience Review Questions

- ❑ **What is a “Design Rule”?**
- ❑ **What is “λ”?**
- ❑ **Why is this a useful unit of measure?**

Design Rules from Ed. 3’s Back Cover

Layer	Rule	Description	SCMOS	SUBM	DEEP
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surround by well	5	6	6
	2.4	Substrate/well contact surround by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field inside	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate/well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4
Contact (to poly or active)	5.1, 6.1	Width (exact)	2x2	3x3	3x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/active contacts	3	3	3
	6.8b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 λ	4	6	6
Via1–Via(N-1)	8.1, 14.1, ...	Width (exact)	2x2	2x2	3x3
	8.2, 14.2, ...	Spacing to via on same layer	3	3	3
	8.4	Spacing to contacts (if no stacked vias)	2	2	n/a
	8.5	Spacing of via1 to poly or active edge	2	2	n/a
	14.4	Spacing of via2 to via1 (if no stacked vias)	2	2	n/a
Metal2–Metal(N-1)	9.1, ...	Width	3	3	3
	9.2, ...	Spacing to same layer metal	3	3	4
	9.3, ...	Overlap of via	1	1	1
	9.4, ...	Spacing to metal for lines wider than 10 λ	6	6	8
Metal3 (3-layer process)	15.1	Width	6	5	n/a
	15.2	Spacing to metal3	4	3	n/a
	15.3	Overlap of via2	2	2	n/a
	15.4	Spacing to metal for lines wider than 10 λ	8	6	n/a



A Conservative Set of Simpler Rules

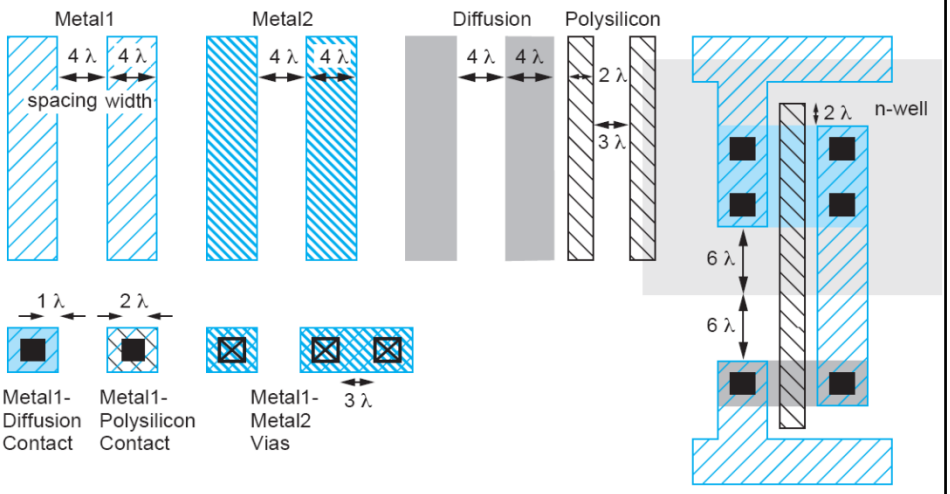


FIGURE 1.39 Simplified λ-based design rules

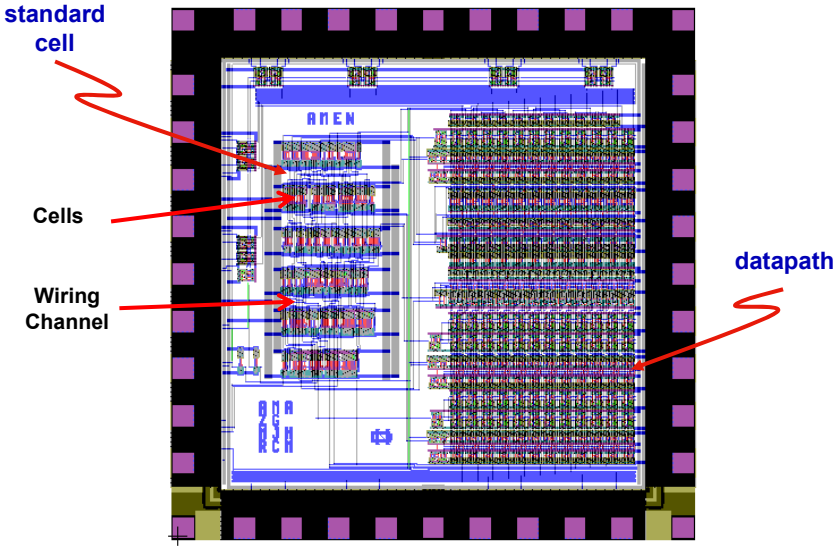
Audience Question: Why are we using 4λ here, vs 3λ from rules

Layout Styles

Layout Styles

- **Custom**
  - Random transistor and other component positioning and wiring.
- **Standard Cell**
  - Logic gates "pre-designed"
    - Power rails (Vdd and Vss) on top and bottom
    - Common N and P wells
      - PMOS transistors on top
      - NMOS transistors on bottom
  - Gates wired together automatically using Place and Route tool.
- **Pitch-Matched Data Path**
  - Custom or automatic layout of logic in data channels.
    - Typically 8, 16, 32, or 64 bits wide.
  - Channels match each-other and mesh.
- **Memory will be discussed later**

Layout Styles: An ND 12 bit Processor

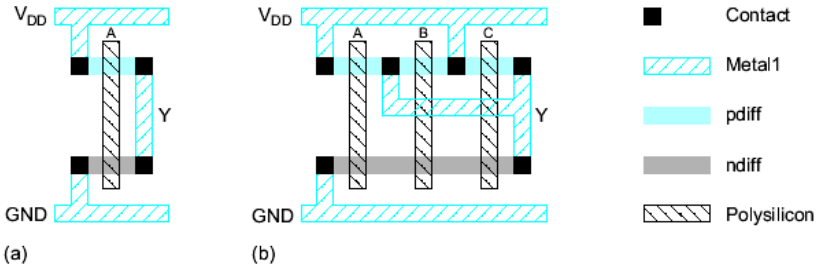


Stick Figure Construction

- Draw horizontal wires as follows
  - Metal1 (blue) for Vdd on top
  - Metal1 (blue) for gnd at bottom
  - Diffusion for ptype just below Vdd
  - Alternative: use green with a yellow box
  - Diffusion for ntype just above Gnd
  - Metal2 for longer range wires
- Draw vertical poly for each gate input
- Select which input corresponds to each vertical
  - "Euler's Algorithm" later on will tell us this
- Determine how/where to wire ■ or X
  - Connections to Vdd/gnd
  - Connections from p to n types
- With "luck" you don't have to "break" the diffusion
- Key parameter to estimate from this: How "wide" is circuit?

Stick Diagrams

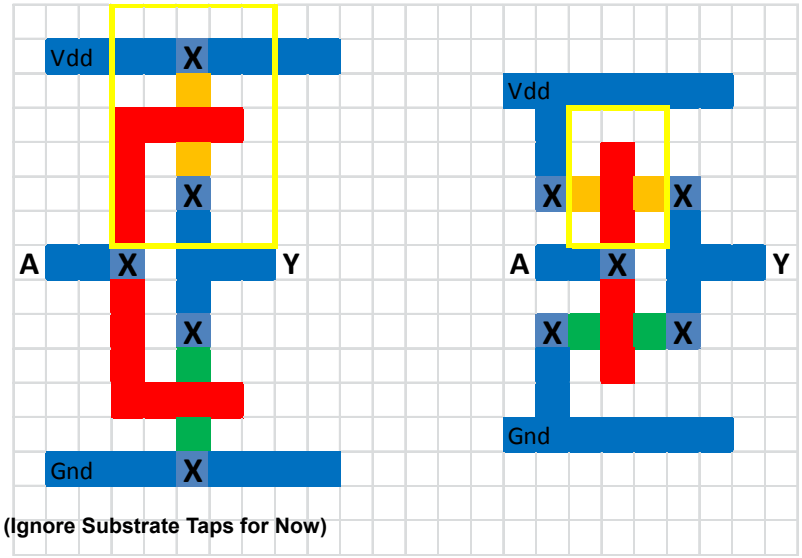
- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers
  - Relative position of key components



What type of gates are these?

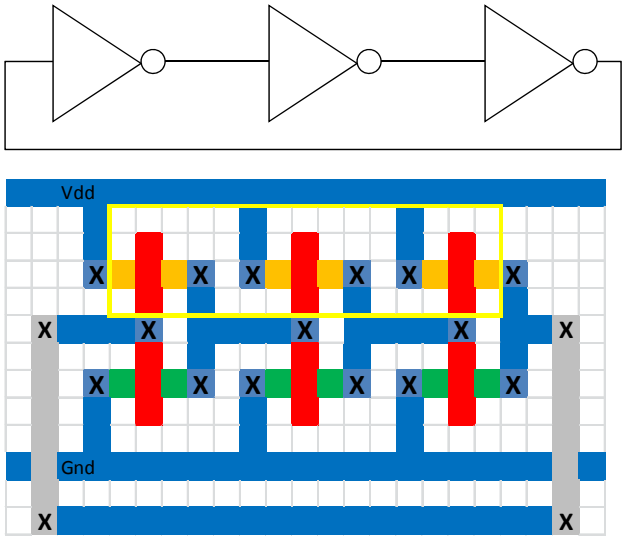
What are the widths of the nmos and pmos transistors?

Alternative Invertor Circuit Layouts (Single Well)

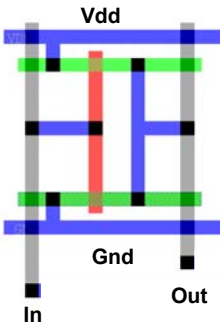


(Ignore Substrate Taps for Now)

Repetitive Custom Layout of Ring Oscillator

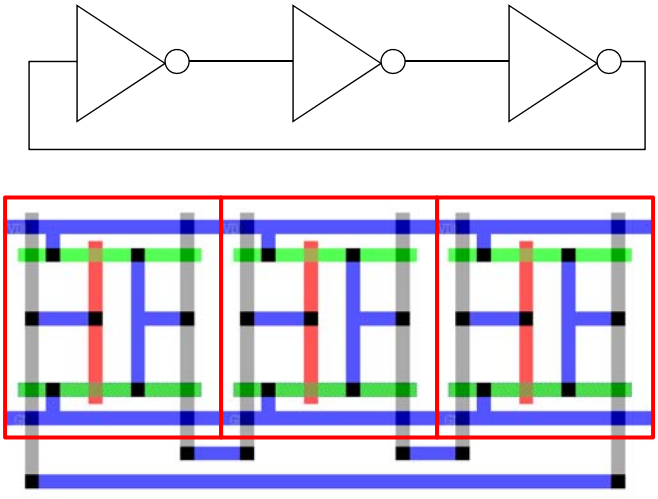


Standardizing the Invertor

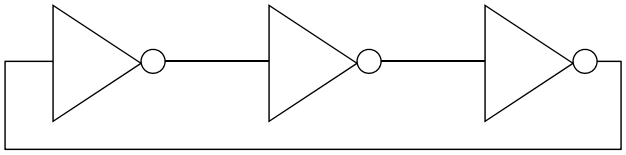


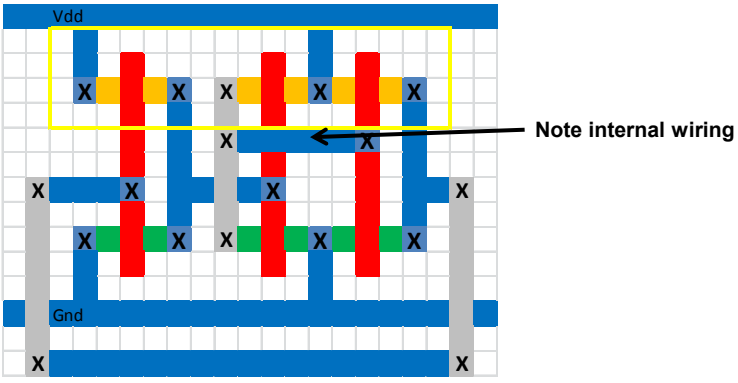
- Standard Height
- Vdd and Ground match up
- I/O Come down from M2 to Wiring Bays below cell
- Width can vary

Standard Cell Layout of Ring Oscillator



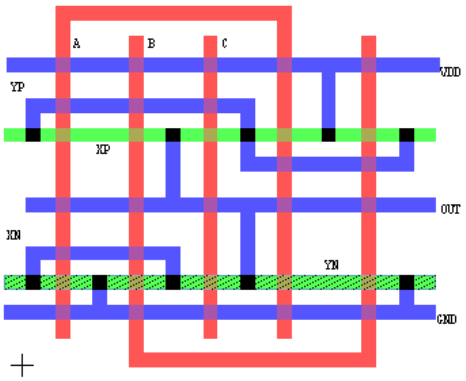
Aside: Optimized Custom Layout of Ring Oscillator



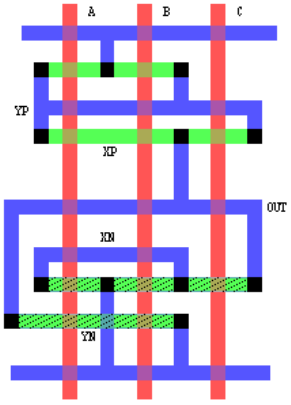


Complex Circuit Layouts

$\overline{C\,(A+B) + AB}$



Single diffusion runs



Multiple Diffusion runs

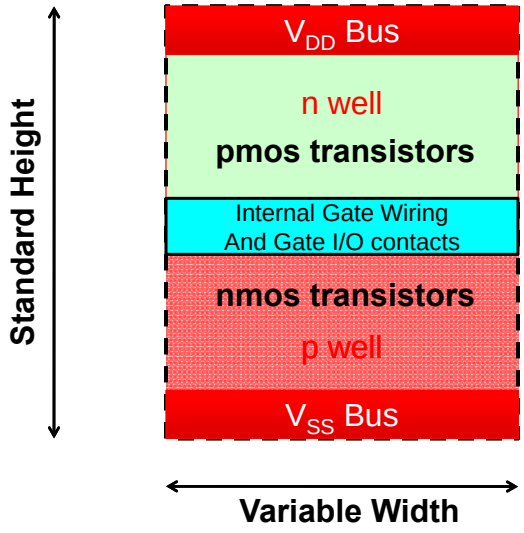
Can you draw the transistor diagram?

Standard Cell Layout

Gate Layout

- **Standard cell design methodology**
  - V_{DD} and GND should be some standard height & parallel
  - Within cell, all pMOS in top half and all nMOS in bottom half
  - Preferred practice: diffusion for all transistors in a row
    - With poly vertical
  - All gates include well and substrate contacts
- **Multi-gate circuits constructed by "snapping" gates together**
  - If two standard cells abut, Vdd & GND "snap together"
  - Adjacent gates must still satisfy design rules at boundaries
- **Bigger circuits constructed by rows of such multi-gates**
  - With "routing channels" between them for wiring
    - Typically using 2 levels of metal
  - And "flips" to align Vdd and Gnd

Standard Cell Layout



Bus connects to neighboring cells

Well connects to neighboring cells

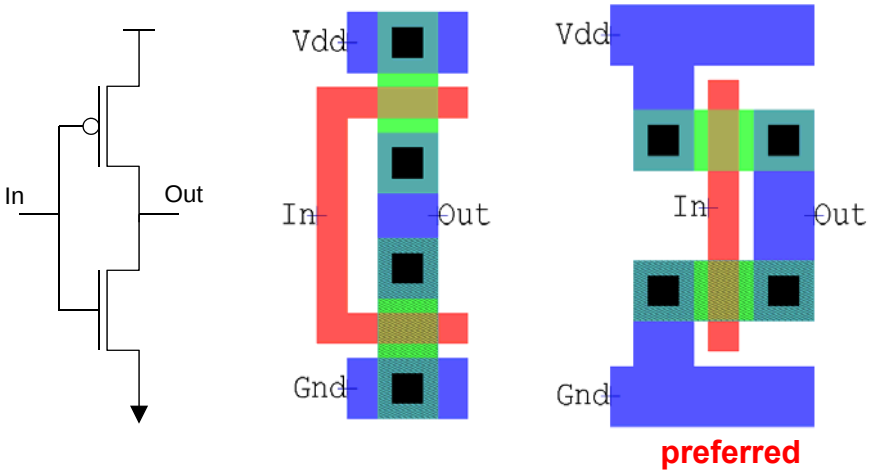
Well connects to neighboring cells

Bus connects to neighboring cells

Audience Question: Why is "connecting to neighbors" a good thing?

Inverter Layout

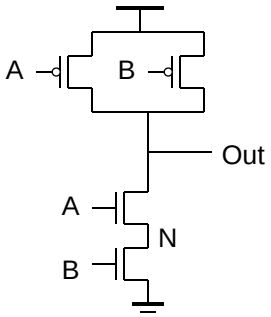
NOT to scale!

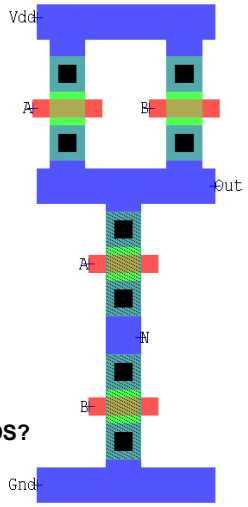


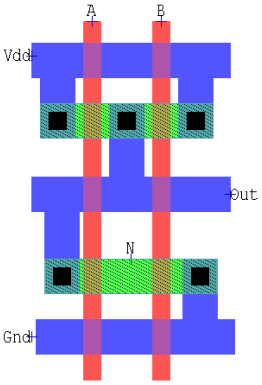
preferred

What is the width of the nmos and pmos transistors? Why?
What happens to size of inverter if we want to change widths?

NAND Gate Layouts







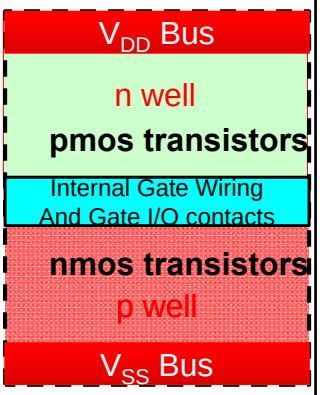
preferred

Audience Questions:

- **What is preferred width of pMOS?**
- **Why is rightmost preferred?**

Inside A Modern "Standard Cell"

- **Have Diffusion running horizontally**
  - **P type "below" the Vdd bus**
  - **N type "above" the GND**
- **Have Poly running vertically**
- **Use metal to appropriately wire diffusions**
  - **To Vdd & GND**
  - **To the other diffusion**
  - **To different points in current diffusion**
- **Attach I/O contacts to metal**



Question to be answered by later "Euler Path" algorithm:
Can we draw diffusion as single long rectangles without gaps?

A Simple Standard Cell Library

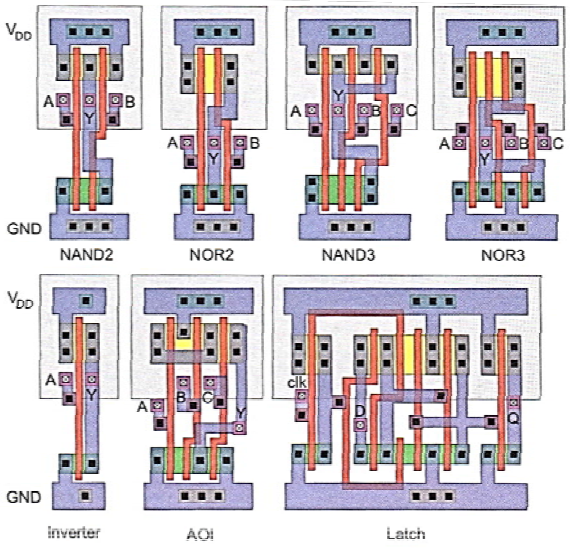
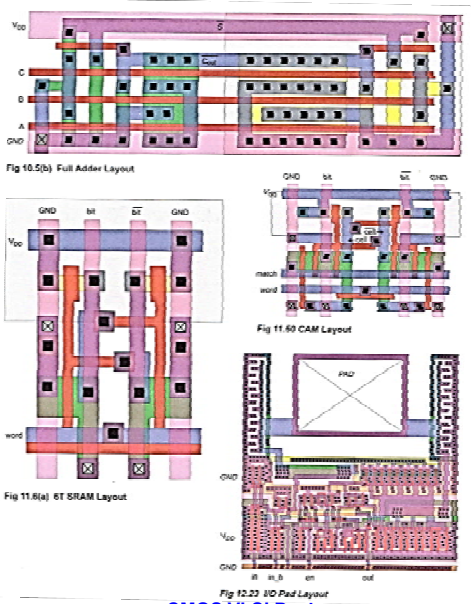


Fig 1.62 Standard Cell Layouts

More Complex Gates



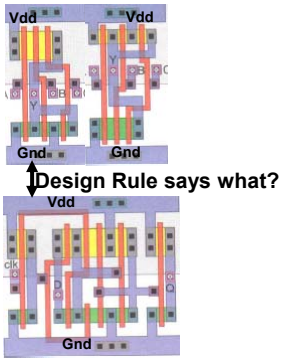
Pitch-Matching (Fig. 1.65)

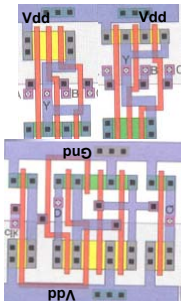
A	A	A	A	B
A	A	A	A	B
A	A	A	A	B
A	A	A	A	B
C		C		D

Would it help if:

- **A could be slightly shorter?**
- **C could be slightly narrower?**
- **D could be smaller?**

What If We Want to "Stack" Gates?





But What if We "Flip" One Row?

MIPS ALU & Data Flow via Standard Cells

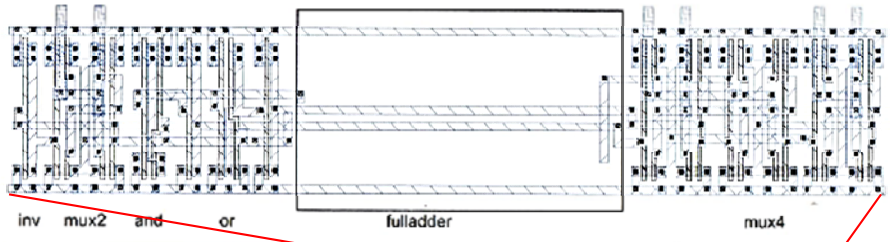
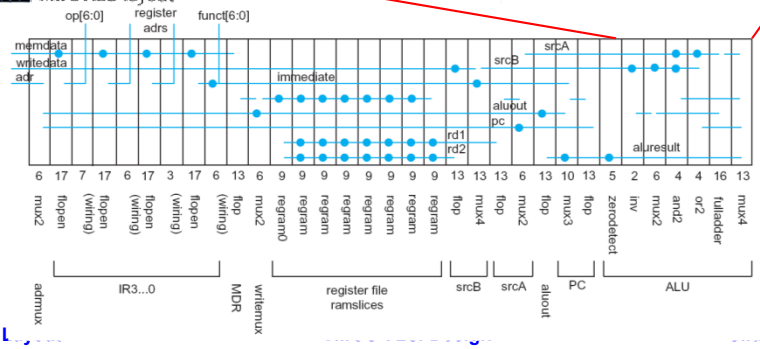
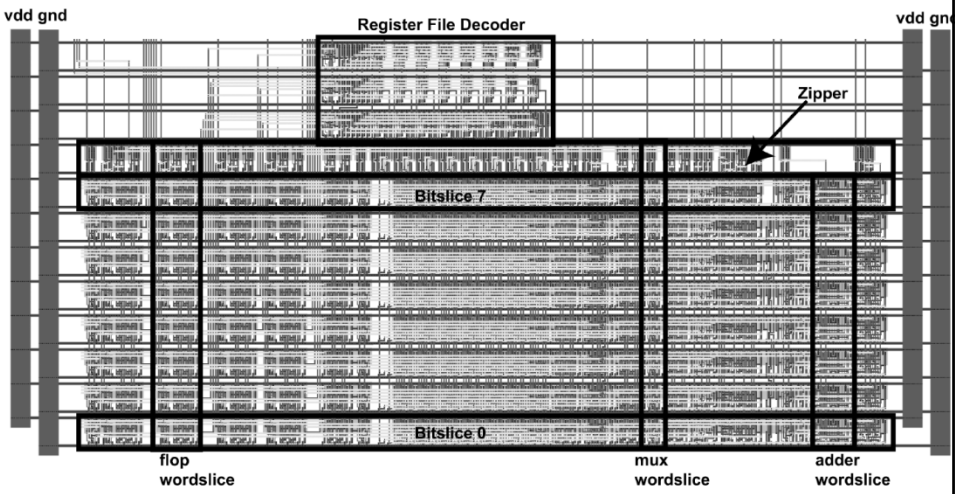


FIG 1.67 MIPS ALU layout



Now for the Full 8 Bit Data Flow



What If We Can't Use the Internal Wiring Channels?

FIGURE 1.64 MIPS controller layout (synthesized)

Audience Questions:

1. **How many levels of metal do we need for this?**
2. **How would you estimate the height of the wiring channels?**
3. **Why is deciding which logic gate standard cell goes where important?**

A Fully Synthesized 8-bit MIPS