Introduction to CMOS VLSI Design

Quick Verilog

Lecture by Peter Kogge
Fall 2009, 2011, 2012, 2015, 2018
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Using some slides by Jay Brockman Notre Dame 2008, and David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Levels of Design Modeling

- **Structural**: how a module is “wired together” from simpler modules
  - modules defined in terms of input and output **ports**
  - “Calling” a module creates a new instance
    - With “arguments” that are named wires.
- **Behavioral**: how outputs change as function of inputs
  - Key statement type: **assignment**
    - **Continuous** assignment – for driving a wire
    - **Always** assignment – for driving a latch
- **Physical**: layout of devices on chip
- **Netlist**: list of all ports connected to each wire
Verilog

- Verilog: one of two popular Hardware Description Languages (HDL)
  - VHDL is the other
- Naturally modular:
  - Define new module type in terms of simpler types
  - When used, creates a new "instance" of module
  - With wire names between "ports" of instance
- Suitable for all levels of models:
  - Behavioral: with no other resources needed
  - Structural: with library of technology-specific modules
  - Physical: as with structural but with "place & route" to
    - Place individual instances on 2D chip surface
    - Route wires between instance ports using chip metal

In Following

- Courier text = sample Verilog code
- Green courier = sample use of a keyword
- <xxx> = a general syntactic term
MIPS8 Overview

MIPS Architecture

- Example: subset of MIPS processor architecture
  - Drawn from Patterson & Hennessy
- MIPS is a 32-bit architecture with 32 registers
  - Consider 8-bit subset using 8-bit datapath
  - Only implement 8 registers ($0 - $7)
  - $0 hardwired to 00000000
  - 8-bit program counter
- David Harris has developed labs to implement
  - Uses Electric CAD tools
  - Illustrate the key concepts in VLSI design
Instruction Set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Encoding</th>
<th>op</th>
<th>funct</th>
</tr>
</thead>
<tbody>
<tr>
<td>add S1, S2, S3</td>
<td>addition: S1 → S2 + S3</td>
<td>R</td>
<td>00000</td>
<td>10000</td>
</tr>
<tr>
<td>sub S1, S2, S3</td>
<td>subtraction: S1 → S2 - S3</td>
<td>R</td>
<td>00000</td>
<td>10010</td>
</tr>
<tr>
<td>and S1, S2, S3</td>
<td>bitwise and: S1 → S2 and S3</td>
<td>R</td>
<td>00000</td>
<td>10100</td>
</tr>
<tr>
<td>or S1, S2, S3</td>
<td>bitwise or: S1 → S2 or S3</td>
<td>R</td>
<td>00000</td>
<td>10101</td>
</tr>
<tr>
<td>slt S1, S2, S3</td>
<td>set less than: S1 → 1 if S2 &lt; S3</td>
<td>R</td>
<td>00000</td>
<td>10110</td>
</tr>
<tr>
<td></td>
<td>S1 → 0 otherwise</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>addi S1, S2, imm</td>
<td>add immediate: S1 → S2 + imm</td>
<td>I</td>
<td>00100</td>
<td>n/a</td>
</tr>
<tr>
<td>beq S1, S2, imm</td>
<td>branch if equal: PC → PC + imm²</td>
<td>I</td>
<td>000100</td>
<td>n/a</td>
</tr>
<tr>
<td>j destination</td>
<td>jump: PC_destination³</td>
<td>J</td>
<td>00010</td>
<td>n/a</td>
</tr>
<tr>
<td>lb S1, imm(S2)</td>
<td>load byte: S1 → mem[S2 + imm]</td>
<td>I</td>
<td>100000</td>
<td>n/a</td>
</tr>
<tr>
<td>sb S1, imm(S2)</td>
<td>store byte: mem[S2 + imm] → S1</td>
<td>I</td>
<td>110000</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Instruction Encoding

- 32-bit instruction encoding
  - Requires four cycles to fetch on 8-bit datapath
MIPS Microarchitecture

- Multicycle microarchitecture from Patterson & Hennessy

Multicycle Controller

8bit MIPS  CMOS VLSI Design  Slide 9

8bit MIPS  CMOS VLSI Design  Slide 10
MIPS Floorplan

MIPS Layout
Fabrication & Packaging

- Tapeout final layout
- Fabrication
  - 6, 8, 12" wafers
  - Optimized for throughput, not latency (10 weeks!)
  - Cut into individual dice
- Packaging
  - Bond gold wires from die I/O pads to package

8bit MIPS  CMOS VLSI Design  Slide 13

Modules, Structural Design, and Netlists

Verilog  CMOS VLSI Design  Slide 14
Signal Declarations

- **wire** <list-of-signal-names>;
  - Each name in list is a separate net
    - Treat as an electrical “wire”
    - No “stored value”
    - echoes whatever value is currently driving it to all other terminals with no time delay

- **reg** <list-of-signal-names>;
  - Each name treated like a “latch”
  - “Stores” value last “assigned” to it

- **parameter** <name> = <value>
  - Defines a constant value as in C const

Defining Modules in Verilog

- **Module**: defines a basic circuit with some input and output signals
- **module** <module-name>(<port-list>);
  - <definitions of internal signals>;
  - <assignments to internal signals and output ports>;
  - **endmodule**

- **<port-list>**: list of circuit I/Os
  - Each port is a named “wire” from/to a “pad”
  - Input signals: **input** <name>,<name>,...,
  - Output signals: **output** <name>,<name>,...,
  - Signals that can be both: **inout** <name>,<name>...
Example

module carry (input a, b, c, output cout);
wire x, y, z;
and g1(x, a, b);
and g2(y, a, c);
and g3(z, b, c);
or g4(cout, x, y, z);
endmodule

Verilog defines new module type
port description
3 internal nets
g1,...g4 instances of other module types
associating net names with ports builds internal netlist

Alternative Port List

module carry (a, b, c, cout);
  input a, b, c;
  output cout;
wire x, y, z;
and g1(x, a, b);
and g2(y, a, c);
and g3(z, b, c);
or g4(cout, x, y, z);
endmodule

Sometimes easier to read
Transistor-Level Model

```verilog
module carry(input a, b, c,
              output cout)
    wire i1, i2, i3, i4, cn;

    tranif1 n1(i1, 0, a);
    tranif1 n2(i1, 0, b);
    tranif1 n3(cn, i1, c);
    tranif1 n4(i2, 0, b);
    tranif1 n5(cn, i2, a);
    tranif0 p1(i3, 1, a);
    tranif0 p2(i3, 1, b);
    tranif0 p3(cn, i3, c);
    tranif0 p4(i4, 1, b);
    tranif0 p5(cn, i4, a);
    tranif1 n6(cout, 0, cn);
    tranif0 p6(cout, 1, cn);
endmodule
```

Note: nets can have more than 2 tie points

Defining Multi-wire Signals

- Often convenient to group set of signals under same name as a `vector`
  - E.g. a data bus
- Precede name by `range specification` `[n:m]`
  - n-m+1 = total number of signals
  - n: “number” given to left-most signal
  - m: “number” given to right-most signal
- To access individual wire use `<name>[i]`
- To access subset of wires use `<name>[i:j]`
- E.g. `input [7:0] memdata` defines 8 bit bus
Example 4-input Ripple Adder

```verilog
module four_bit_adder(input [3:0] a, b, input cin;
    output [3:0] s, output cout);

    wire [3:1] c;
    fulladder fa0(a[0], b[0], cin,   s[0], c[1]);
    fulladder fa1(a[1], b[1], c[1],   s[1], c[2]);
    fulladder fa2(a[1], b[1], c[2],   s[2], c[3]);
    fulladder fa3(a[1], b[1], c[3],   s[3], cout);
endmodule;
```

Note: “order” of instance statements in code is irrelevant

Types of Nets in Verilog

- **Wire**: a normal metal or poly line
  - driven by some single output port
  - Replicates signal at arbitrary # of input ports
- **Tri**: a tri-stated wire
  - May be driven by multiple tri-stated output ports
- **Supply0**: ground
- **Supply1**: Vdd
- **Wand**: wired AND
  - May be driven by multiple open collector drivers
- **Wor**: wired OR
  - May be driven by multiple emitter-coupled drivers
- **Triand**, **tior**: similar to above but may be three-state
  - Tri0: resistor to ground
  - Tri1: resistor to Vdd
- **Trireg**: models charge stored on a net
Verilog Value Types

- **Scalar**: (i.e. a single bit) may have values
  - 0: signal is driven to ground
  - 1: signal is driven high (typically to Vdd)
  - X: signal value is unknown or conflicted
  - Z: signal is “high impedance”

- **Sized numbers** written as `<number>`<base>`<digits>`
  - `<number>` is the number of digits
  - `<base>` is the base for the number representation
    - B or b: binary
    - O or o: octal
    - H or h: hexadecimal
    - D or d: decimal
  - `<digits>`: string of digits in the specified base notation

- **Unsized numbers**: eliminate the `<number>`

---

Value Examples

<table>
<thead>
<tr>
<th>Table A.2</th>
<th>Constants</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number</strong></td>
<td><strong># Bits</strong></td>
</tr>
<tr>
<td>3'b101</td>
<td>3</td>
</tr>
<tr>
<td>'b11</td>
<td>unsized</td>
</tr>
<tr>
<td>8'b11</td>
<td>8</td>
</tr>
<tr>
<td>8'b1010_1011</td>
<td>8</td>
</tr>
<tr>
<td>3'd6</td>
<td>3</td>
</tr>
<tr>
<td>6'o42</td>
<td>6</td>
</tr>
<tr>
<td>8'hAB</td>
<td>8</td>
</tr>
<tr>
<td>42</td>
<td>unsized</td>
</tr>
</tbody>
</table>

from W&H
High Level Verilog MIPS

// simplified MIPS processor
module mips #(parameter WIDTH = 8, REGBITS = 3)
  input clk, reset,
  input [WIDTH-1:0] memdata,
  output memread, memwrite,
  output [WIDTH-1:0] adrr, writedata);

  wire [31:0] instr;
  wire zero, alusrc, memoreg, iord, pcen, regwrite, regdst;
  wire [1:0] aluop, psource, alusrc;
  wire [3:0] irwrite;
  wire [2:0] alucont;

  controller cont(clk, reset, instr[31:26], zero, memread, memwrite,
                  alusrc, memoreg, iord, pcen, regwrite, regdst,
                  psource, alusrc, aluop, irwrite);
  alucontrol ac(aluop, instr[5:0], alucont);
  datapath # (WIDTH, REGBITS)
    dp(clk, reset, memdata, alusrc, memoreg, iord, pcen,
      regwrite, regdst, psource, alusrc, irwrite, alucont,
      zero, instr, adrr, writedata);
endmodule
Verilog Execution Model

Verilog Execution Model (1)

- Module definitions define
  - Input and output ports that can be wired to other module
  - Behavior: What happens in any instance when actual inputs change
- Model construction defines multiple instances of modules
  - How they are wired together
  - What to do “at time 0”
**Verilog Execution Model (2)**

- At any point in time
  - Compute values for all expressions that have been "activated"
  - Tag with time when changes should happen
  - Sort updates by time
- To advance to next step
  - Find updates with smallest time – make that the "current time"
  - Apply all updates
  - See (via appropriate netlists) which circuits see changes in inputs
  - Compute new values, tag the updates, and repeat

**Discrete Event Execution**

1. Sorted (by time) list of (time, port, new value)
2. Update current time to soonest time
3. For each touched input port:
   - Compute new output
   - See if changed from previous
   - Compute when change occurs
4. Follow net from output port(s) that changed to all connected input ports
Verilog Behavioral Models & Expressions

Behavioral Models in Verilog

- Normal Purpose:
  - Simplify design process for “simple” logic
  - ESPECIALLY STATE MACHINES
  - Avoid doing detailed structural design early in the design cycle
- Behavioral models act just like structural
  - Mixed model designs can be simulated simply
- Tools exist for synthesizing a structural design from behavior module
A Behavioral Module

module <module-name>(<port-list>);
<declarations>

assign #<delay> <net-name> = <expression>;

endmodule

repeated multiple times

Distributing Signals: Nets

- **Net**: changes value whenever circuit driving it changes
  - Carries a signal
  - Most common – a **wire**
- **assign #<delay> <net-name> = <expression>;**
  - *Any change in expression changes value assigned to net*
  - **<expression>**: functional combination of constants and other signals
  - **<net-name>**: name of net that “tracks” value of expression
  - #<delay>: optional “delay” from time expression changes until time net signal changes
Operators in Expressions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
<th>Precedence</th>
</tr>
</thead>
<tbody>
<tr>
<td>~</td>
<td>NOT</td>
<td>Highest</td>
</tr>
<tr>
<td>*, /, %</td>
<td>MUL, DIV, MODULO</td>
<td></td>
</tr>
<tr>
<td>+, -</td>
<td>PLUS, MINUS</td>
<td></td>
</tr>
<tr>
<td>&lt;&lt;, &gt;&gt;</td>
<td>Logical Left/Right Shift</td>
<td></td>
</tr>
<tr>
<td>&lt;&lt;&lt;, &gt;&gt;&gt;</td>
<td>Arithmetic Left/Right Shift</td>
<td></td>
</tr>
<tr>
<td>&lt;, &lt;=, &gt;, &gt;=</td>
<td>Relative Comparison</td>
<td></td>
</tr>
<tr>
<td>==, !=</td>
<td>Equality Comparison</td>
<td></td>
</tr>
<tr>
<td>&amp;, ~&amp;</td>
<td>AND, NAND</td>
<td></td>
</tr>
<tr>
<td>^, ~</td>
<td>XOR, XNOR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>, ~</td>
<td></td>
</tr>
<tr>
<td>?:</td>
<td>Conditional</td>
<td>Lowest</td>
</tr>
</tbody>
</table>

from W&H

Motivating Example

```verilog
module fulladder(input a, b, c,
                  output s, cout);

  Xor2 sum_1(a, b, s1);
  Xor2 sum_2(s1, c, s);
  carry cl(a, b, c, cout);
endmodule

module carry(input a, b, c,
              output cout)

  assign cout = (a&b) | (a&c) | (b&c);
endmodule
```

Which is:
- Structural?
- Behavioral?
Example: Carry Logic – Standard Cell Gates

- `assign cout = (a&b) | (a&c) | (b&c);`

Example: Carry Logic - Transistors

- `assign cout = (a&b) | (a&c) | (b&c);`
MIPS Datapath

- Multicycle μarchitecture from Patterson & Hennessy

Standard Cell Library

- Uniform cell height
- Uniform well height
- M1 $V_{DD}$ and GND rails
- M2 Access to I/Os
- Well / substrate taps
- Exploits regularity
Slice Plans

- Slice plan for bitslice
  - Cell ordering, dimensions, wiring tracks
  - Arrange cells for wiring locality

MIPS Datapath

- 8-bit datapath built from 8 bitslices (regularity)
- Zipper at top drives control signals to datapath
MIPS Verilog DataPath (1)

module datapath #(parameter WIDTH = 8, REGBITS = 3)
  input clk, reset,
  input [WIDTH-1:0] memdata,
  input [1:0] alusrc0, memtoreg0, lor0, pc0,
  input [1:0] rsource, alusrch0,
  input [3:0] irwrite,
  input [2:0] alucontrol,
  output zero,
  output [WIDTH-1:0] instr,
  output [WIDTH-1:0] a0, w0;
endmodule

// size of the parameters must be changed to match the WIDTH parameter
parameter CONST_ZERO = 8'b0;
parameter CONST_ONE = 8'b1;

wire [REGBITS-1:0] ra1, ra2, wa;
wire [WIDTH-1:0] pc, nextpc, m0, rd0, rd2, w0, s, src1, src2, aluresult,
  alucontrol, constx4;

assign constx4 = {instr[WIDTH-3:0], 2'b00};

// register file address fields
assign ra1 = instr[REGBITS+2:21];
assign ra2 = instr[REGBITS+15:16];
mux2 #(REGBITS) regmux(instr[REGBITS+15:16], instr[REGBITS+10:11],
  regset0, wa);

MIPS Verilog Data Path (2)

// independent of bit width, load instruction into four 8-bit registers
// over four cycles
flop #8 ir0(clk, irwrite[0], memdata[7:0], instr[7:0]);
flop #8 ir1(clk, irwrite[1], memdata[7:0], instr[15:8]);
flop #8 ir2(clk, irwrite[2], memdata[7:0], instr[23:16]);
flop #8 ir3(clk, irwrite[3], memdata[7:0], instr[31:24]);

// datapath
flopenc # (WIDTH) pcreg(clk, reset, pcen, nextpc, pc);
flop # (WIDTH) mdr(clk, memdata, rd);
flop # (WIDTH) arreg(clk, rd1, a);
flop # (WIDTH) wrd(clk, rd2, w0, writedata);
flop # (WIDTH) res(clk, aluresult, alucontrol);
mux2 # (WIDTH) addmux(pc, alucontrol, lor0, adz);
mux2 # (WIDTH) src1mux(pc, a, alucontrol, src1);
mux4 # (WIDTH) src2mux(w0, aluresult, CONST_ONE, instr[WIDTH-1:0],
  constx4, alusrch, src2);
mux4 # (WIDTH) pmux(aluresult, alucontrol, constx4, CONST_ZERO,
  pcsource, nextpc);
mux2 # (WIDTH) wdmux(alucontrol, md, memtoreg, w0);
regfile # (WIDTH, REGBITS) tff(clk, regwrite, ra0, ra2, wa, w0, rd1,
  rd2);
alu # (WIDTH) alunot(src1, src2, alucontrol, aluresult);
zerodetect # (WIDTH) zd(aluresult, zero);
endmodule

Verilog  CMOS VLSI Design  Slide 43

Verilog  CMOS VLSI Design  Slide 44
MIPS ALU

- Arithmetic / Logic Unit is part of bitslice

Behavioral ALU

```verilog
module alu #(parameter WIDTH = 8)
(input [WIDTH-1:0] a, b,
 input [2:0] alucont,
 output reg [WIDTH-1:0] result);

wire [WIDTH-1:0] b2, sum, slt;

assign sum = a + b2 + alucont[2];
// slt should be 1 if most significant bit of sum is 1
assign slt = sum[WIDTH-1];

always@(*)
case(alucont[1:0])
  2'b00: result <= a & b;
  2'b01: result <= a | b;
  2'b10: result <= sum;
  2'b11: result <= slt;
endcase
endmodule
```
Continuous Assignments

- `assign` statements are “continuous”
- Written once, executed “continuously”
- Any changes in right-hand side immediately reflected in left-hand signal
  - Delayed in time perhaps by `delay`
- If multiple assigns in a block,
  - execution is `order independent`
Procedural Assignments

- Sometime we want to execute statements \textit{procedurally} (like a C program), i.e.
  - Start statements at some point in time
  - And then in some order
  - Especially important for controlling registers
- Two kinds of such behavior
  - \textbf{Single pass behavior} is executed only once
    - At initialization
  - \textbf{Cyclic behavior} is triggered whenever “something” happens
    - Where “something” can be defined in advance
- Need \textit{registers} to capture values between changes

Registers

- Verilog \textit{registers} much like C variables
  - Once assigned a value, they keep it
  - Until another value is assigned
- Defined by: \texttt{reg [msb]:[lsb]} <\texttt{reg-name}>
  - If no [:] then default size is 1 bit
  - Initial value is “x”
- Typically assignments tied into events like clocks
Procedural Assignments

\[ \text{<reg-name>} = \text{<expression>}; \]

- Note: no “assign”
- When statement executed, register takes on value from expression
  - Actually an update event is scheduled
- Update event is done BEFORE next statement in program order

Verilog

module D_latch(input D, CLK, output Q);
Q = CLK ? D : Q;
endmodule
A D Latch with a Reset

module D_latch_wReset(input D, CLK, Reset,
  output Q);

  Q = Reset ? 0 (CLK ? D : Q);

endmodule

Program Blocks

- Often more than 1 statement needs to be executed in a time-sensitive assignment
- Such statements grouped into **blocks**
  - `<statement> ; ... <statement> ;`
- **begin** `<statement-block> end ;`
  - All statements in block are executed in **order**
    - i.e. one at a time top to bottom
  - Assignment statements within block are said to be **blocking assignments**
    - Next one cannot start until last completes
- **fork** `<statement-block> join ;`
  - All statements in block are executed in **parallel**
    - i.e. in any order
Single Execution Behavior

- Execute *only* at specific time, i.e. time=0
- Typically used by test benches for startup

```
initial <statement>;
```

- Example:
  ```
  initial begin
  Reset = 0;
  #10 Reset = 1;
  #5 Reset = 0;
  end
  ```

  What is the waveform?

Controlling Cyclic Behavior

- Statement to be executed at specific times
  - E.g. at clock pulses
  ```
  always @(<sensitivity list>) <statement>
  ```
- `@` is optional *event control operator*
- `<sensitivity-list>` is list of signal names
  - `@*` means use all nets & variables read by procedure’s statements
- Whenever *any one of signals* in sensitivity-list *changes*, `<statement>` is executed
  - And only then
- What kind of change is immaterial, unless signal name preceded by:
  - `posedge`: execute only on a 0 to 1
  - `negedge`: execute only on a 1 to 0
Non-blocking Assignments

- Use of "\(<=\)" instead of "\(=\)" in assignment makes statement execute concurrently with later statements
  \(<\text{register}> <\text{expression}>;\)
  - left-hand side MUST be a register
- Order of such assignments is immaterial;
  - They ALL HAPPEN AT ONCE!
- Better match to real circuits

\[
\text{always }@(\text{posedge } \text{clock})
\begin{align*}
\text{begin} & \quad \text{All expressions evaluated at same time;} \\
\text{reg1 } \leftarrow \text{expr1;} & \quad \text{then all assignments happen at same time} \\
\text{reg2 } \leftarrow \text{expr2;} & \\
\ldots & \\
\text{end} & \\
\end{align*}
\]

Example: Clock Generation

```verilog
Reg clk;

always
begin
    clk <= 1; \quad \text{schedules a change to clk “now”}
    # 5;
    clk <= 0; \quad \text{schedules a change to clk in 5 time units}
    # 5;
end
```
Assignment Summary

- Continuous assignment:
  - `assign #<delay> <net-name> = <expression>`
- Procedural assignment:
  - `<register> = <expression>;`
- Non-blocking assignment:
  - `<register> <= <expression>;`

Finite State Machines

```
module FSM(input clock, In1, ...Inn, output O1, ...Om);
reg state, next_state;
always @(posedge clock)
begin
  state <= next_state;
  ...
  Code that does something like next_state <= <expression>;
  ...
end
```
Multicycle Controller

8-bit MIPS

MIPS VERILOG CONTROL LOGIC

module controller(input clk, reset,
                  input [5:0] op,
                  input zero,
                  output reg memread, memwrite, alusrca, memtoreg, iord,
                  output pcad,
                  output reg irwrite, regdst,
                  output reg [1:0] pcsource, alurop, aluop,
                  output reg [3:0] irwrite);

- Next: list of constants to define machine states
- Then an “always” sensitive to rising edge of clock
  - Embedded case statement
  - One case per state
  - Determines what new state should be at end of this clock
- Then an “always” sensitive to any change in values
  - Embedded case statement
  - Each case specifies control signals to dataflow & memory
More Syntax

Memory

```verilog
reg <word-size> <memory-name> <mem-size>...<mem-size>;

- <word-size> is [<msb>:<lsb>]
- <mem-size> is [<low-index>:<high-index>]

Example: define register d_array as 2D array of 16 bit words

```verilog
reg [15:0] d_array [0:127][0:255]
```

- Selecting a word from an array:
  - Assume a_byte is an 8 bit set of wires
    ```verilog
    a_byte = d_array[64][32][12:5];
    ```
  - takes 8 bits from 32nd column of 64th row
Other Verilog Constructs

- **Comments**:
  - Single line: // ...
  - Block: /* .... */

- **Identifiers**:
  - start with letter or _
  - follow by letters, digits, _, or $
  - case sensitive

If Statement

```verilog
if (<expression>)
  <then_statement>
else <else_statement>
end
```

- else is optional
- nesting permitted, as in else if ....
Case Statement

case (<expression>)
  <case_item>: <case_item_statement>
  ...
  default: <case_item_statement>
endcase

- <case_item> is a constant that is matched against that from the <expression>
  - If match, then do the <case_item_statement>
    - And exit case statement after completion
  - If not, try next case
- default is optional for no matches

For Statement

for (<initial_assignment>;
  <condition-expression>;
  <update_statement>)
begin
<loop-statements>
end

- <initial_assignment> and <update_statement> are some form of assignment
- All iterations of <loop-statements> conceptually done AT SAME TIME
Other Loops

- `repeat (<expression>)`
- `while (<condition>)`
- `begin`<br>- `begin`<br>- `<loop-statements>`<br>- `<loop-statements>`<br>- `end`<br>- `end`

  - `wait(<expression>) <statement>`

  All iterations of `<loop-statements>` conceptually done AT SAME TIME

Timescale

- `timescale <time_unit>/<time_precision>`
  - `<time_unit>` and `<time_precision>` of form:
    - `<number> <space> <unit>`
    - with `<unit>` as s ms us ns ps fs

  From this point on:
  - for delays: 1 time unit = `<time_unit>`
  - for precision of internal time calculations: use `<time_precision>`
Module Instantiation
Options

- Previously
  
  `<module-type> <instance-name> (<list-of-signal-names>);`

- In place of `<list-of-signal-names>`, use list of
  
  `. <port-name>(<net-name>)`

- Optionally add `#(<parameter_assignment_list>)` after `<module-type>`
  
  - Associate values with parameters within module definition
  - Overwrites `parameter <name> = <value>` inside definition

More
(See Quick Reference Card)

- Builtln modules: and, or, nand, nor, xor, xnor
  
  - One output (first argument)
  - One or more inputs (rest of arguments)

- `$display` statement: verilog eqvt of printf
  
  - `$display ( <format string>);`
    
    - (“… text …”, <list of var-names>)
      
      - `%<format-code>` in text says how to format “next” var in list
      
      - `$time` is current time
  
  - executed as any other statement in a block
  
  - references variable values AS THEY ARE THEN

  see http://www.hpcc.ecs.soton.ac.uk/hpci/tools/vlogref.pdf
More Examples

Typical Design

- File with list of module definitions
- Typically first one is a **testbench**
  - Glues together other pieces in a way that allows appropriate operation to be demonstrated
  - Includes `initial` code to start up & reset system
  - Includes code to generate clocks & other common control signals

```verilog
module TestBench(); \ no ports
reg <in-list>; \ all input ports to DUT
wire <out-list>; \ all output ports from DUT

module Device_Under_Test(input <in-list>, output <out-list>);
...
endmodule;

initial begin
  code to change values of regs in <in-list>
end;
endmodule;
```
**A Behavioral Full Adder**

```
module fulladder(input a, b, cin, output s, cout);
    wire prop;
    assign prop = a ^ b;
    assign s = prop ^ cin;
    assign cout = (a & b) | (cin & (a | b));
endmodule
```

Note: “order” of *assigns* in code is irrelevant.

---

**Example: A 4 bit Shift Register**

```
module shiftreg(input E, clk, reset, output D, C, B, A);
    reg A, B, C, D; // note these output port defined to be regs
    always @(posedge clk or posedge reset)
    begin
        if (reset) begin A=0;B=0;C=0;D=0;E=0; end
        else begin
            A = B;
            B = C;
            C = D;
            D = E;
            end
    end
endmodule
```

What happens if we reorder these?
**Repeat Shift Register Example:**

![Diagram of a shift register]

```
module shiftreg(input E, clk, reset,
               output reg D, C, B, A);
always @(posedge clk or posedge reset)
begin
  if (reset) begin A<=0; B<=0; C<=0; D<=0; E<=0; end
  else begin
    A <= B;
    B <= C;
    C <= D;
    D <= E;
  end
end
```

Note simplified syntax

Now what happens if we reorder these?

---

**Finite State Machines**

![Diagram of a finite state machine]

```
module FSM(input clock, In1, … Inn, output O1, … Om);
  reg state, next_state;
  parameter _statei = 'bxxxx;
  always @(posedge clock)
  begin
    state <= next_state;
    case (state) ...
      …
        statei: begin next_state<=statei; Ok <= … end;
        …
    end
end
```

Verilog