Possible Project Plan- 2018 VLSI

Goal: come up with a design document that would be sufficient to use as a basis for a possible real layout and fab of the microTPU (uTPU) on ND process. This design document should have at least the following sections (order is suggestive – choose what makes the most sense):

1. Description of project goal: design a single node of a uTPU having a short 8-bit floating point multiply-adder, and sufficient I/O to allow coupling to other chips.
2. Description of microarchitecture of uTPU – next level of detail from that in the notes. Include all the I/O signals that you need.
3. Description of how such a chip could be used in a variety of possible systems, including external SRAM to load data in and take sums out.
4. Functional model in Verilog of the uTPU. Have a testbench which is sufficient to test out design, and one or two other that reflect how uTPU might be used for real. Code in an Appendix.
5. Summary of assumed technology
6. List of key logic cells, with area, delay, input cap, etc of each in a table. (Appendix will have cell layouts using Electric)
7. Structural model in Verilog of the uTPU. Reuse functional testbenches. Each logic cell is a module in Verilog. Code in an Appendix. Feel free to simplify design such as using ripple adders.
8. Approximate layout of design to allow you to estimate area , worst case delay (i.e. max clock rate), and power.
9. Compare if you can to Google TPU.
10. What would you do different and/or to extend the design to a possible real implementation.
11. Log of personnel responsibilities and approximate time spent.

Note: feel free to assume we will make time in class to discuss issues as they come up.