

### SCMOS Layout Rules - Contact to Poly

On 0.50 micron process (and all finer feature size processes), it is required that all features on the insulator layers (CONTACT, VIA, VIA2) must be of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

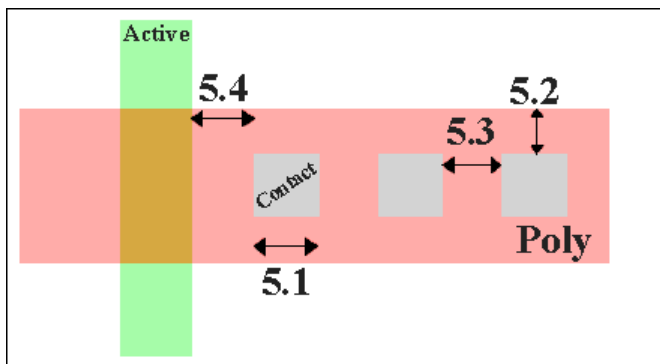
If your design cannot tolerate 1.5 lambda contact overlap in 5.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 5.1, 5.3, and 5.4, still apply and are unchanged.

#### Simple Contact to Poly

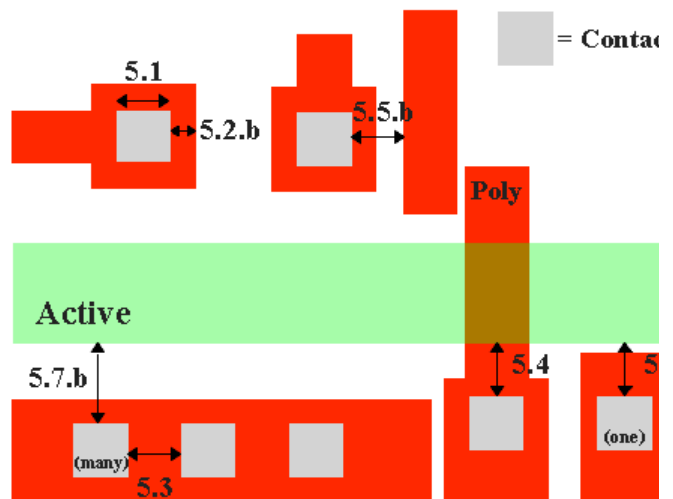
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2

#### Alternative Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.2.b	Minimum poly overlap	1	1	1
5.5.b	Minimum spacing to other poly	4	5	5
5.6.b	Minimum spacing to active (one contact)	2	2	2
5.7.b	Minimum spacing to active (many contacts)	3	3	3



Simple Poly to Contact



Alternative Contact to Poly

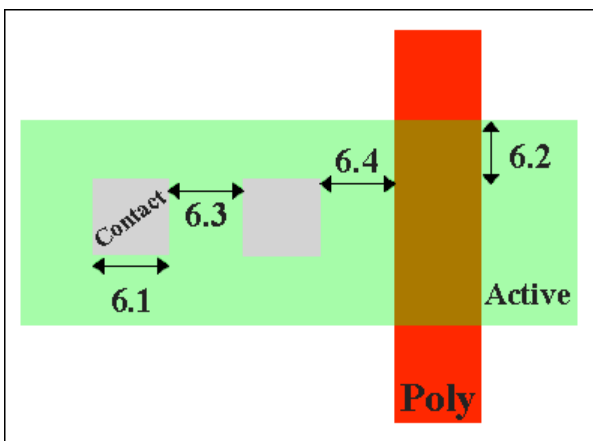
### SCMOS Layout Rules - Contact to Active

If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

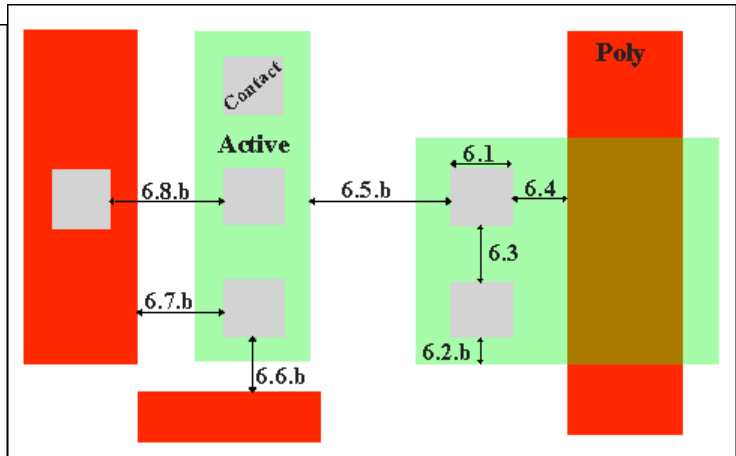
**Simple Contact to Active**

**Alternative Contact to Active**

Rule	Description	Lambda			Rule	Description	Lambda		
		SCMOS	SUBM	DEEP			SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2	6.2.b	Minimum active overlap	1	1	1
6.2	Minimum active overlap	1.5	1.5	1.5	6.5.b	Minimum spacing to diffusion active	5	5	5
6.3	Minimum contact spacing	2	3	4	6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.4	Minimum spacing to gate of transistor	2	2	2	6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
					6.8.b	Minimum spacing to poly contact	4	4	4



**Simple Contact to Active**



**Alternative Contact to Active**