

CMOS VLSI Design

CMOS Processing

Peter Kogge
University of Notre Dame
Fall 2015, 2018

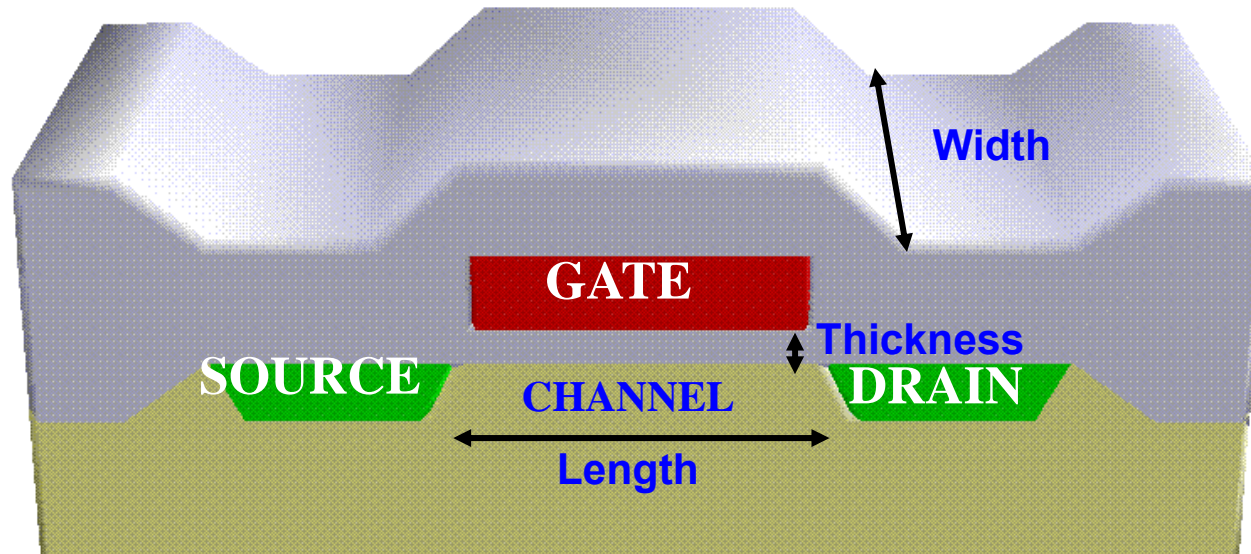
Based on material from
Prof. Jay Brockman, Joseph Nahas, University of Notre Dam
Prof. David Harris, Harvey Mudd College
<http://www.cmosvlsi.com/coursematerials.html>

Outline

- ❑ **CMOS Physical Structure**
- ❑ **Photolithography (Using light to define objects)**
 - ❖ **Positive**
 - ❖ **Negative**
- ❑ **Fabrication Overview**
- ❑ **Fabrication Step-by-Step**
 - ❖ **Etching (Removal of material)**
 - ❖ **Doping of Semiconductor (Adding donor and acceptors)**
 - ❖ **Deposition (Adding material on top of wafer)**
- ❑ **Newer Processes**

CMOS Cross Sections

MOS Transistor Cross-section



❑ Key Controlling Physical Parameters

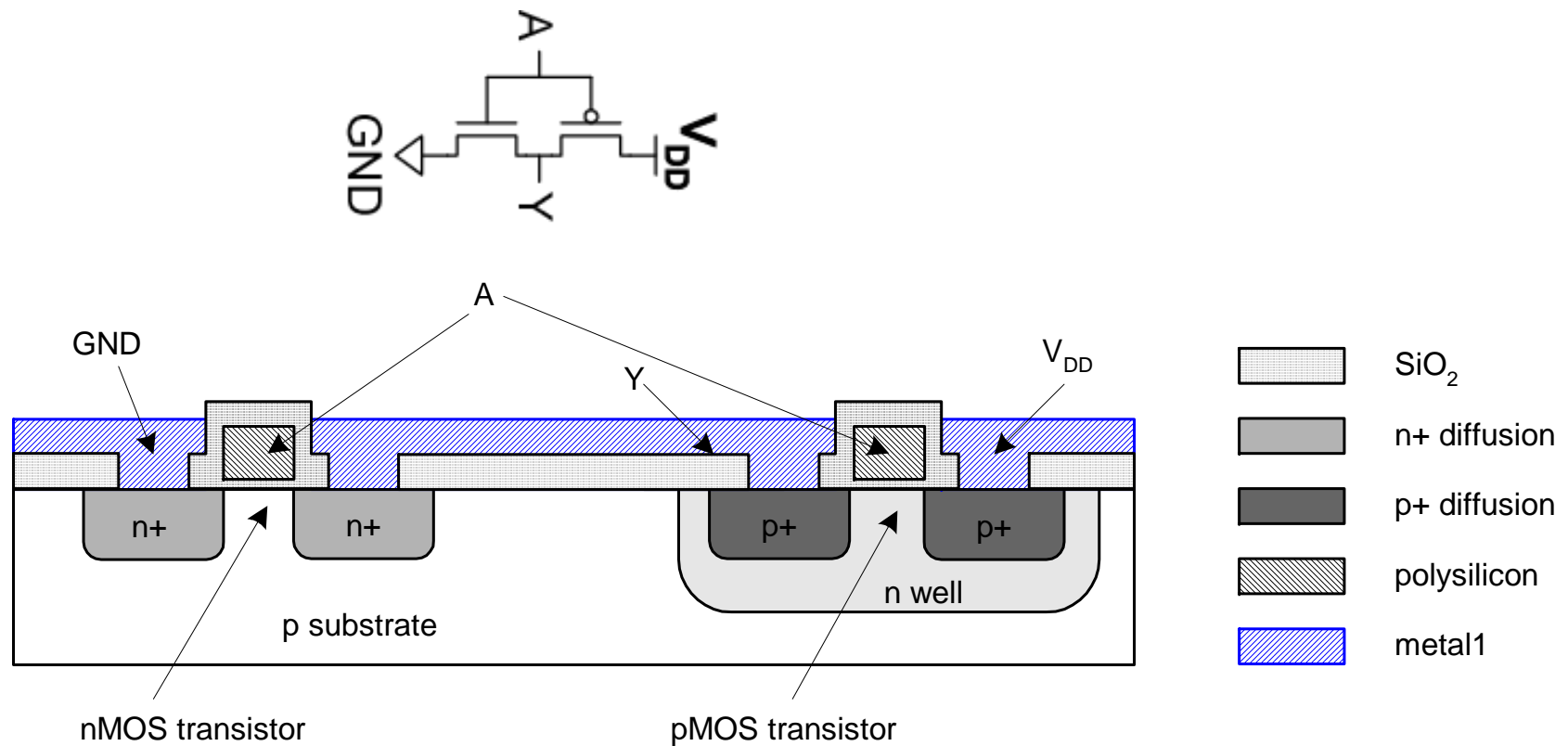
- ❖ **Length (L)** of channel
- ❖ **Width (W)** of Channel
- ❖ **Thickness (t_{ox})** of gate insulator

❑ Material types

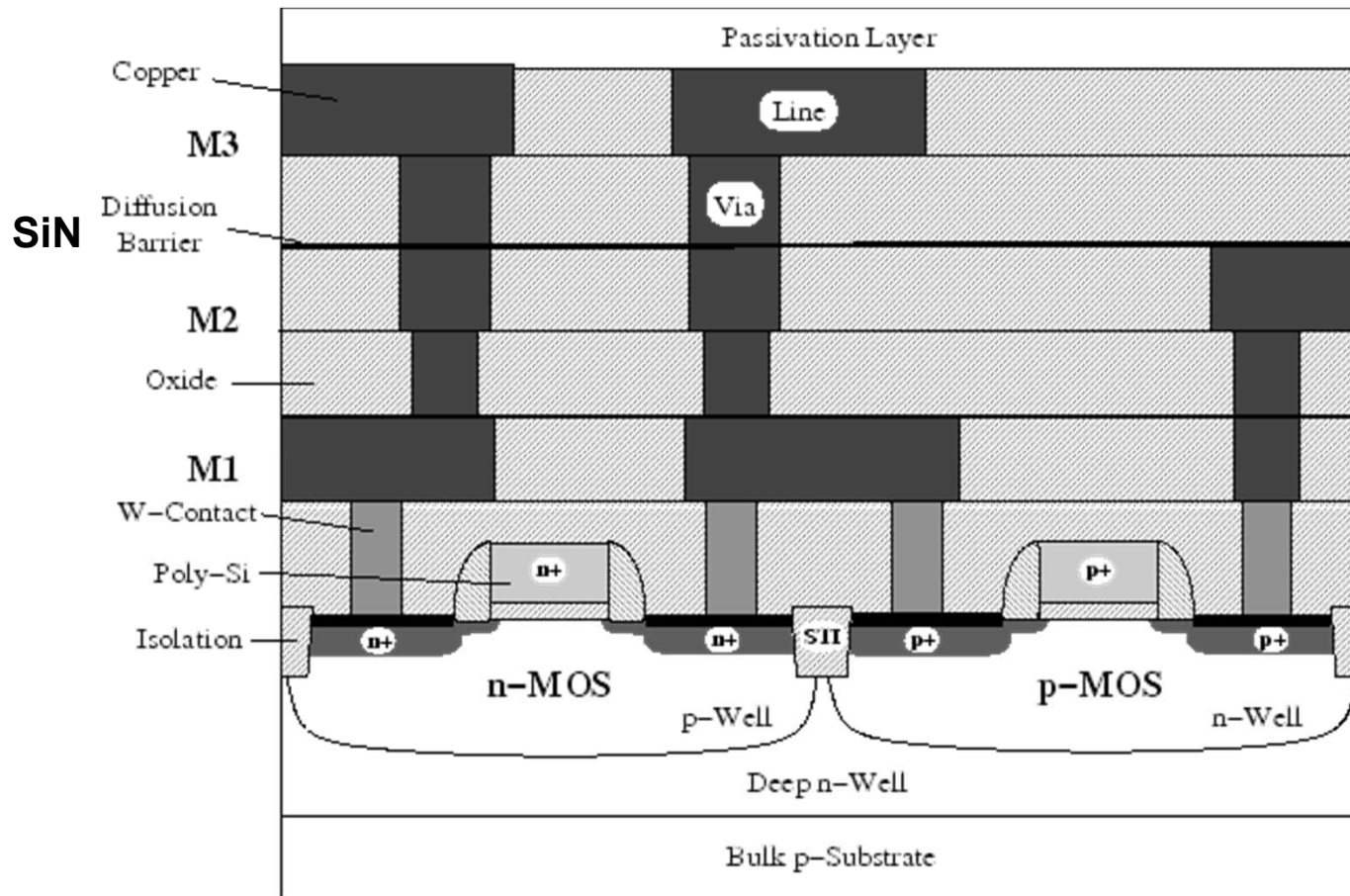
- ❖ **N-type:** Phosphorous doped to provide “free” electrons
- ❖ **P-type:** Boron doped to provide “free” positive holes

Inverter Cross-section

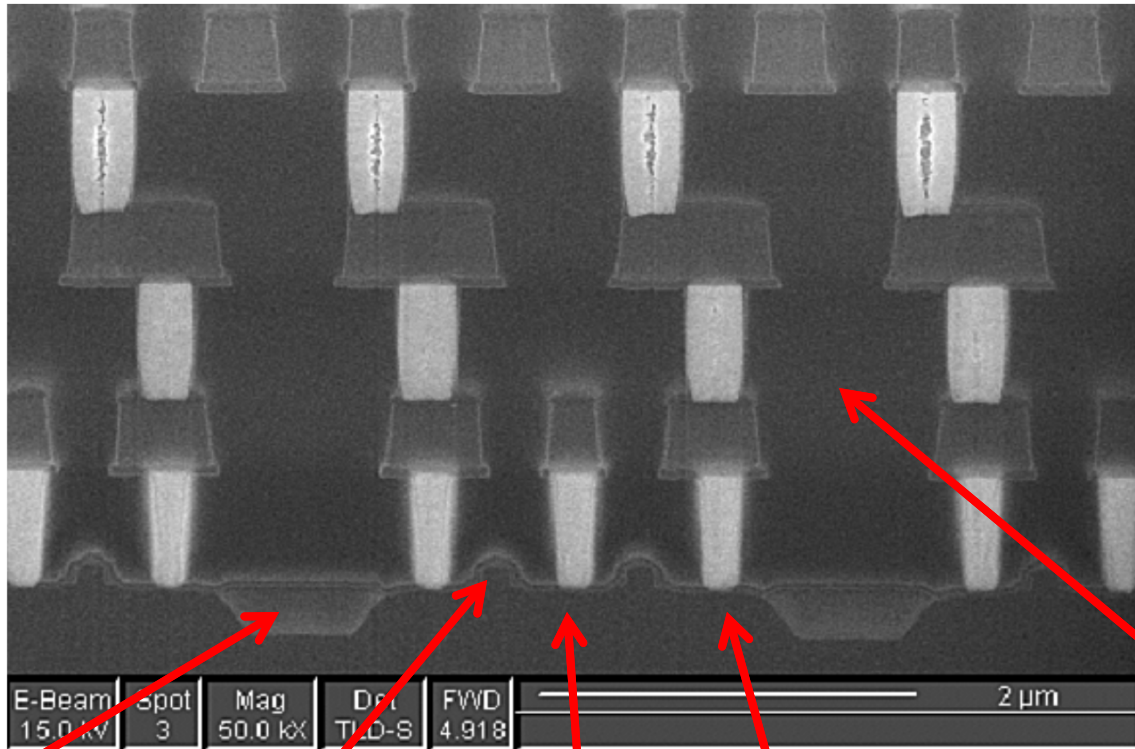
- ❑ Typically use *p-type substrate* for nMOS transistors
- ❑ Requires *n-well* for body of pMOS transistors



CMOS Technology Cross Section



TSMC 0.18 CMOS Cross Section



Al Metal 3
W Via 2
Al Metal 2
W Via 1
Al Metal 1
W Contact

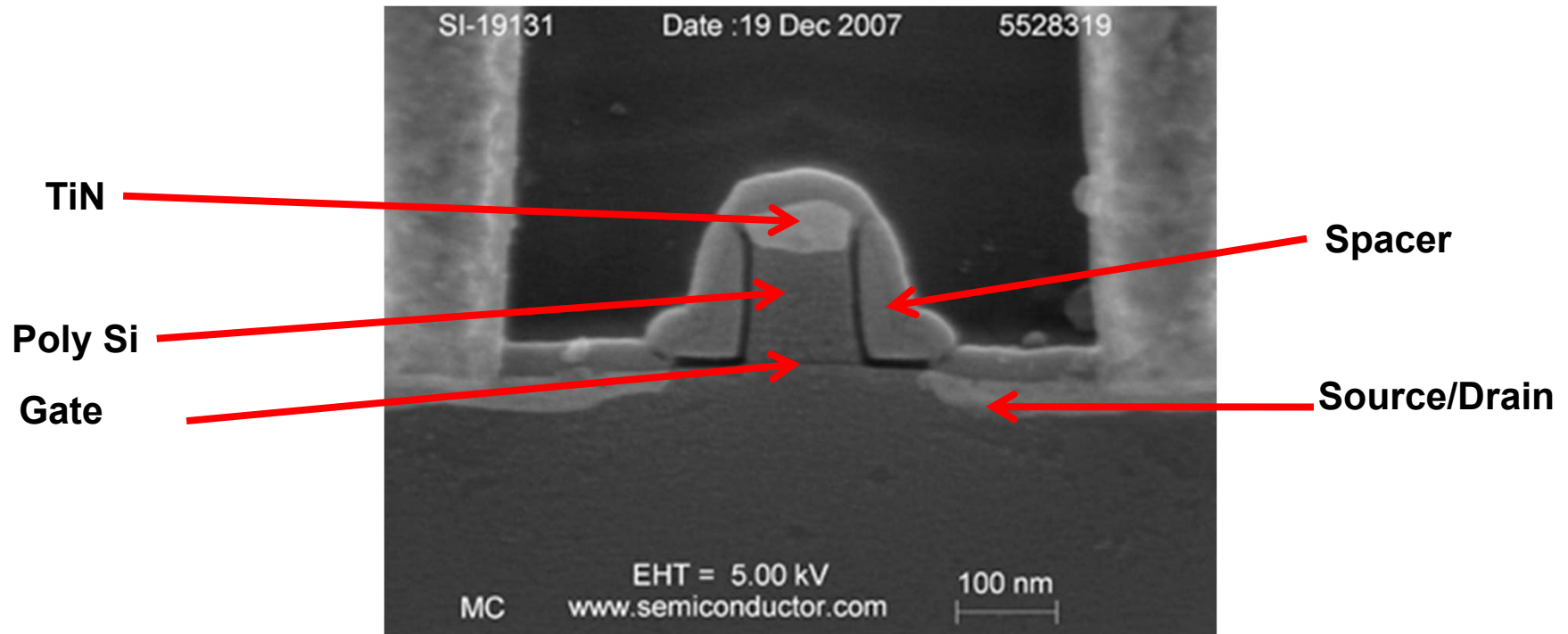
Shallow
Trench
Isolation
(STI)

Poly
Gate

Source
Drain

SiO₂

130 nm transistor

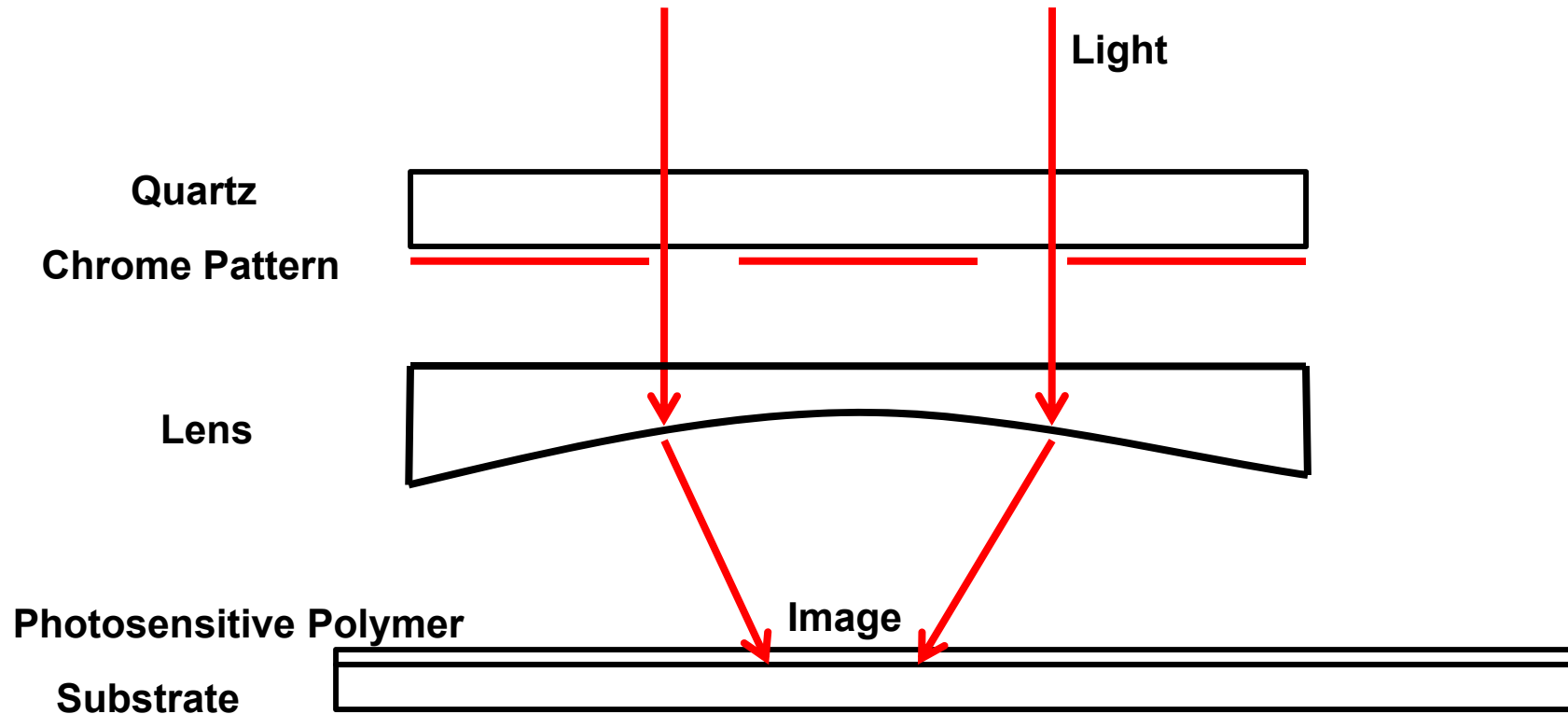


Photolithography

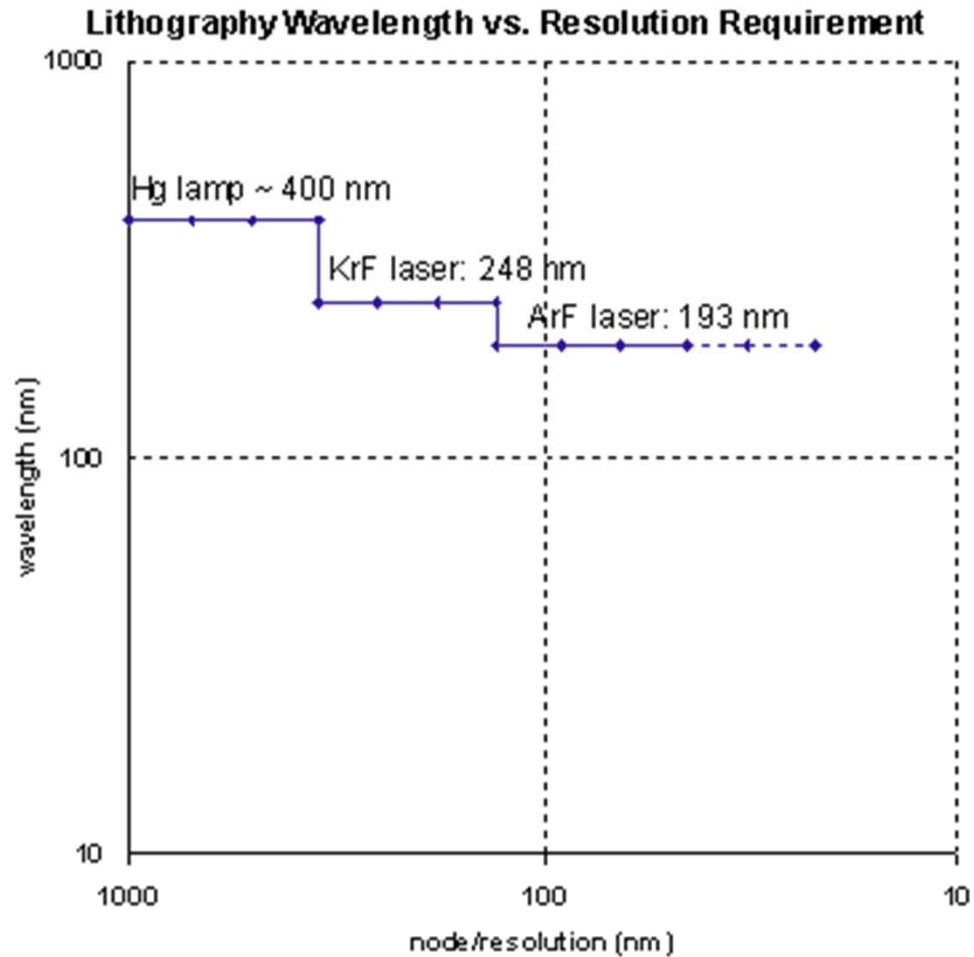
Photolithography

- ❑ Aka "*optical lithography*"
- ❑ Selectively remove parts of a
 - ❖ *thin film* on top of a substrate
 - ❖ or the *bulk* of a substrate.
- ❑ Uses light to transfer geometric pattern
 - ❖ from photo mask
 - ❖ to light-sensitive chemical photo resist, ("*resist*"), on the substrate.
- ❑ Series of chemical treatments engraves exposure pattern into material underneath the photo resist.

Exposure



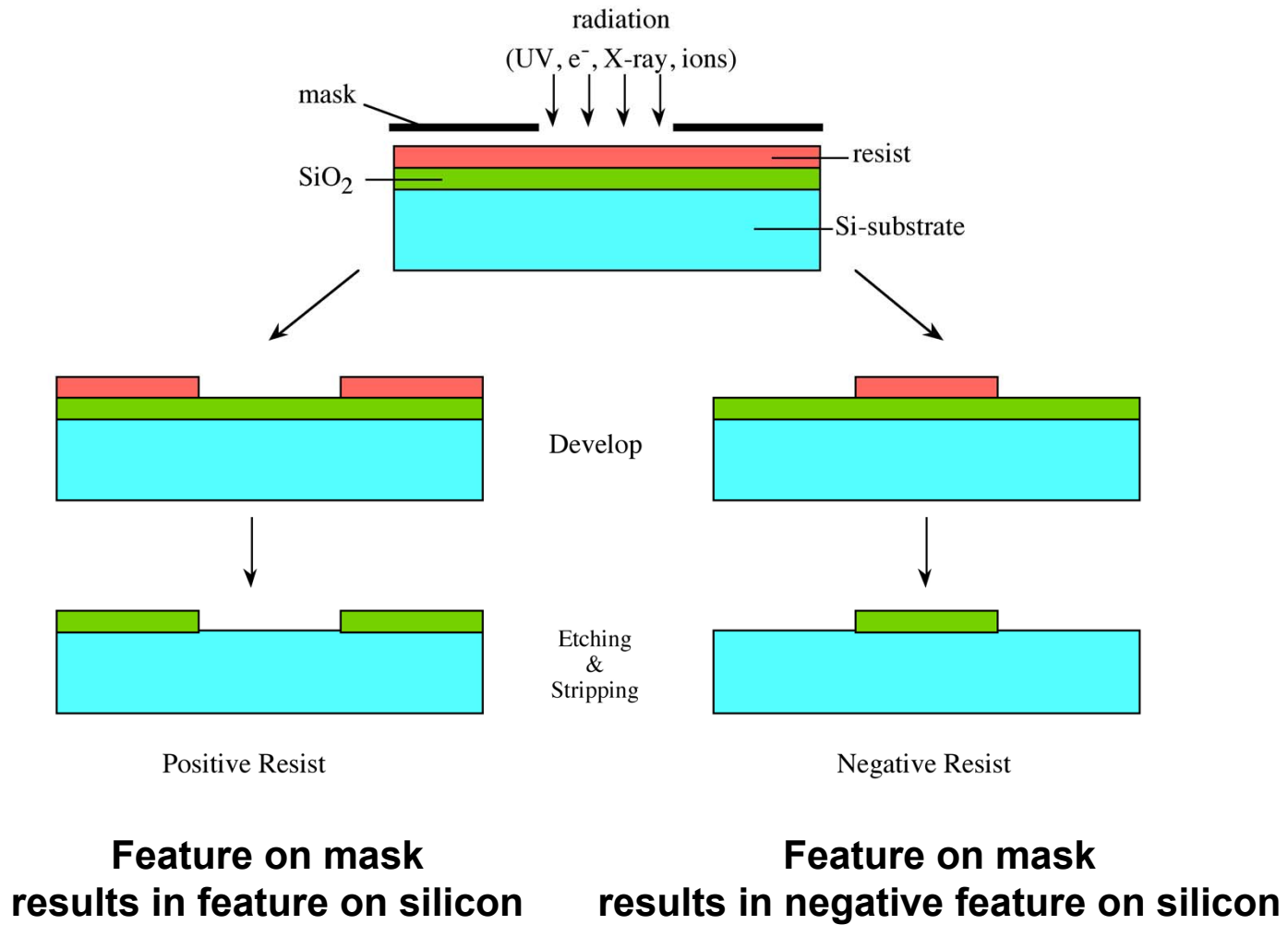
Photolithography Light



Photolithography

- ❑ **Process of transferring geometric shapes on a *mask* (quartz glass plate) to the surface of a silicon wafer.**
- ❑ **Mask is created using a photolithographic process with an electron beam to scan the images on the plate.**

Photolithography

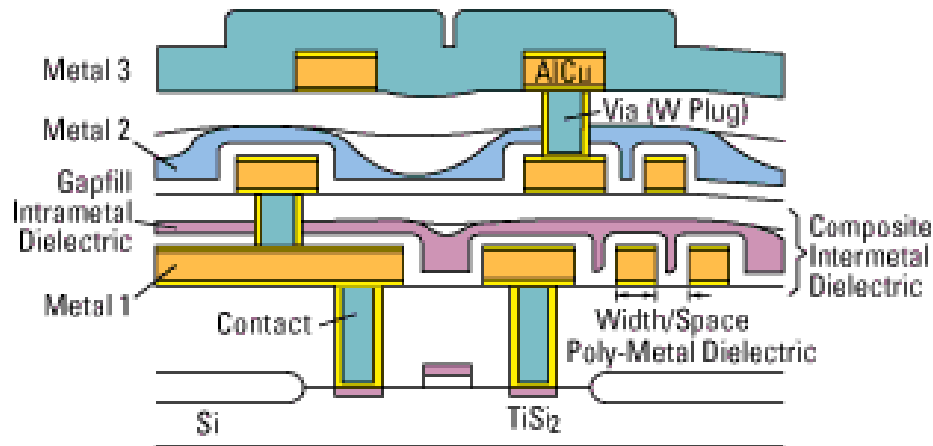


Fabrication Overview

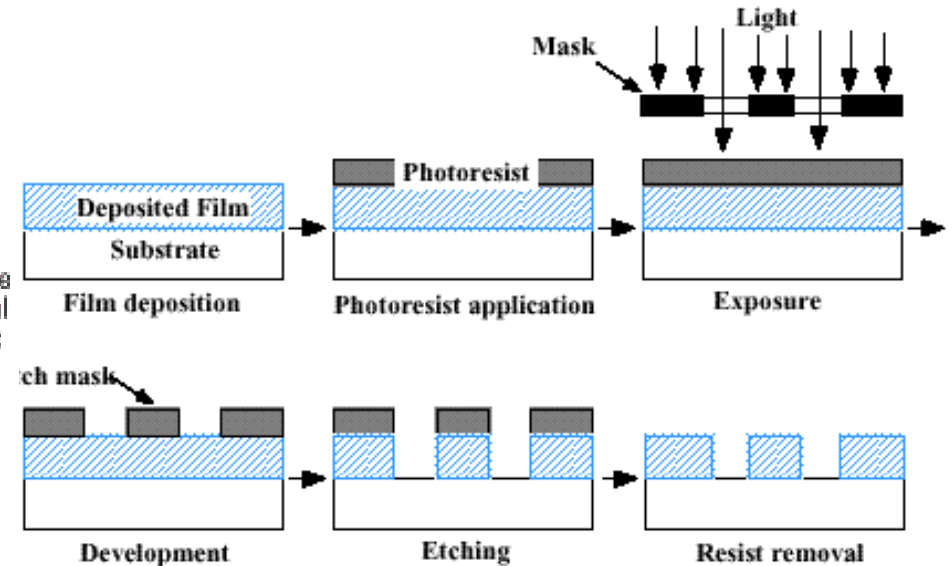
CMOS Fabrication

- ❑ CMOS transistors fabricated on silicon *wafer*
 - ❖ One wafer contains tens to thousands of chips
 - ❖ Today wafers are up to 300 mm across
- ❑ *Photolithography* process “prints” patterns on the wafer.
- ❑ On each step, different materials are *deposited* or *etched*
- ❑ Easiest to understand: view both *top* and *cross-section* of wafer in a simplified manufacturing process, circa **1980**.

CMOS Chips In Cross Section



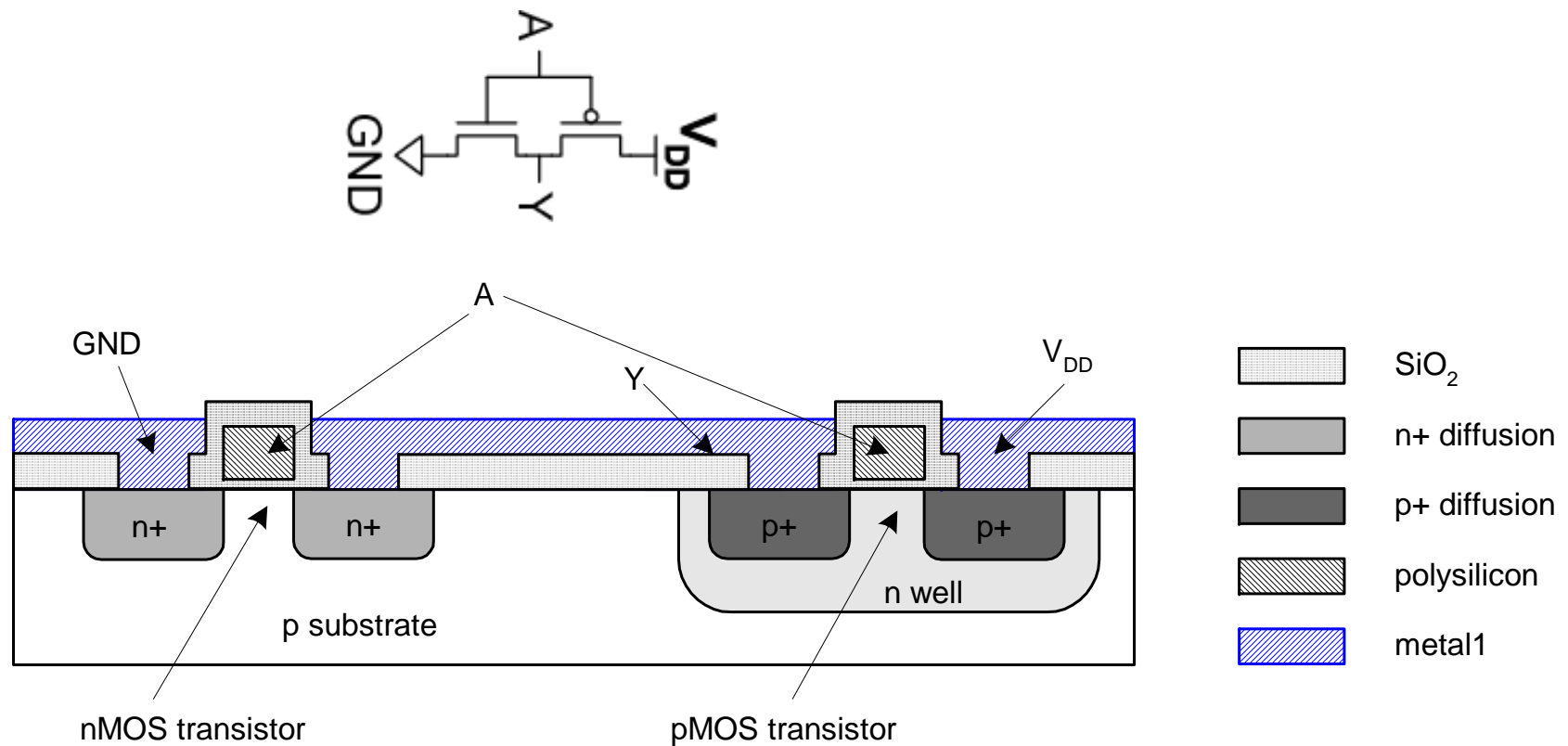
<http://www.engr.sjsu.edu/WofMatE/images/intercon.gif>



<http://www.hitequest.com/Kiss/photolithography.gif>

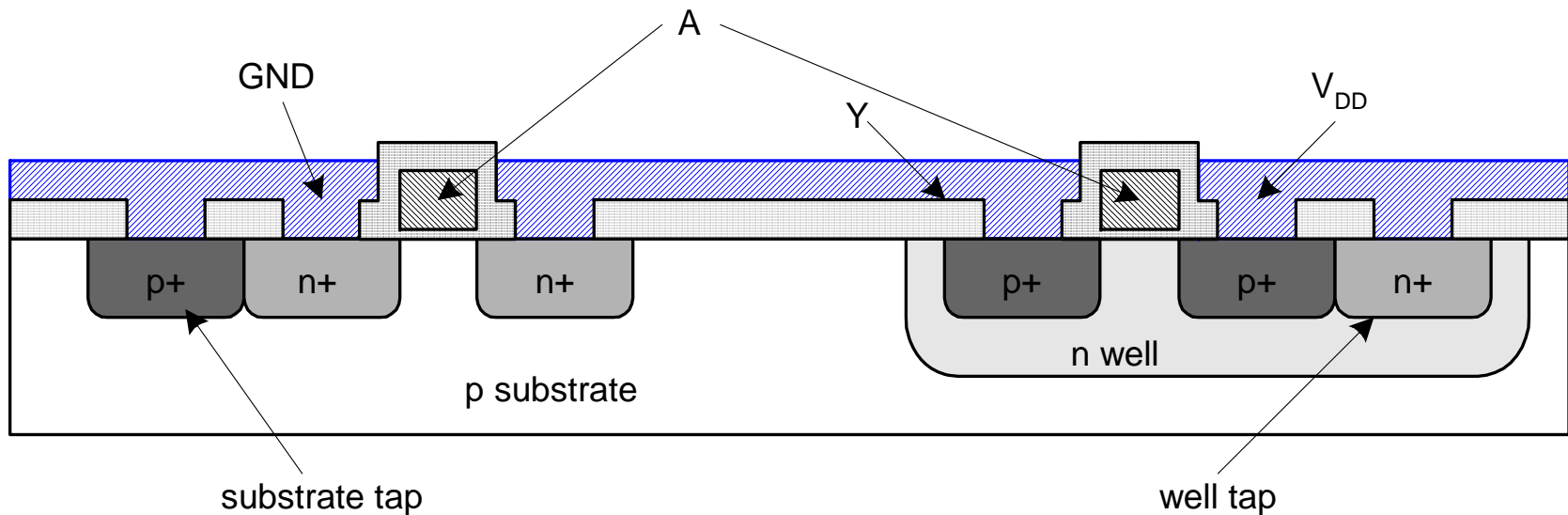
Inverter Cross-section

- ❑ Typically use *p-type substrate* for nMOS transistors
- ❑ Requires *n-well* for body of pMOS transistors



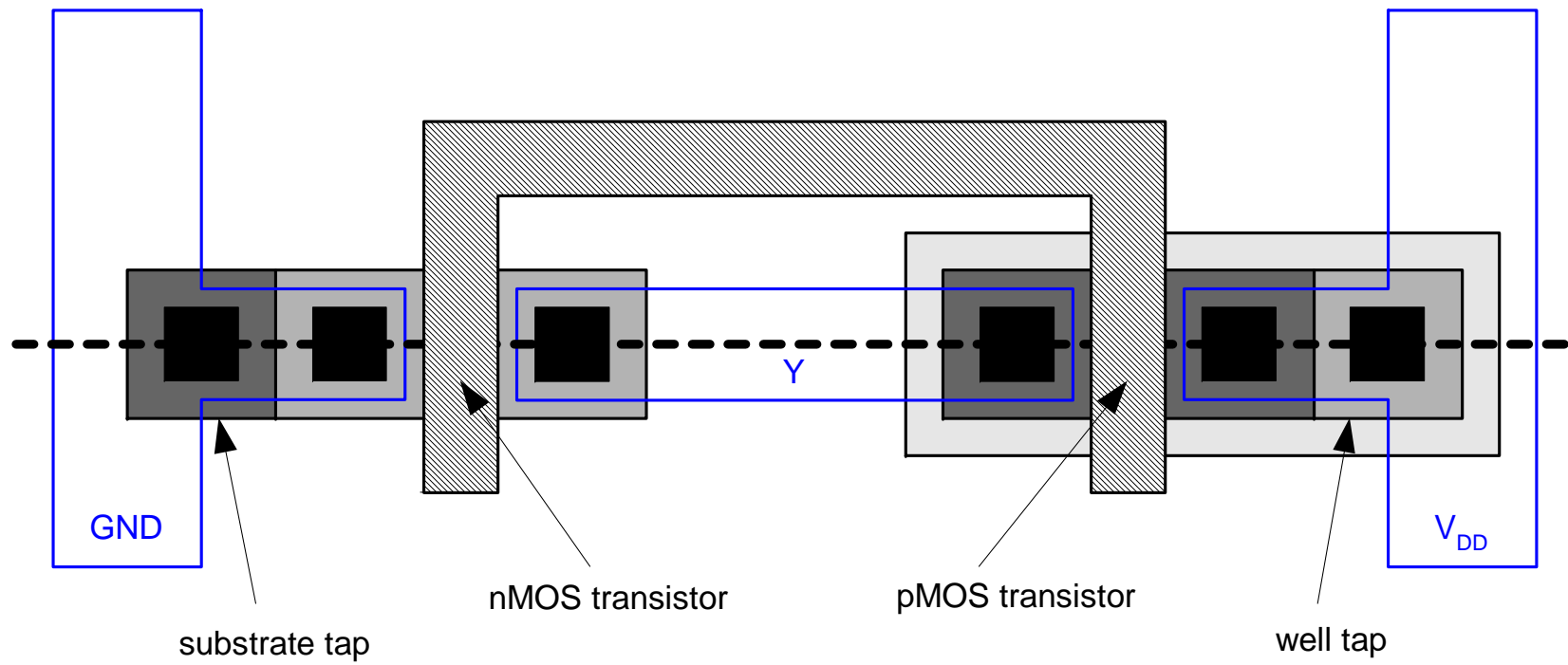
Well and Substrate Taps

- ❑ Process circa 1980
 - ❖ Modern processes much more complicated but more robust.
- ❑ Substrate must be tied to GND and n-well to V_{DD}
- ❑ Metal to lightly-doped semiconductor forms poor connection called *Schottky Diode*
 - ❖ Very low threshold voltage
- ❑ Use heavily doped well and substrate contacts / taps



Inverter 6 Mask Set

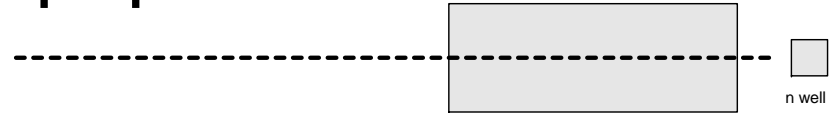
- ❑ Transistors and wires are defined by sets of *masks*
 - ❖ 2D pattern selectively allows/blocks access to chip surface
 - ❖ Each mask controls one kind of structure
- ❑ Two views will be shown in the following slides
 - ❖ Mask view
 - ❖ *Vertical cross-section* taken along dashed line (see previous slide)



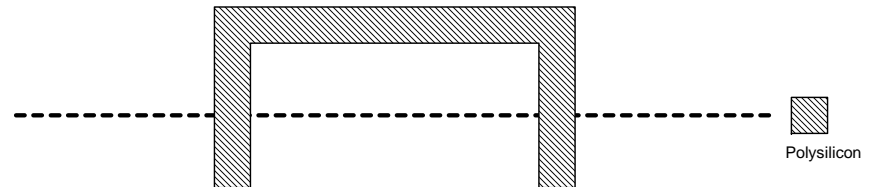
Mask Views

❑ Six masks for a very simple process

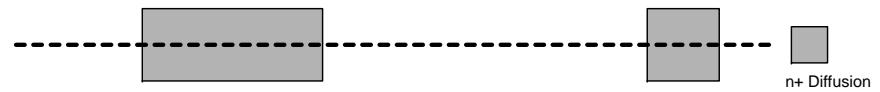
❖ n-well



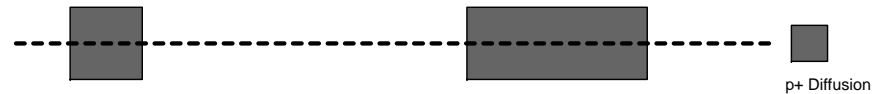
❖ Polysilicon



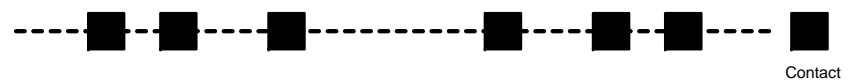
❖ n+ diffusion



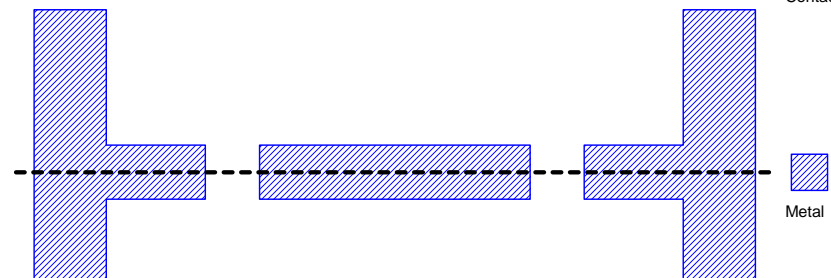
❖ p+ diffusion



❖ Contact

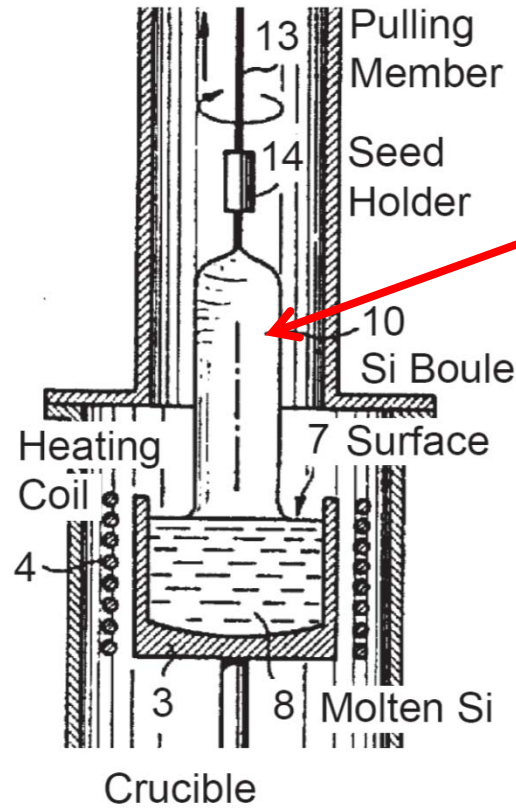


❖ Metal



Fabrication Step by Step

Silicon Growth



**Single
Crystal of
Silicon**

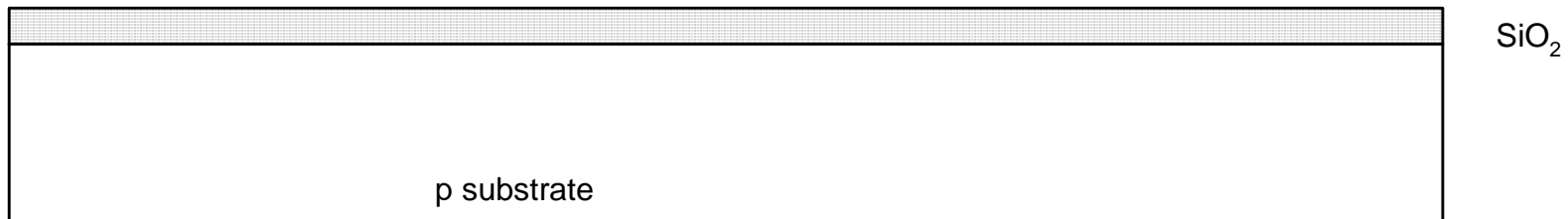
Fabrication Steps

- ❑ **Start with blank wafer**
- ❑ **Build inverter from the bottom up**
- ❑ **First step will be to form the n-well**
 - ❖ **Cover wafer with protective layer of SiO_2 (oxide)**
 - ❖ **Remove layer where n-well should be built**
 - ❖ **Implant or diffuse n dopants into exposed wafer**
 - ❖ **Strip off SiO_2**



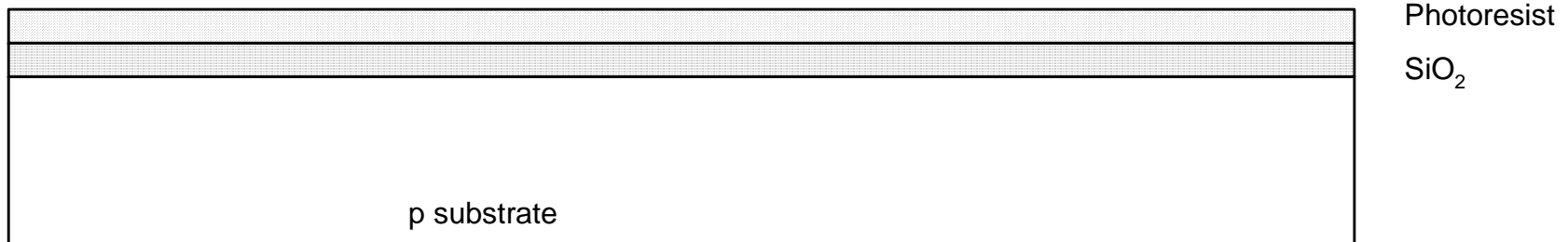
n-well: Oxidation

- **Grow SiO₂ on top of Si wafer**
 - ❖ **900 – 1200 C with H₂O or O₂ in oxidation furnace**



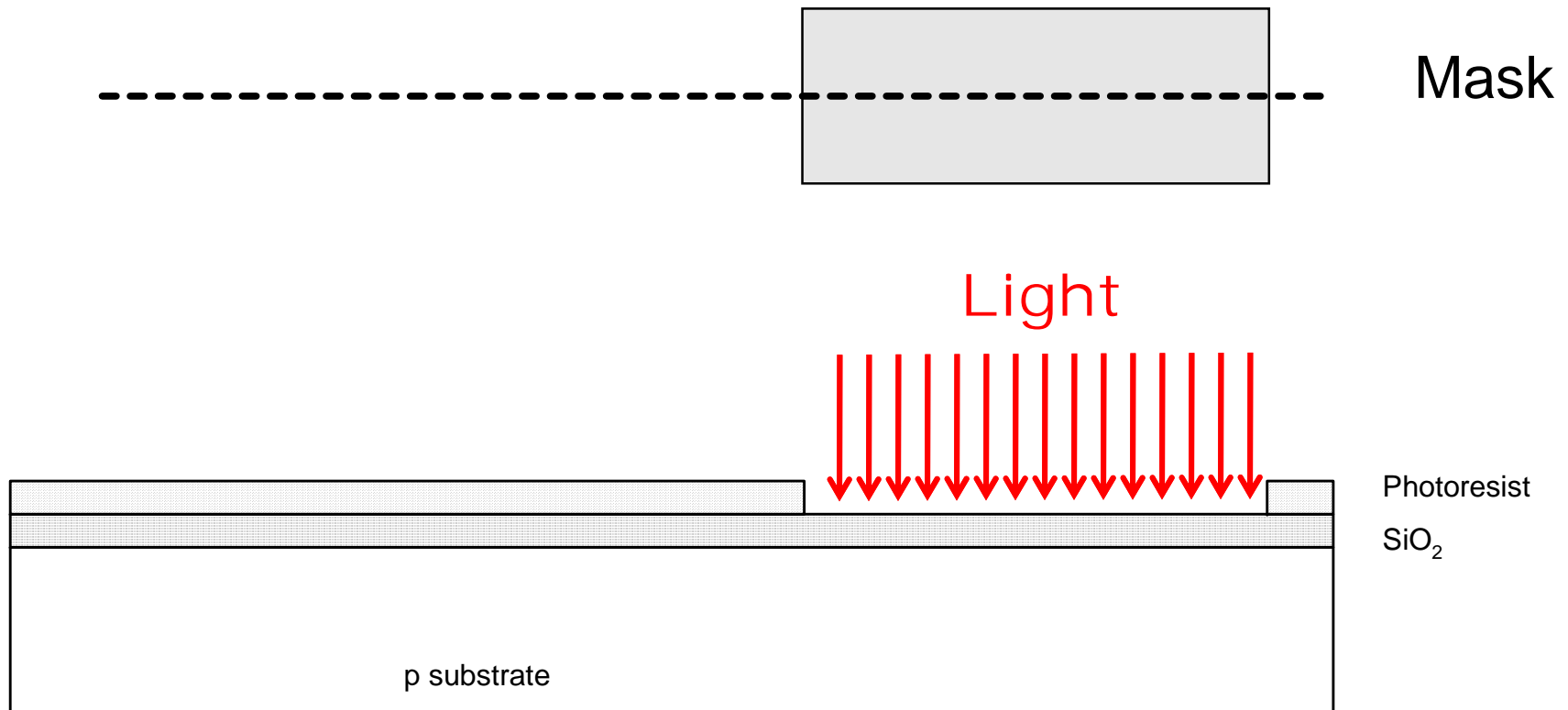
n-well: Photoresist

- ❑ Spin on *photoresist*
 - ❖ Photoresist is a light-sensitive organic polymer
 - ❖ Softens (positive) or hardens (negative) where exposed to light



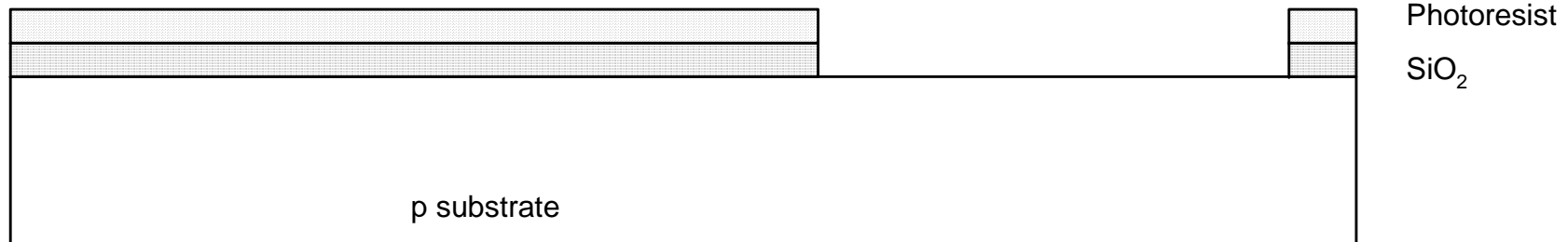
n-well: Lithography

- ❑ Expose photoresist through n-well mask
- ❑ Strip off exposed photoresist

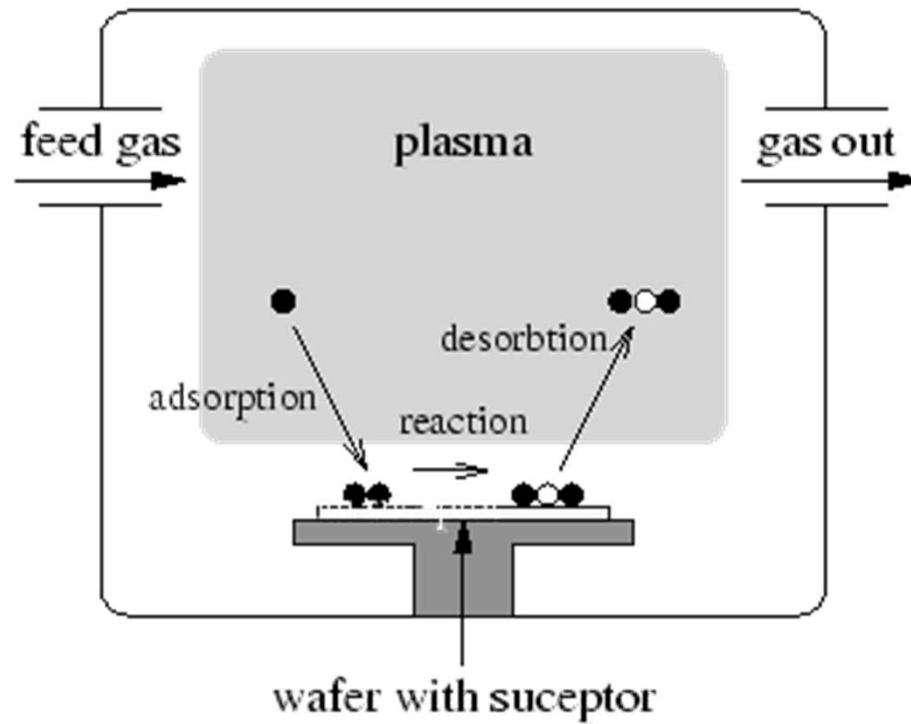


n-well: Etch

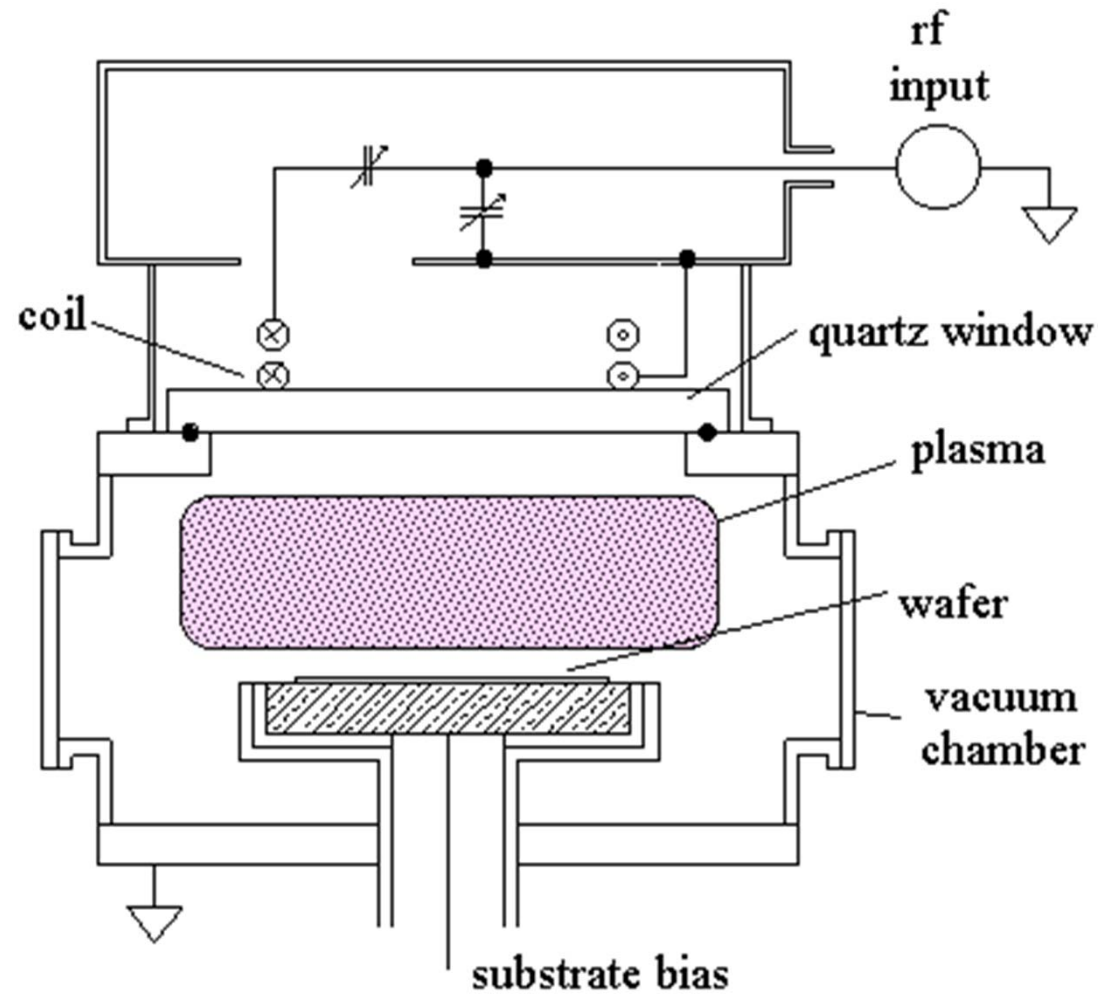
- ❑ Etch oxide with hydrofluoric acid (HF)
 - ❖ Seeps through skin and eats bone; nasty stuff!!!
- ❑ Dry etch using plasma etch (CF_4)
- ❑ Only attacks oxide where resist has been exposed



Plasma Etching

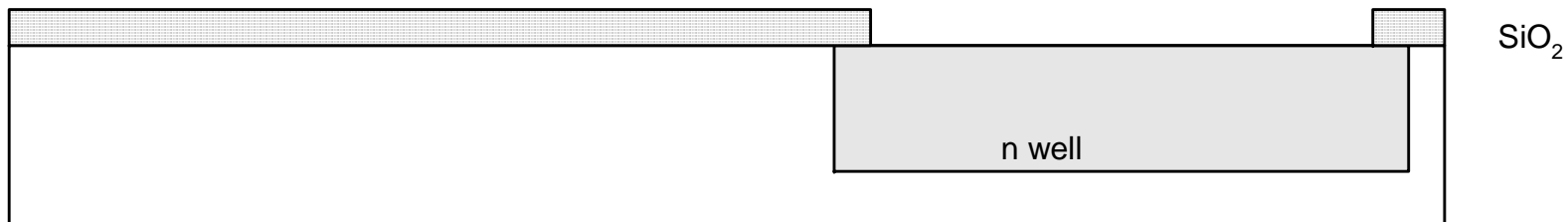


Plasma Etcher

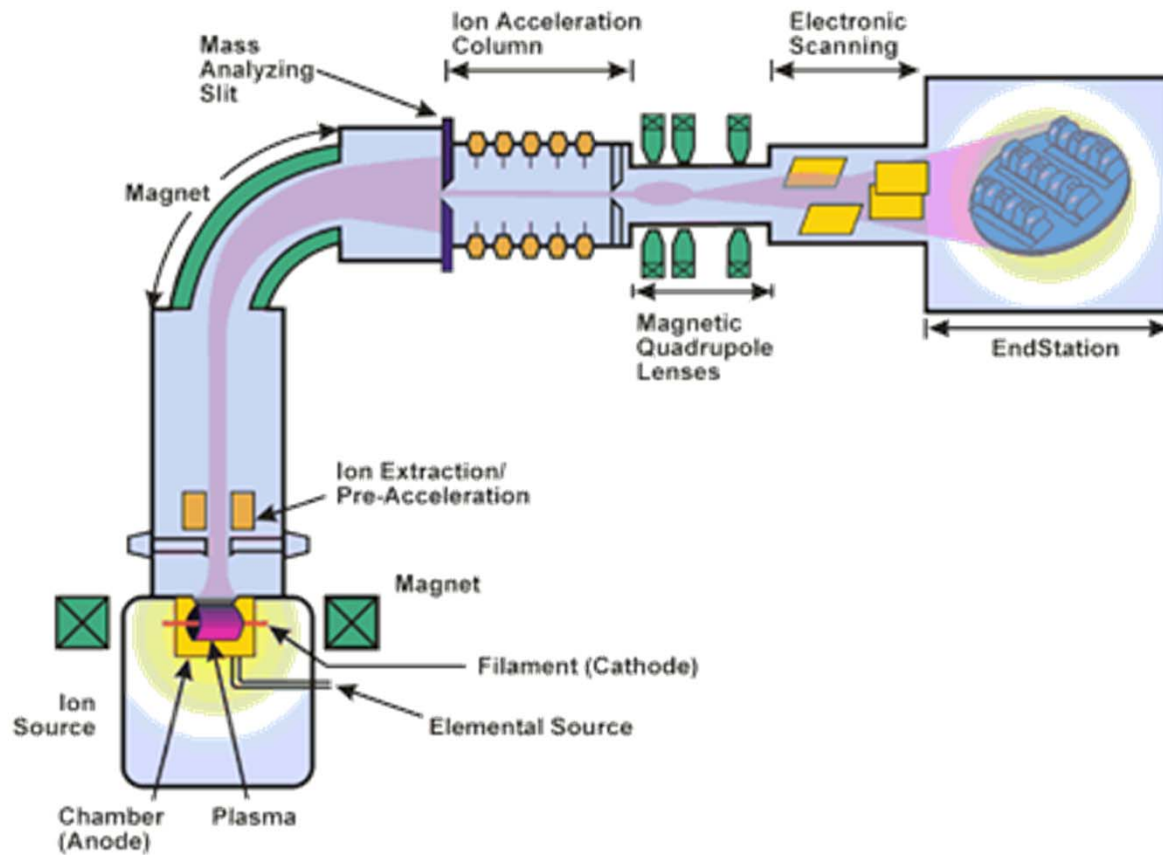


n-well: Diffusion

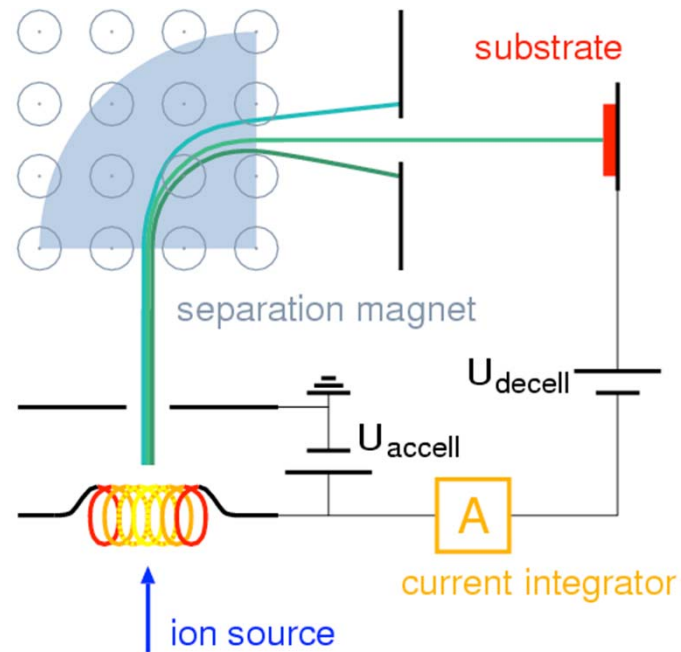
- ❑ n-well is formed with *diffusion* or *ion implantation*
- ❑ Diffusion
 - ❖ Place wafer in furnace with arsenic (As) gas
 - ❖ Heat until As atoms diffuse into exposed Si
- ❑ Ion Implantation
 - ❖ Blast wafer with beam of As ions
 - ❖ Ions blocked by SiO_2 , only enter exposed Si



Ion Implantation



Ion Implantation



□ Parameters

❖ Acceleration Voltage

- Determines depth of implant

❖ Integrated Current – Charge

- Determines amount of implant

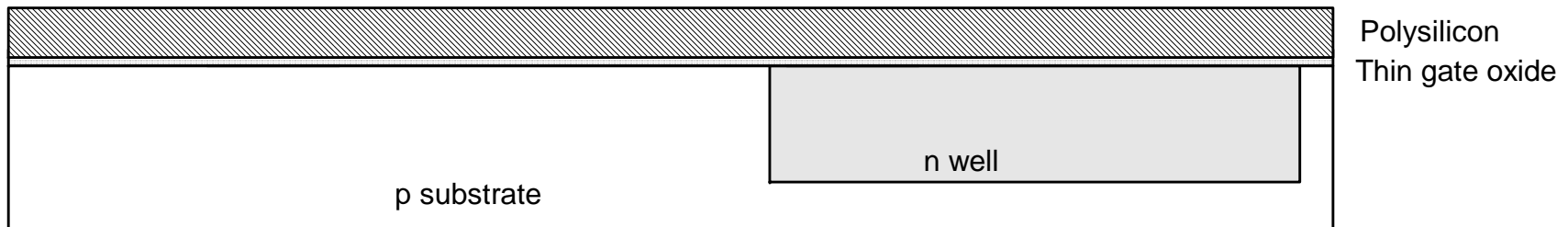
n-well: Strip Oxide

- ❑ Strip off the remaining oxide using HF
- ❑ Back to bare wafer with n-well
- ❑ Subsequent steps involve similar series of steps

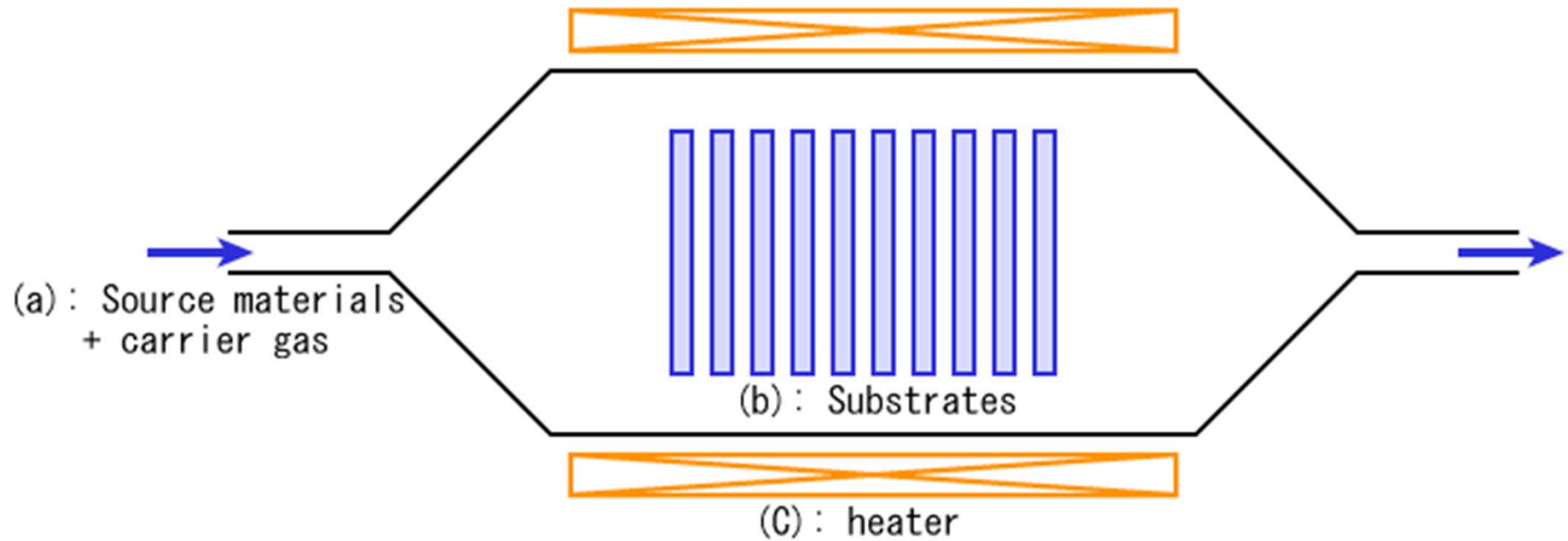


Forming the Gates

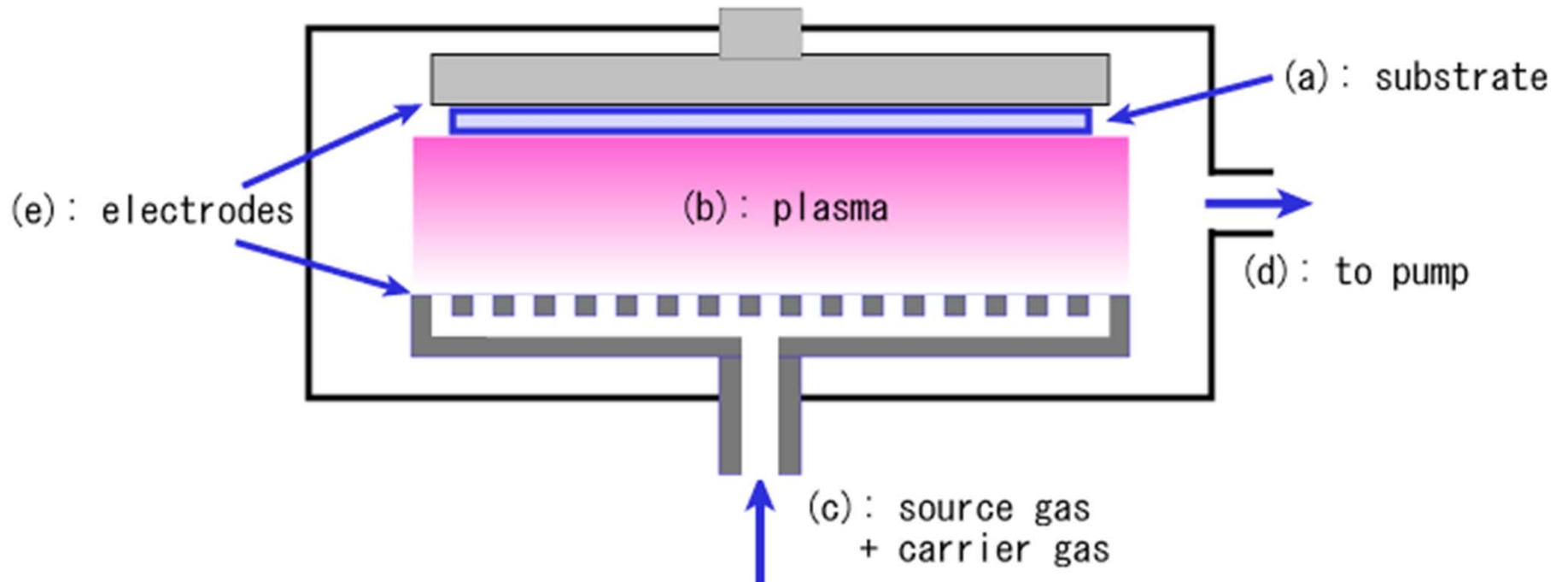
- ❑ Deposit very thin layer of *gate oxide*
 - ❖ $< 20 \text{ \AA}$ (6-7 atomic layers)
- ❑ *Chemical Vapor Deposition (CVD)* of silicon layer
 - ❖ Place wafer in furnace with Silane gas (SiH_4)
 - ❖ Forms many small crystals called polysilicon
 - ❖ Heavily doped to be good conductor
- ❑ When the acronym “MOS” was invented, Al was used for the gate, instead of polysilicon.
- ❑ In 45 nm technology, metal gates and hafnium oxide are used.



Batch CVD

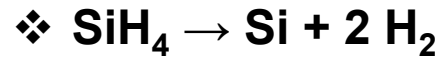


Plasma Assisted CVD

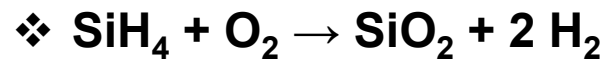


CVD Reactions

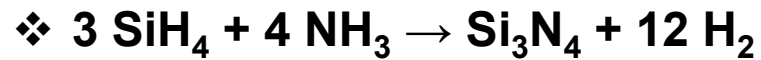
- ❑ **Silicon**



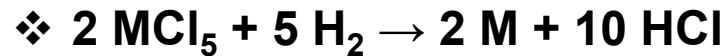
- ❑ **Silicon Dioxide**



- ❑ **Silicon Nitride**

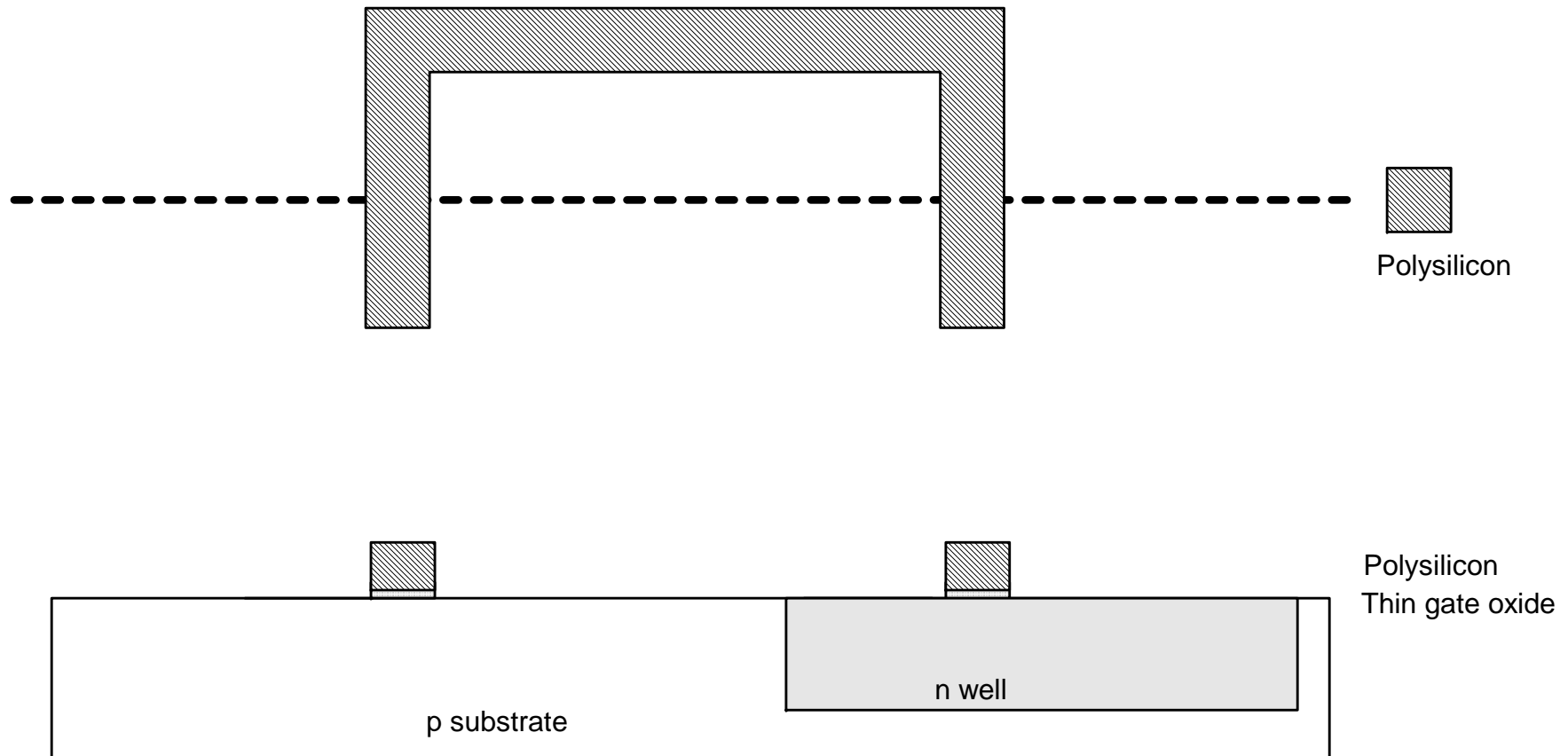


- ❑ **Metal**



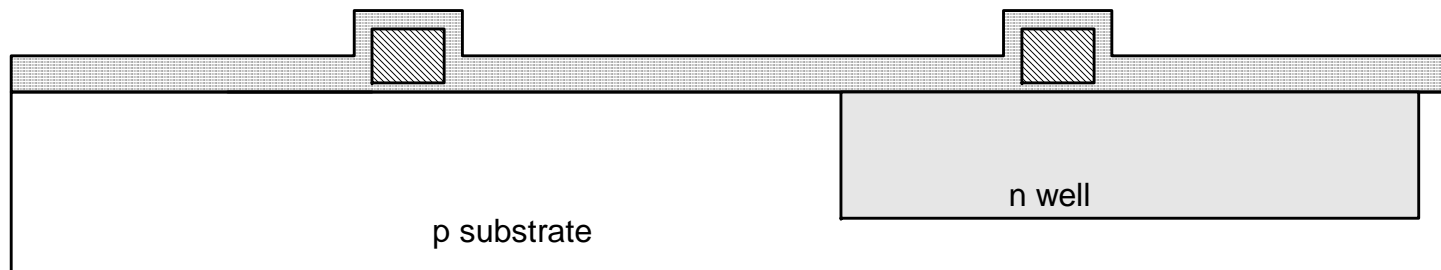
Gate: Polysilicon Patterning

- Use same lithography process to pattern *polysilicon*



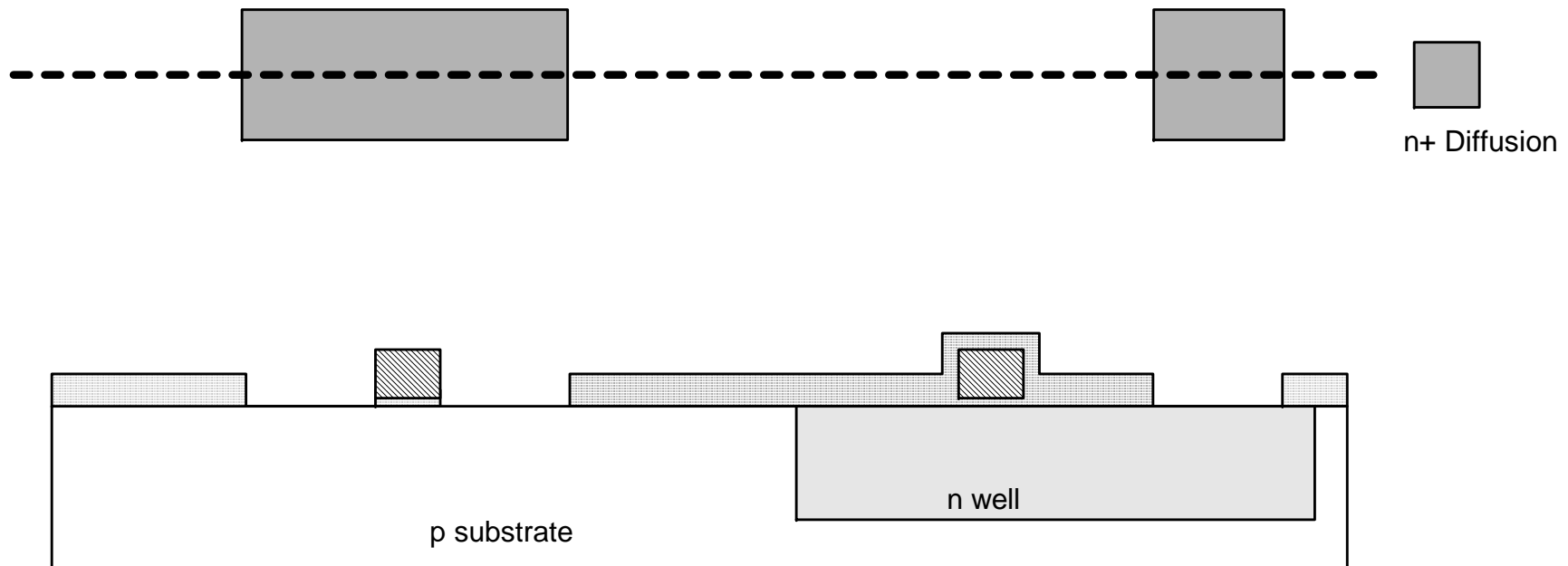
Transistor formation: Self-Aligned Process

- ❑ Use oxide and masking to expose where n+ dopants should be diffused or implanted
- ❑ N-diffusion forms nMOS source, drain, and n-well contact



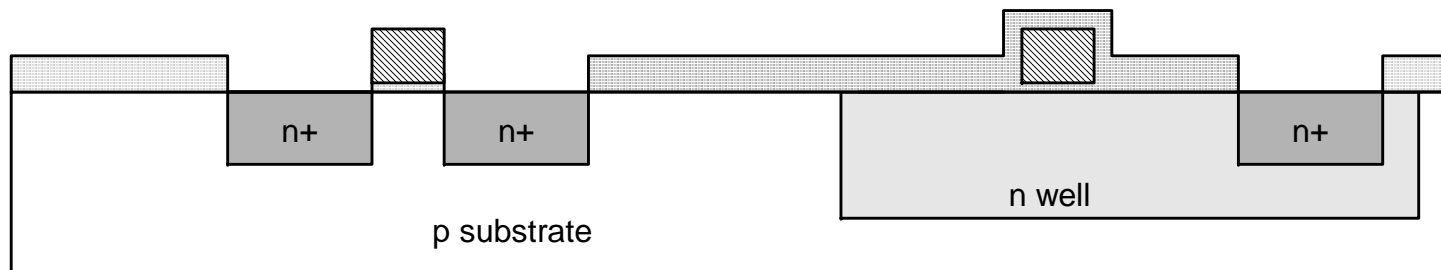
Transistor: N-diffusion

- ❑ Pattern oxide and form n+ regions
- ❑ *Self-aligned process* where gate blocks diffusion
- ❑ Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



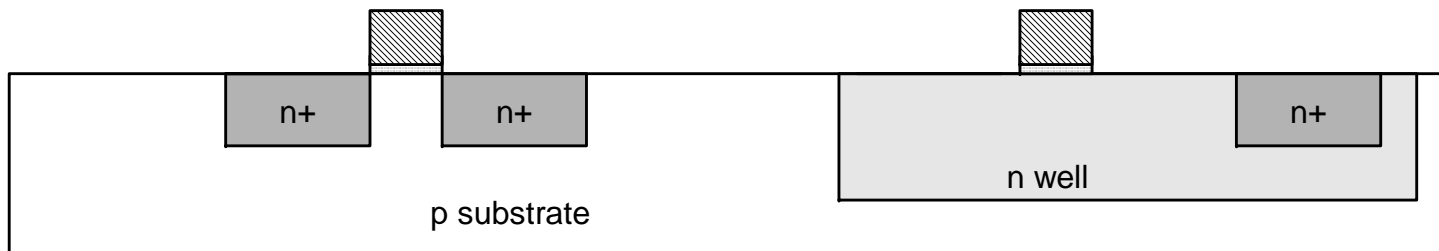
Transistor: N-diffusion cont.

- ❑ Historically dopants were diffused
- ❑ Usually ion implantation today
- ❑ But regions are still called diffusion



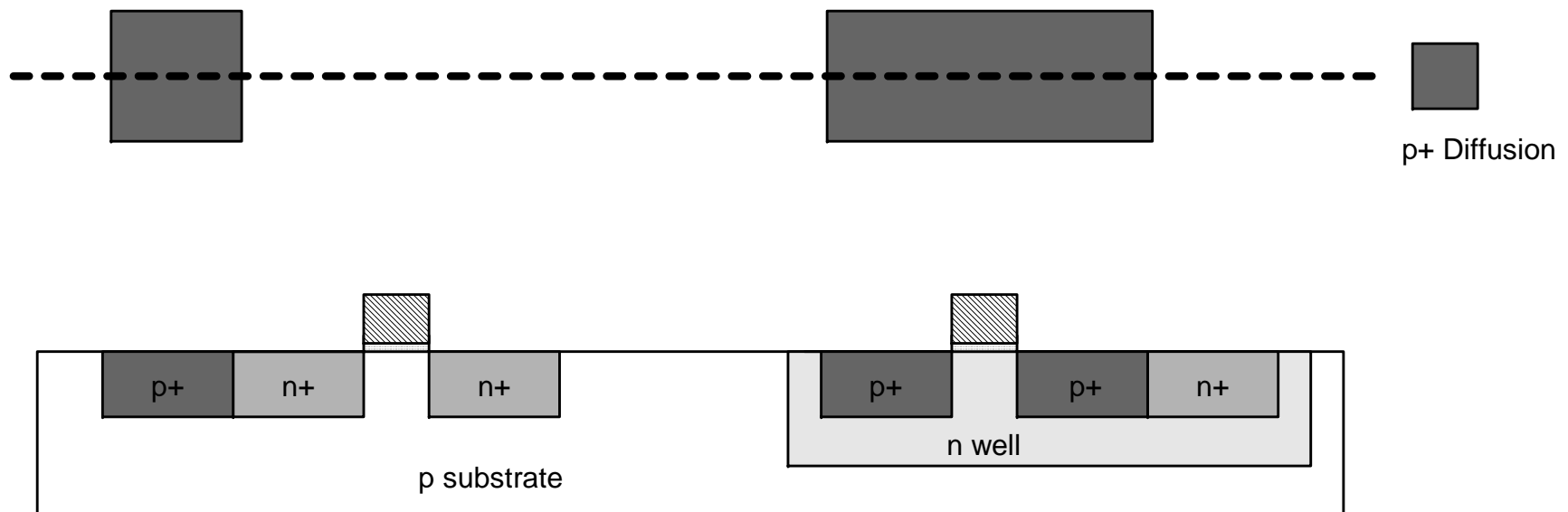
Transistor: N-diffusion cont.

- ❑ Strip off oxide to complete patterning step



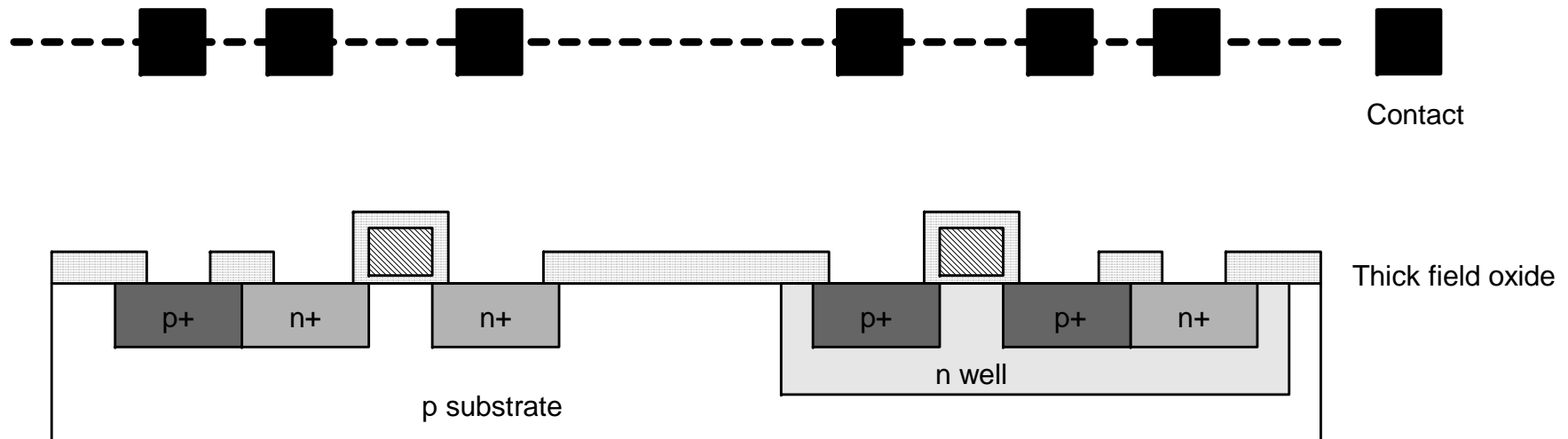
Transistor: P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



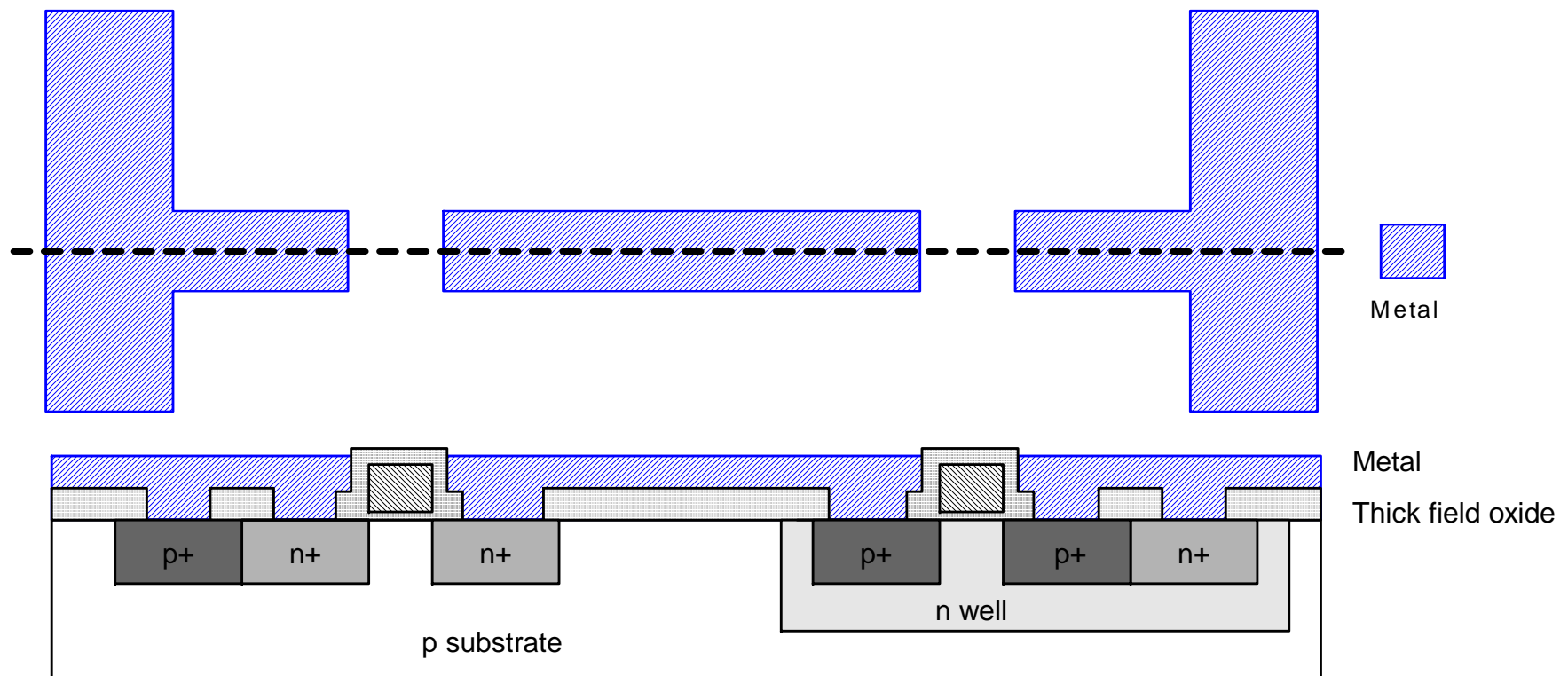
Forming Contacts

- ❑ Now we need to wire together the devices
- ❑ Cover chip with thick field oxide
- ❑ Etch oxide where contact cuts are needed

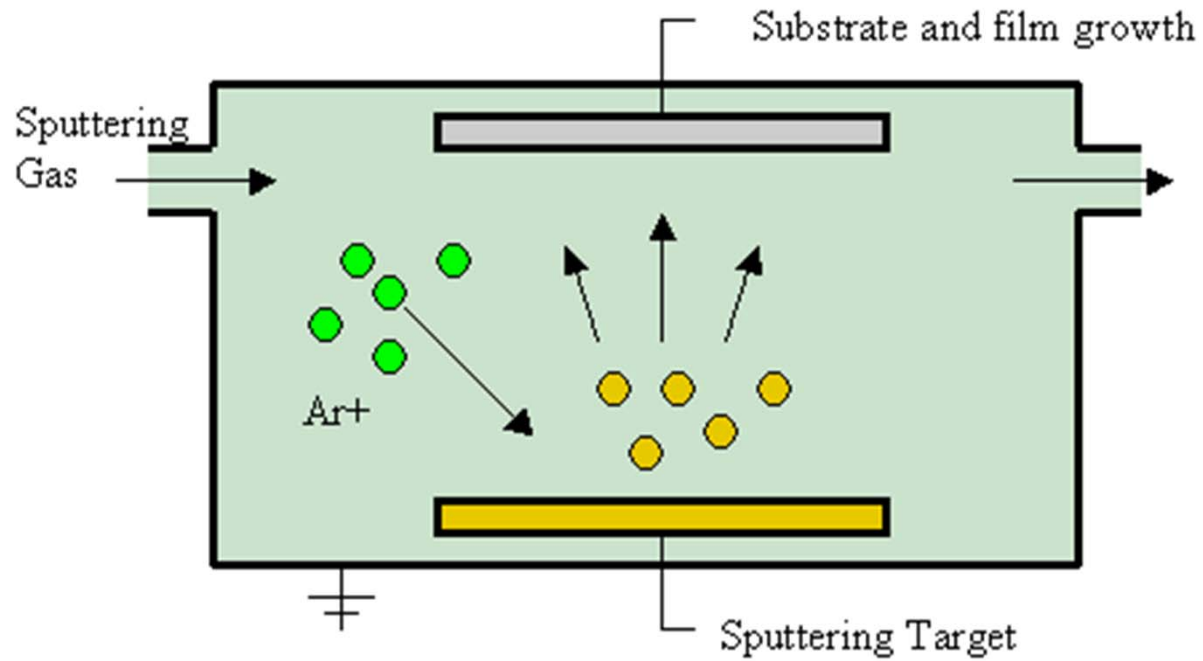


Metalization

- ❑ Sputter on aluminum over whole wafer
- ❑ Pattern to remove excess metal, leaving wires



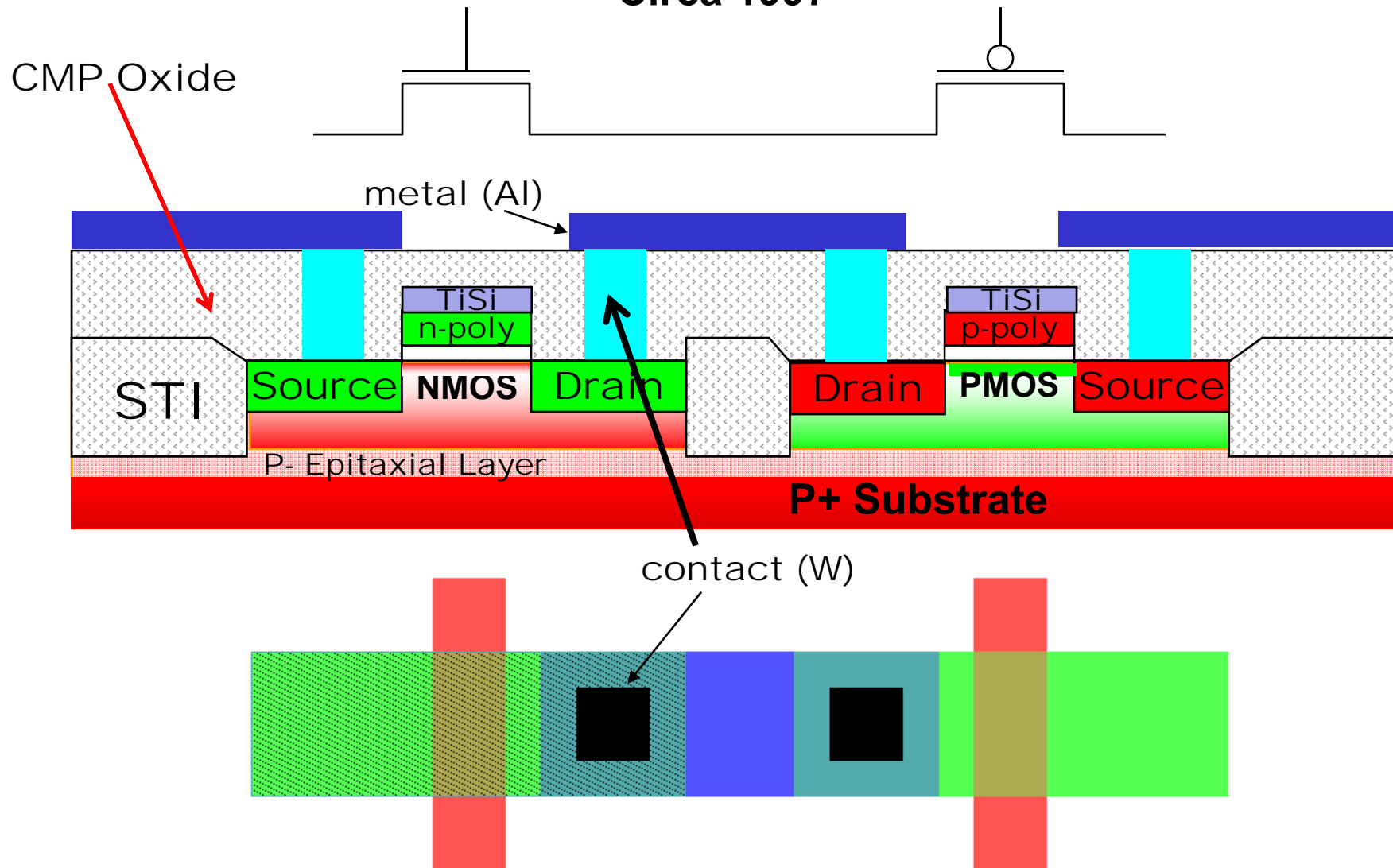
Sputter Deposition



Advanced Processes

Twin Tub CMOS w/STI & Al-W metal

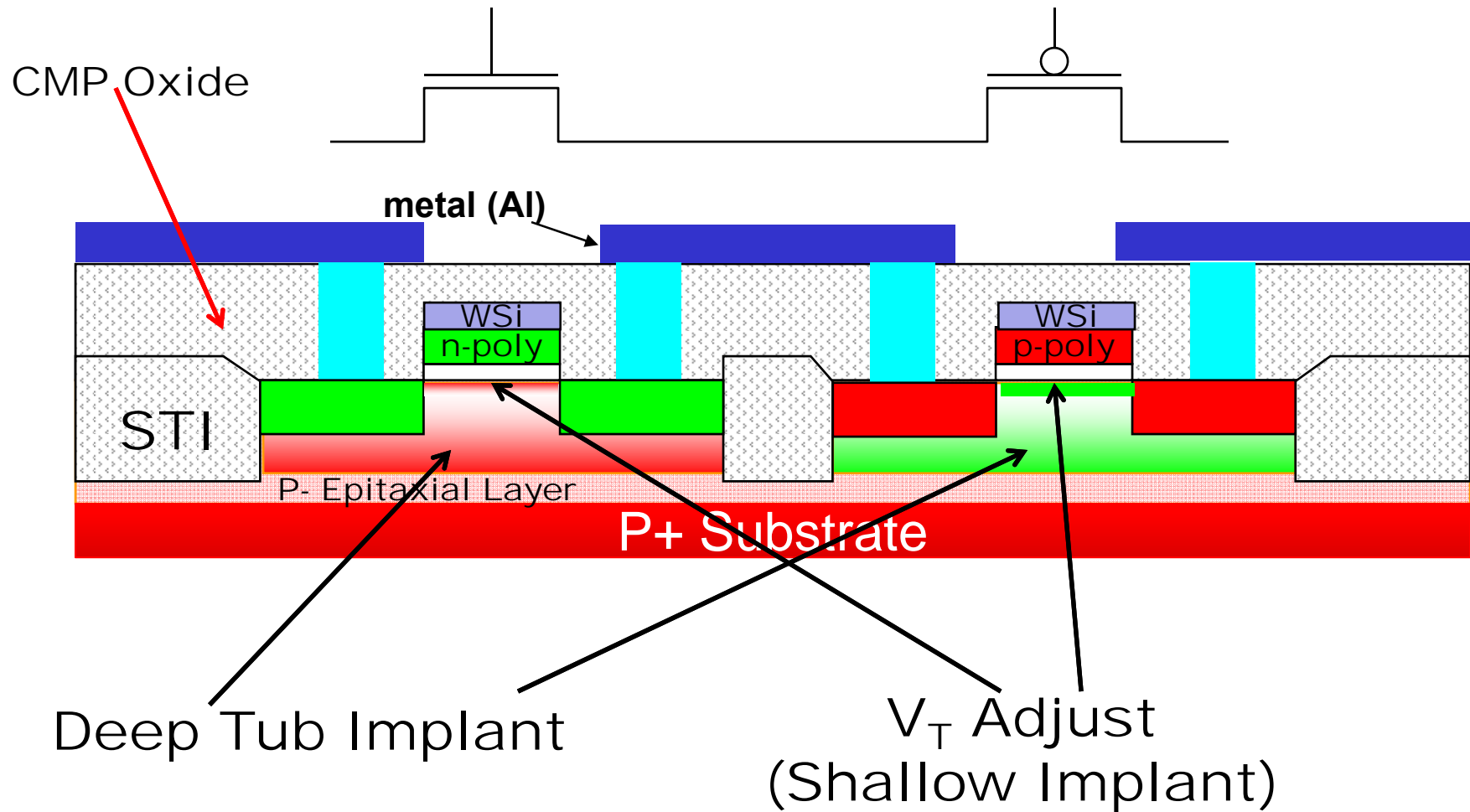
Circa 1997



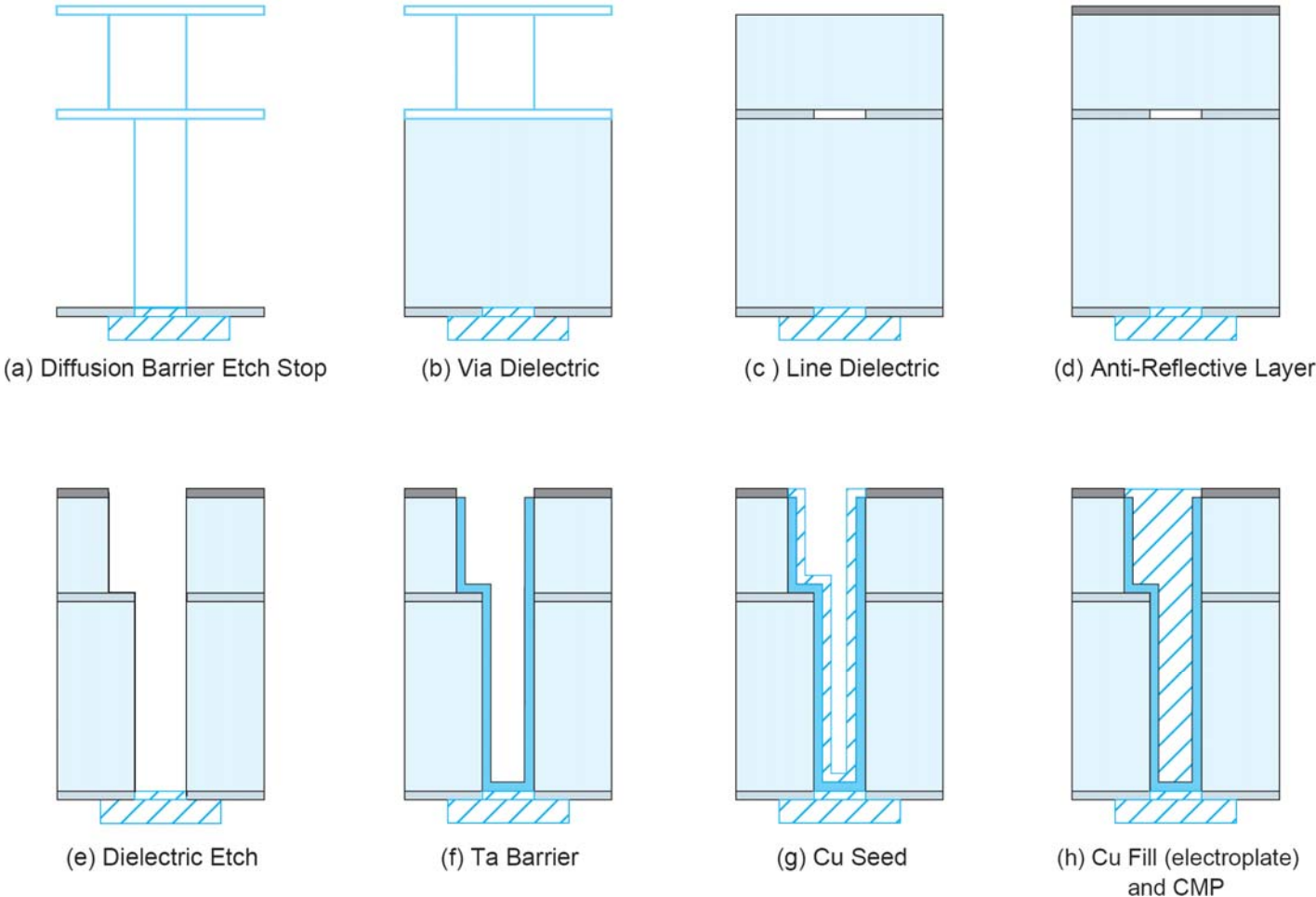
Why Changes?

- ❑ **CMP Oxide**
 - ❖ **Chemical Mechanical Polishing (CMP)**
 - ❖ **Flatten surface to enable multiple levels of metal**
- ❑ **Tungsten (W) contacts and Vias**
 - ❖ **Enable use of CMP**
- ❑ **P+ Substrate**
 - ❖ **Reduce substrate resistance and thus reduce latch-up.**
- ❑ **P- Epi**
 - ❖ **Needed to enable p and n transistor tub doping with P+ Substrate**
- ❑ **Shallow Trench Isolation (STI)**
 - ❖ **Reduce source and drain capacitance**
 - ❖ **Reduce source and drain spacing**
- ❑ **Tungsten-Silicide**
 - ❖ **Reduce gate resistance**

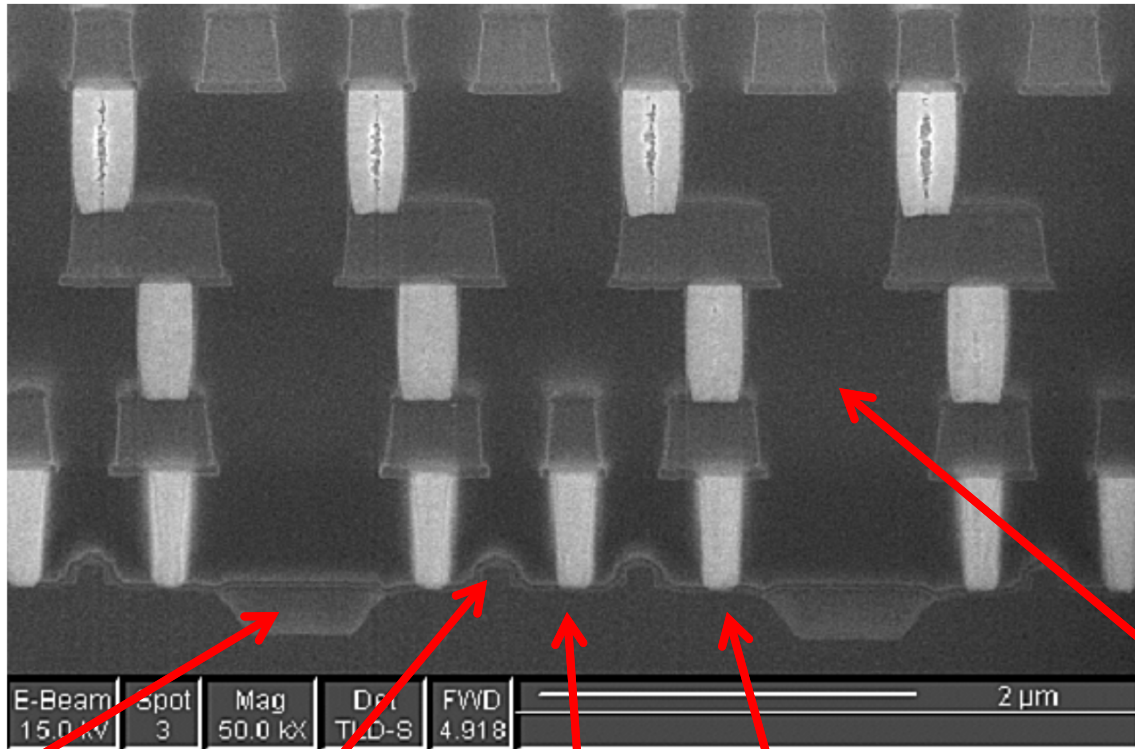
Twin Tub CMOS w/STI & Al-W metal



Dual Damascene Cu Process



TSMC 0.18 CMOS Cross Section



Al Metal 3
W Via 2
Al Metal 2
W Via 1
Al Metal 1
W Contact

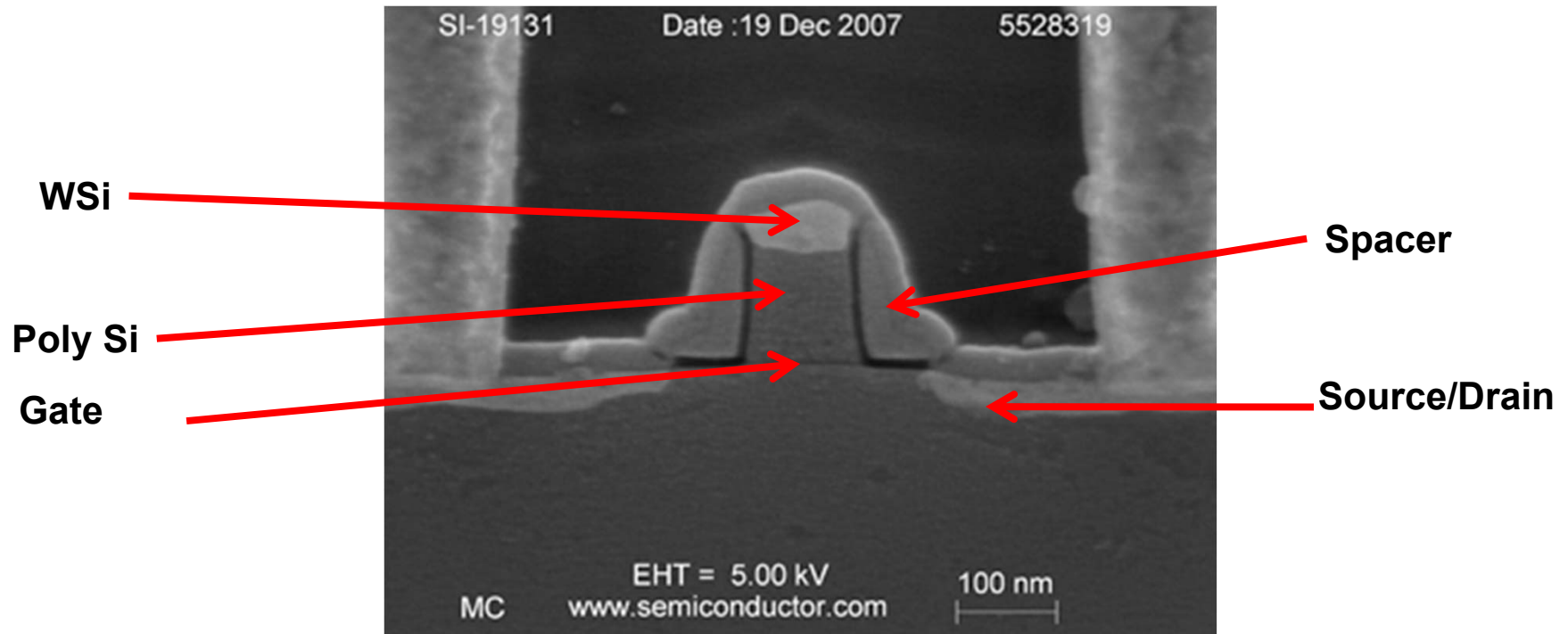
Shallow
Trench
Isolation
(STI)

Poly
Gate

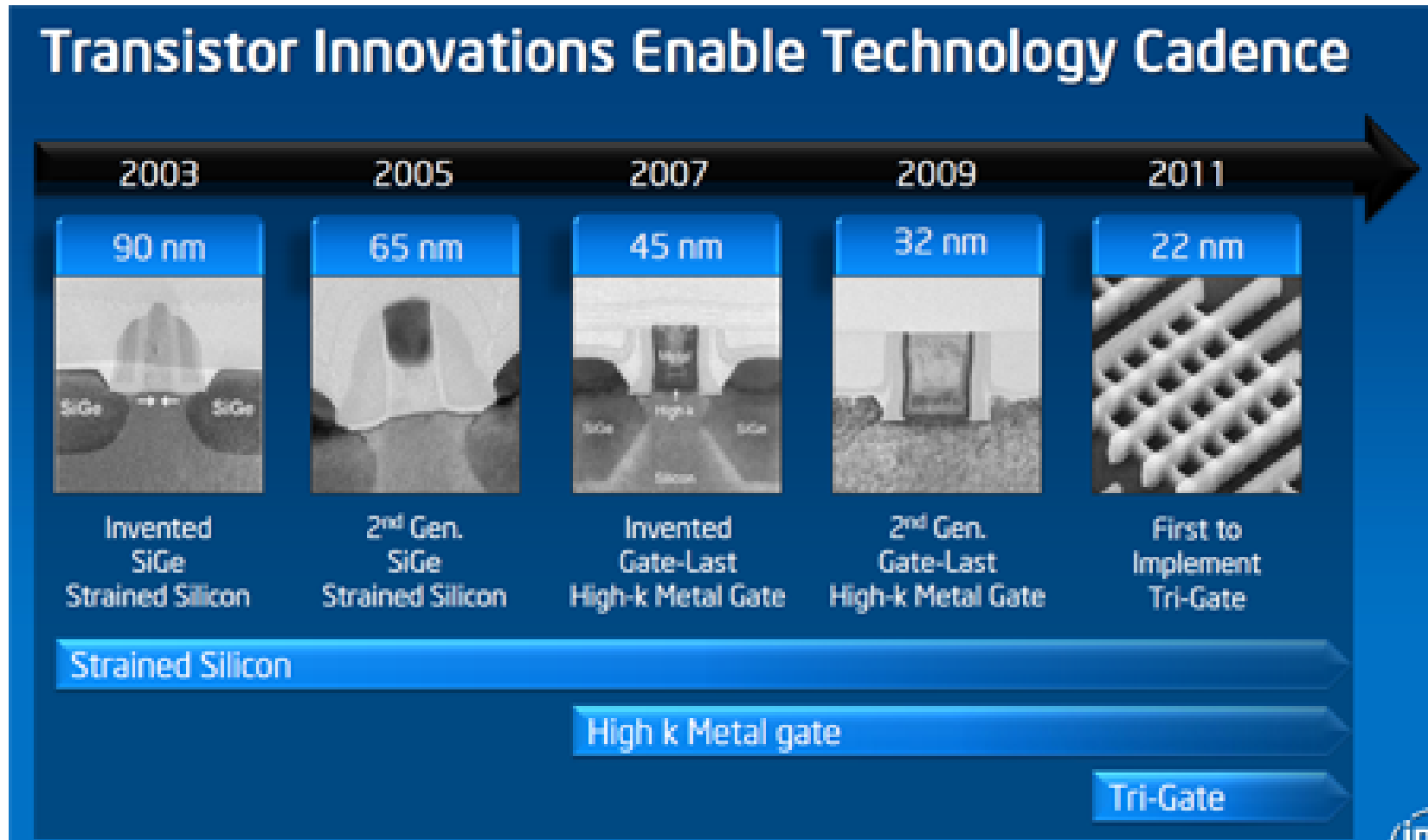
Source
Drain

SiO₂

130 nm transistor

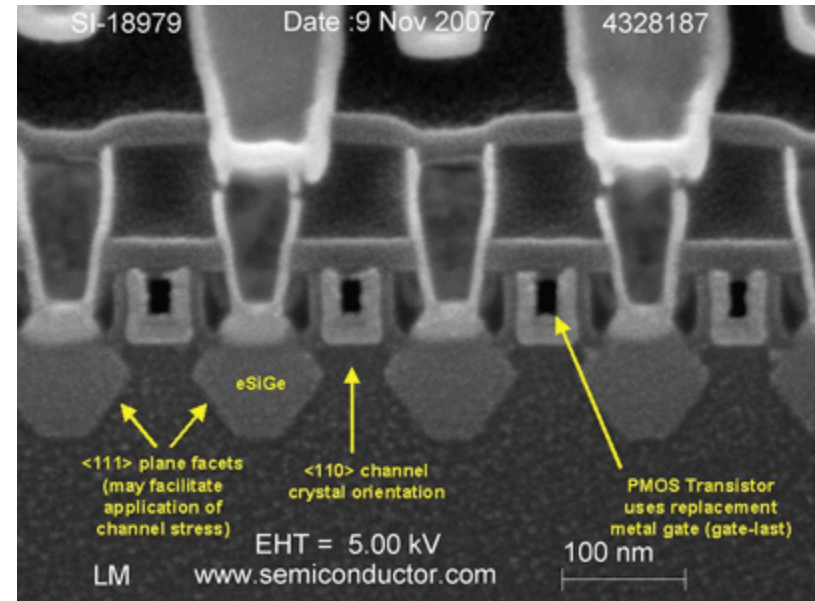
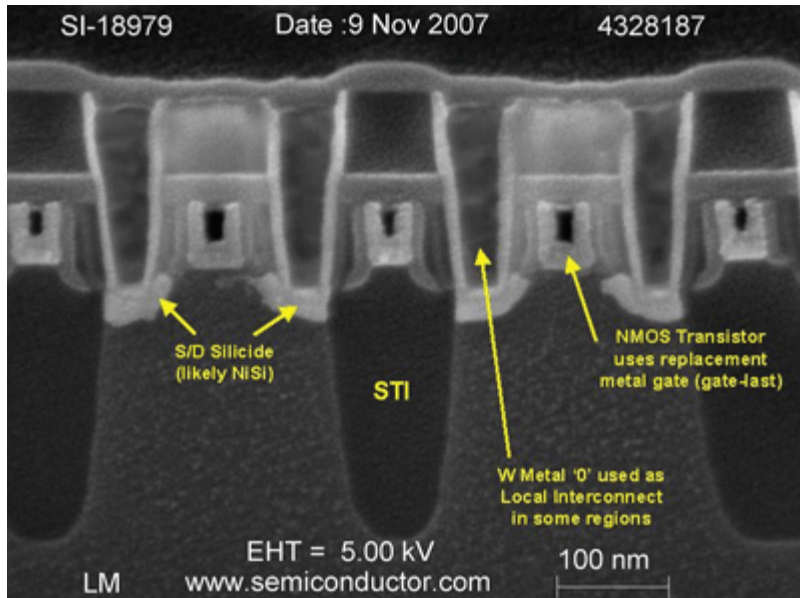


Deep Sub Micron Progress



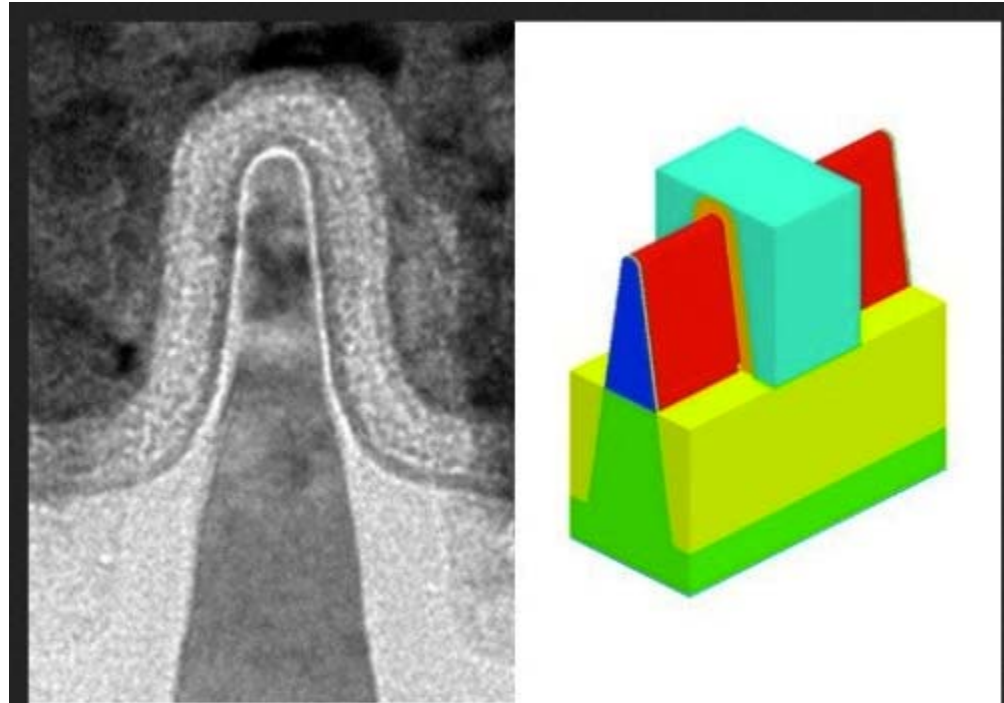
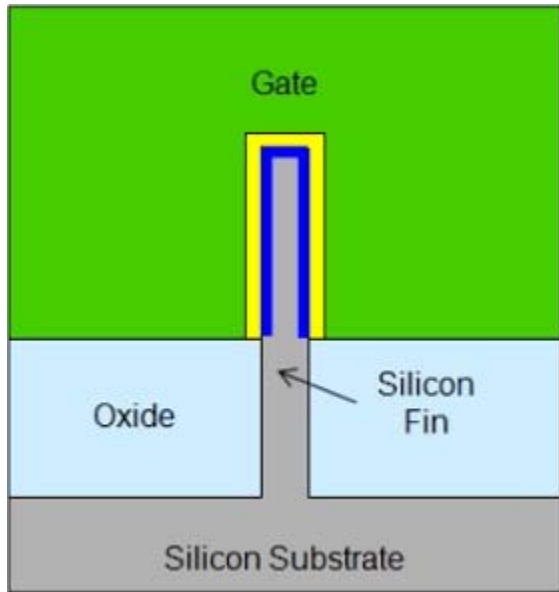
<http://www.zdnet.com/blog/computers/why-intels-22nm-technology-really-matters/5703>

Intel 45 nm Transistor



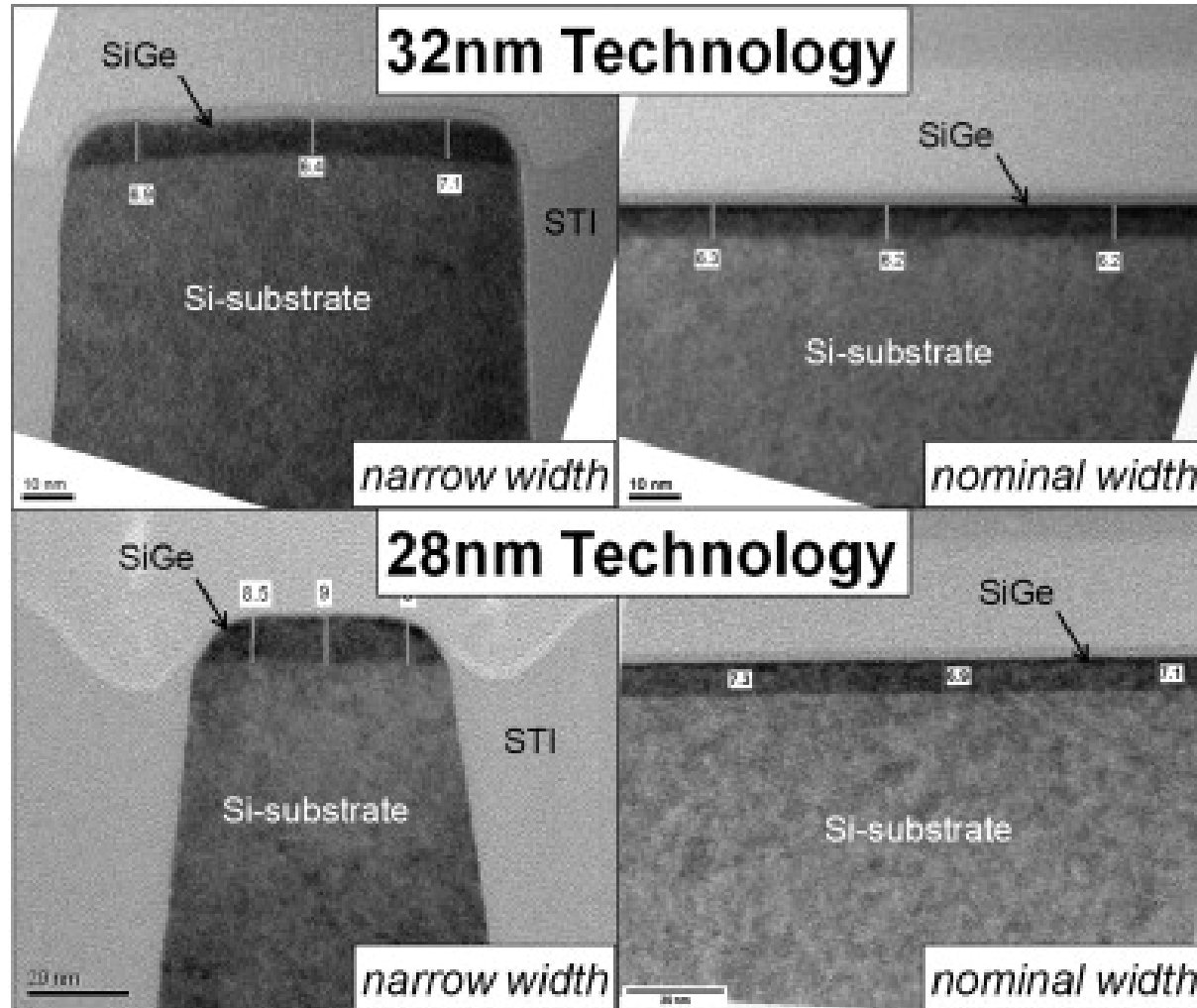
<http://www.eetimes.com/design/automotive-design/4004782/Under-the-Hood-Intel-s-45-nm-high-k-metal-gate-process>

TriGate or FinFET Transistor



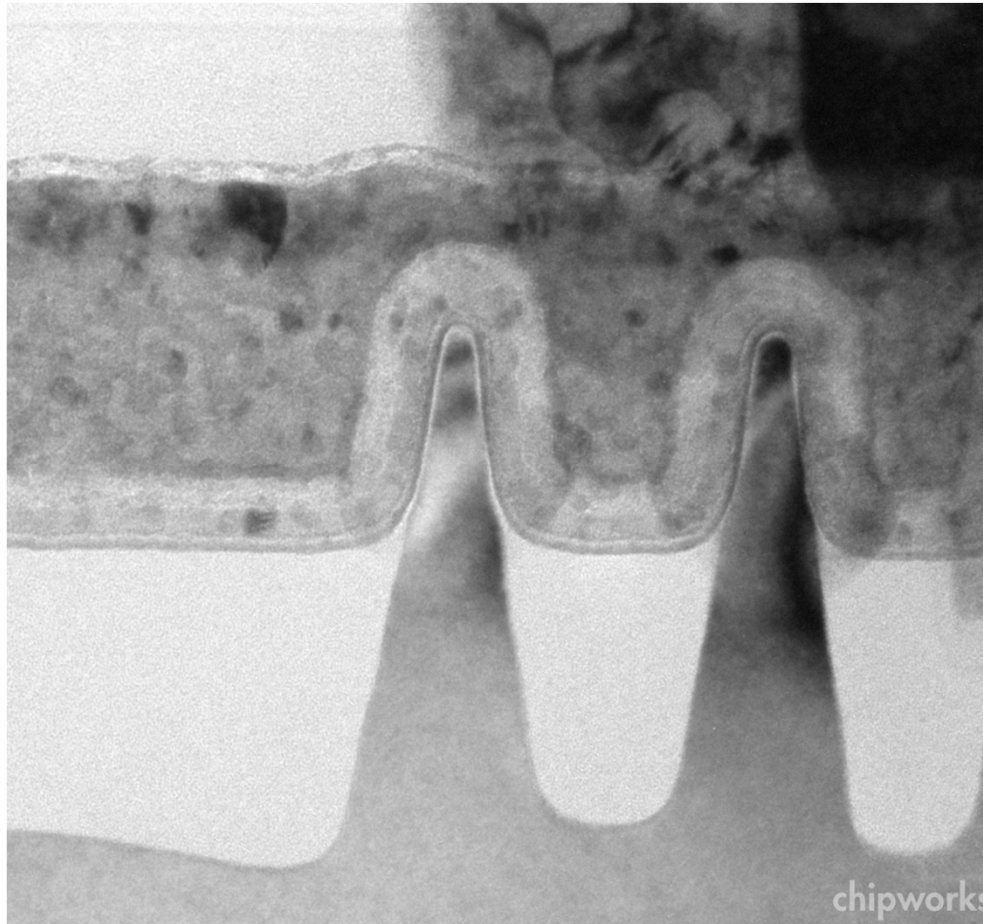
http://www.electronicproducts.com/uploadedImages/Digital_ICs/Microprocessors_Microcontrollers_DSPs/MOUCM_Processing0102_AUG2013.jpg

32 and 28 nm Transistors



<http://www.sciencedirect.com/science/article/pii/S0040609011018335>

Intel 22 nm Tri-gate Transistor

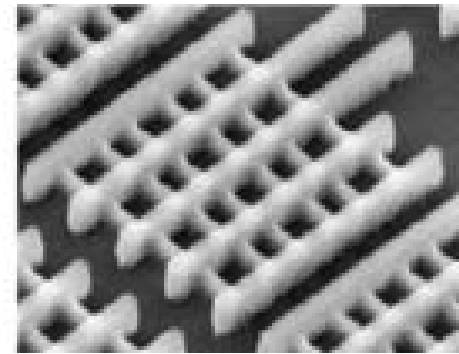
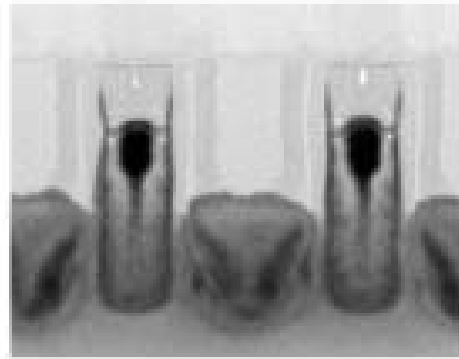
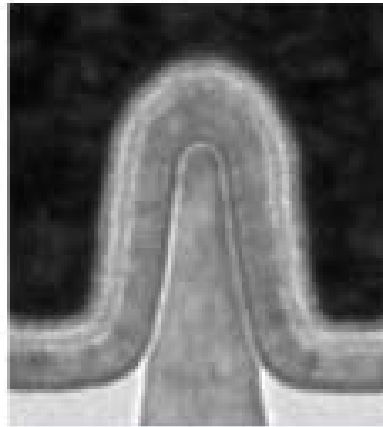


http://www.electroiq.com/blogs/chipworks_real_chips_blog/2012/04/intel-s-22-nm-trigate-transistors-exposed.html

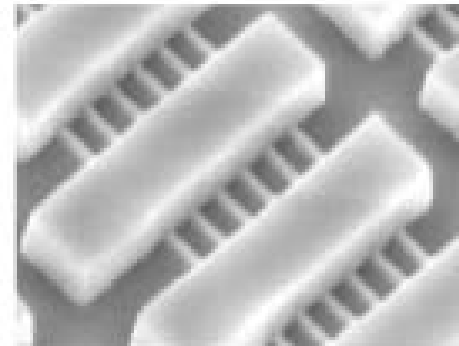
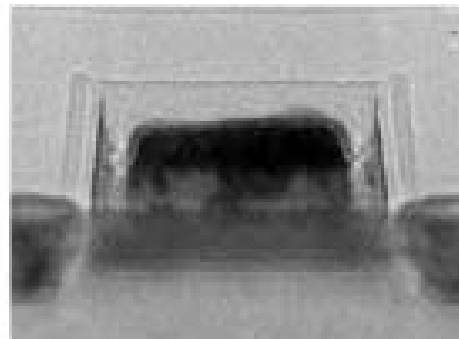
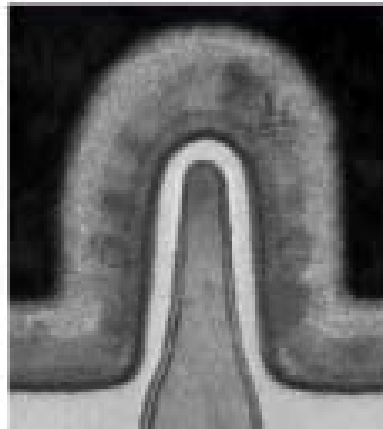
10nm FINFET

Logic

- High Speed (HP/SP)
- Low Power (LP/ULP)

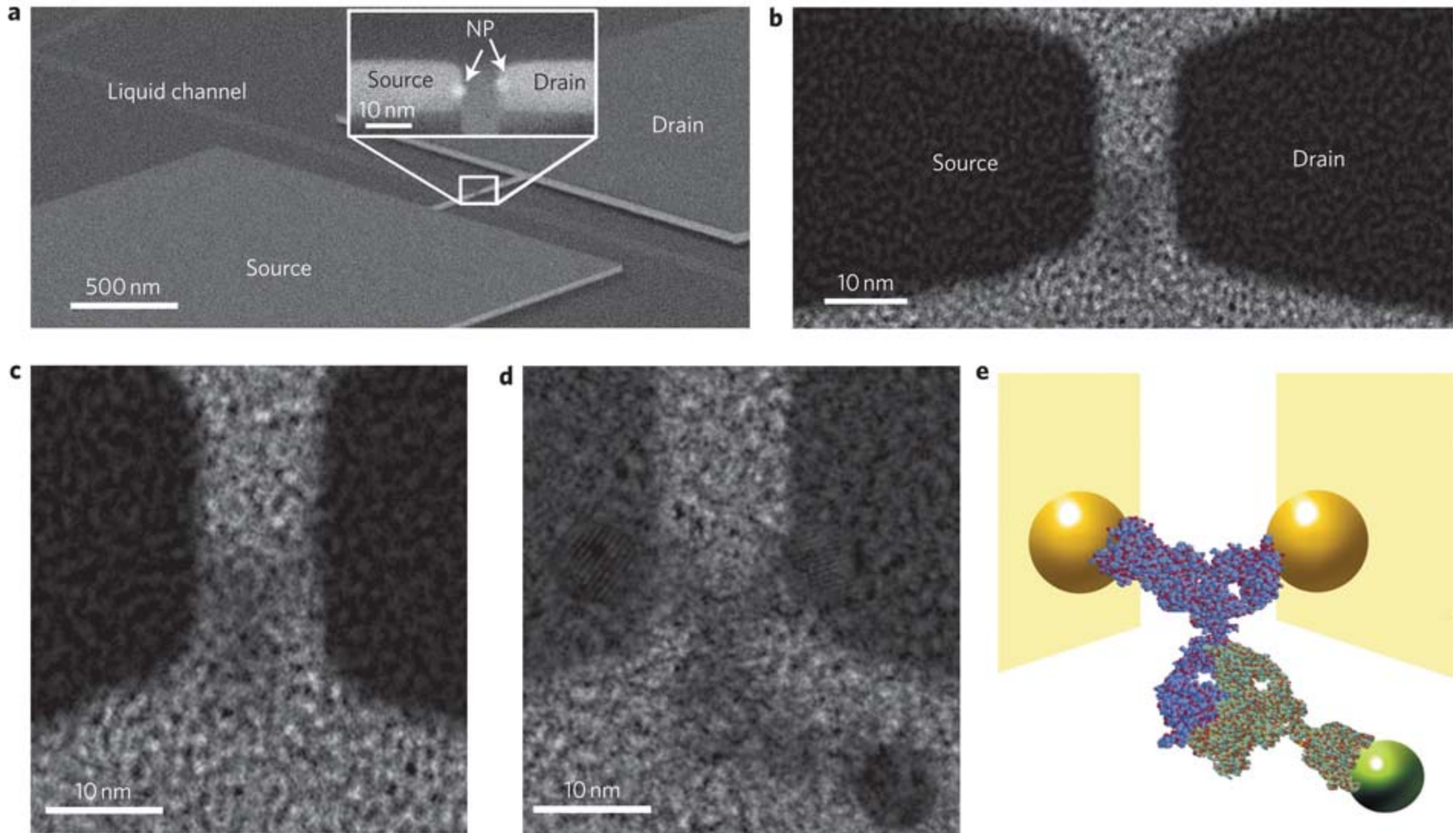


High Voltage



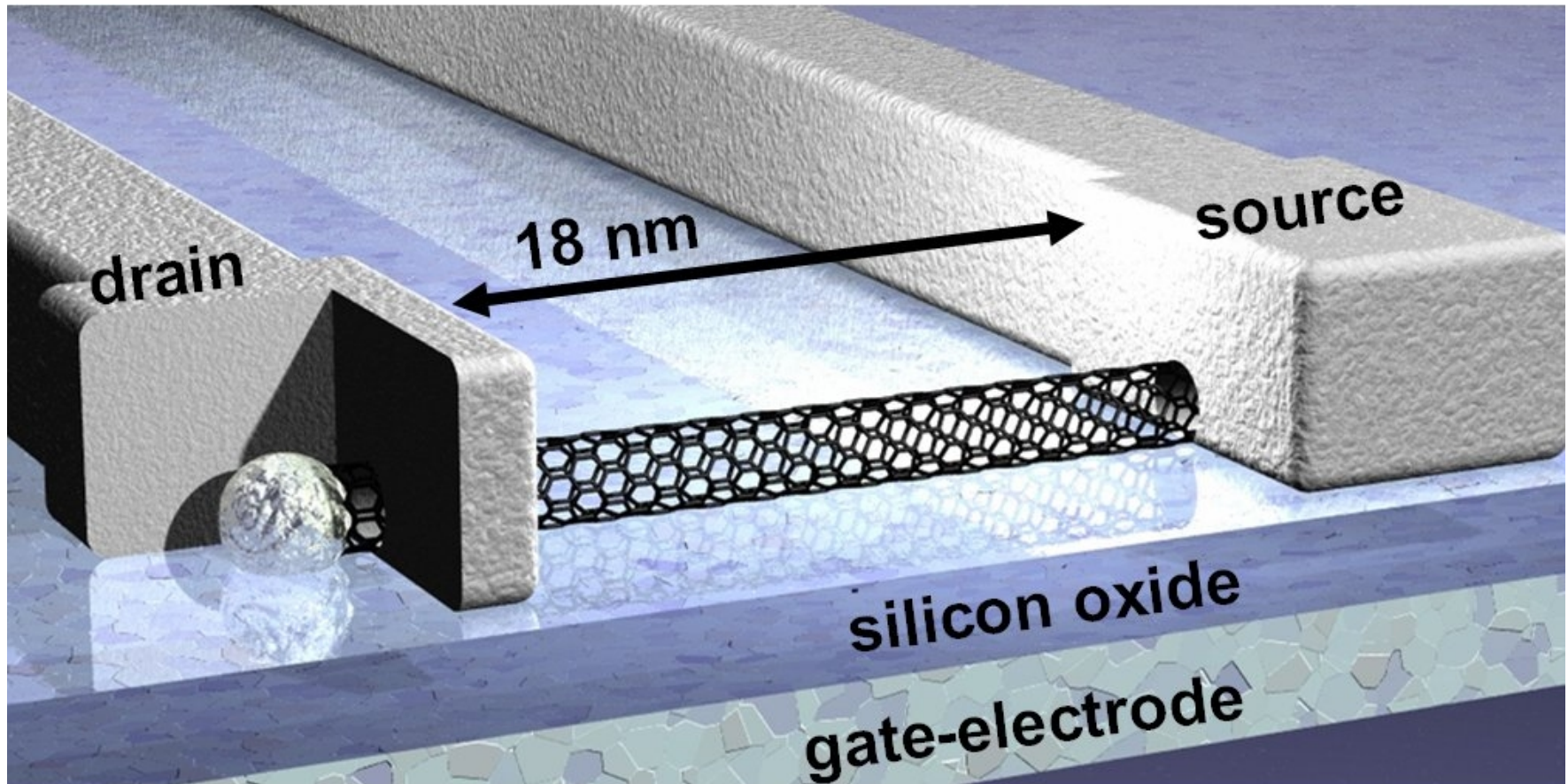
http://www.electronicproducts.com/uploadedImages/Digital_ICs/Microprocessors_Microcontrollers_DSPs/MOUCM_Processing0103_AUG2013.jpg

A 10nm Protein Transistor



http://www.nature.com/nnano/journal/v7/n3/fig_tab/nnano.2012.7_F2.html

Carbon Nanotube Transistor



http://www.infineon.com/export/sites/default/media/press/Image/migration/nanotube_english.jpg