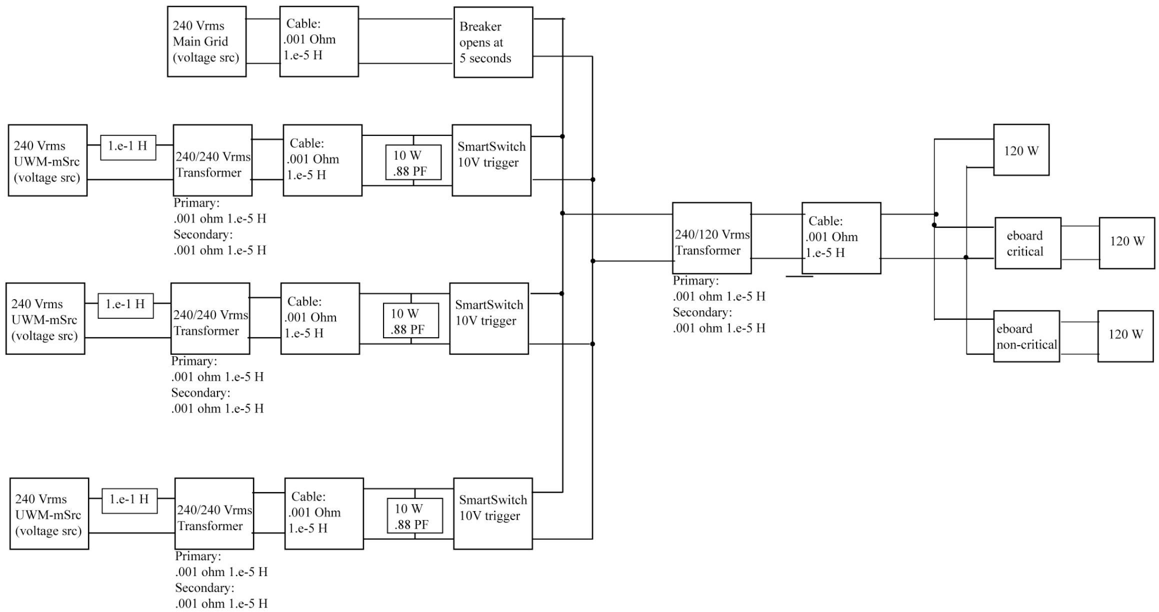
Interim Technical Report:

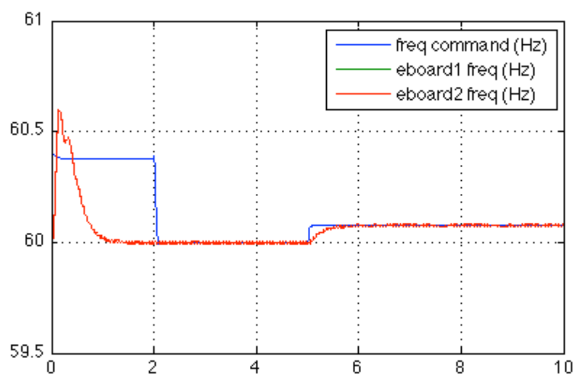
In February we received information from Odyssian concerning the single-phase demonstration that was to be conducted at the company. The main items we became aware of were 1) that the microsources would be 240V/200W sources and 2) that the Odyssian testbed would be single phase. We began developing a single-phase simulation of the testbed, making some modifications that were needed to ensure that the simulation was able to execute. The modified testbed block diagram is shown below. There are certain items present in this diagram that were not present in the original Odyssian block diagram.

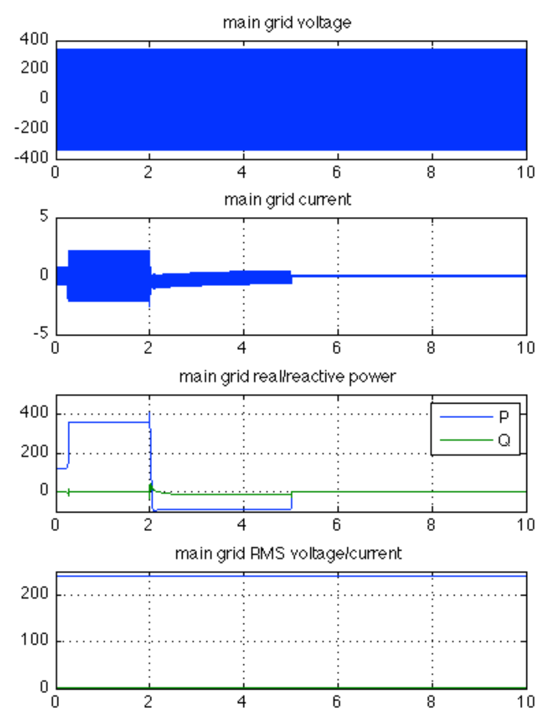
1) We only use 3 (instead of 10 microsources). Simulation times get too long if we use too many sources
2) We assumed that the UWM-controlled sources could be modeled as voltage sources that are interfaced to the grid through a transformer. The actual value of the inductor in series with the transformer had to be chosen relatively large (1.e-1 H) to prevent simulation step size from shrinking below tolerance levels. The secondary of the transformer was connected to a 10 VA load with .88 power factor.
3) Cables were used to model the cables interconnecting the sources and loads. The nominal values were 0.001 Ohm with a 1.e-5 H series inductance.
4) Smart Couplers were used to connect the microsources to the grid. The coupler's were closed once the filtered RMS voltage across the switch was less than 10 V. The filter in this case was a simple analog low pass filter with cutoff frequency at 100 rad/sec.
5) In this simulation the main grid is initially connected with the microsources disconnected. The smartcoupler closes the switch at about 2 seconds. The main grid then disconnects at 5 seconds.
6) The loads were connected through a 240/120 Vrms step down transformer to the sources. There are resistive loads each drawing 120 W. One load is always connected. The other two loads are connected through e-boards that connect at about 0.25 seconds into the simulation. The e-boards also estimate frequency using a phase locked loop (PLL). The PLL is implemented digitally with a 10 msec step size. The low pass filter in the PLL is implemented as a 16 bit fixed point biquad filter.
7) Simulation plots are attached showing that the frequency estimator accurately estimates the commanded frequency from the microsources. The other plots show the time histories of the instantaneous voltage, current, active/reactive power, and RMS voltage current passing out of the main-grid, one of the microsources, and the into all of the loads.

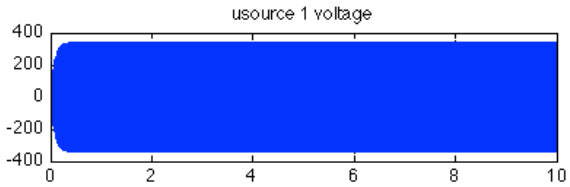
Comments: These plots should provide a more detailed description of the Odyssian single phase testbed, than was presented in the earlier drawing submitted by J. Peterson. From the simulator's standpoint, the selection of transformer and cable Inductances as well as the use of a smart coupler appeared to be rather important. It would be beneficial for UWM to look at this and provide some better guidance concerning the modeling of the microsources and transformers. Later work will simulate a scenario testing the e-board's load shedding logic.

At time = 0, main grid is connected and microsources are disconnected with initial load of 120 W
At t=0.25 seconds the e-board loads are switched on rainsing the total load to 360W
SmartSwitches enable smooth connection of microsources to main grid.
At t=5 seconds, the main grid is disconnected and the system islands.





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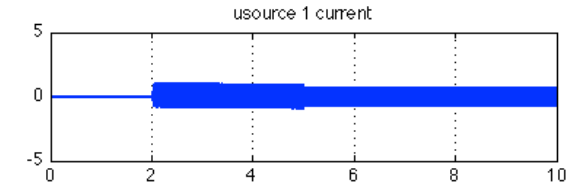
200
0
-200
-400
0
2
4
6
8
10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0
-5
0
2
4
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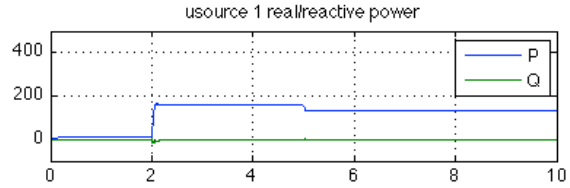
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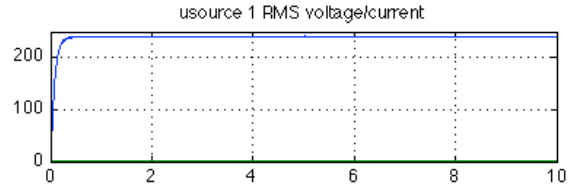
400
200
0
P
Q
0
2
4
6
8
10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200
100
0
0
2
4
6
8
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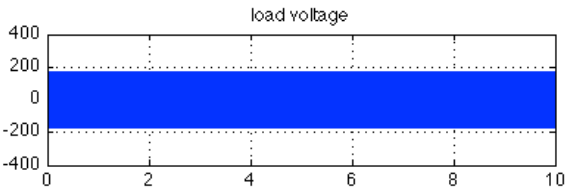
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-200
-400
0
2
4
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8
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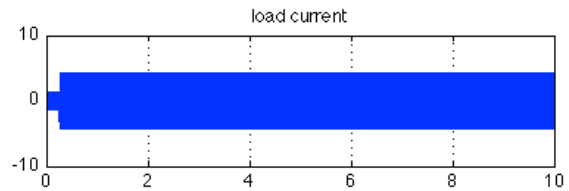
load current
10
0
-10
0
2
4
6
8
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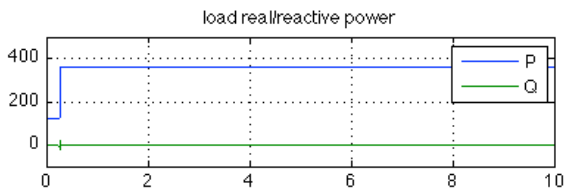
load real/reactive power
400
200
0
P
Q
0
2
4
6
8
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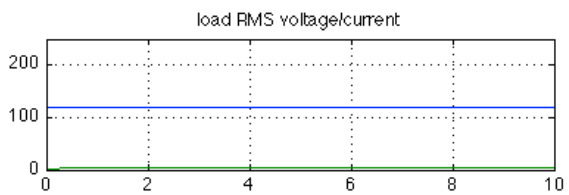
load RMS voltage/current
200
100
0
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2
4
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