Power dissipation in clocked quantum-dot cellular automata circuits

Mo Liu and Craig S. Lent
Department of Electrical Engineering, University of Notre Dame
Email: mliu1@nd.edu

Power dissipation has become an important issue as a result of the increasing densities in microelectronic and nanoelectronic circuits. A new computation paradigm, quantum-dot cellular automata (QCA), has been proposed [1] to offer a possible way to achieve the ultimate in low power dissipation. QCA encodes bit information by charge configuration instead of current switches. No current flows through the cells. The interaction between the cells is purely Coulombic. Adiabatic clocking is applied to obtain power gain and low power dissipation. QCA devices have been demonstrated both theoretically and experimentally [2-4].

Here we report on the dynamic behavior of power dissipation in a clocked QCA majority gate. A distributed clocking scheme is employed in the QCA array to form a "computation wave" which moves smoothly across the circuit. The quantum dynamical calculation is done with coherence vector formalism with dissipation incorporated so that we can see power flowing to the environment, and also to and from the clocking circuit.

Figure 1 shows the layout of a three input majority gate. Figure 2 shows a snap shot of clocked data flow and the energy dissipated in each individual cell when the three input bits are [1 1 1], [1 0 1] and [1 1 0]. The white area indicates the active domain where clocks are high (bits are locked) while the blue area is the null domain where clocks are low. In Figure 2(a), when all inputs are "1", the total energy dissipated in the computation is much less than kTln(2). As long as no information is discarded, computation can be achieved with no fundamental lower bound on the energy dissipated. In Figure 2(b,c) information is lost and the computation necessarily dissipates at least kTln(2). We describe a new clocking scheme for QCA, Bennett-clocking, in which all operations can be performed with no minimum energy dissipation required.

[1] C. S. Lent, P. D. Tougaw, W. Porod and G. H. Bernstein, Nanotechnology 4, 49 (1993).
[2] P. D. Tougaw, C. S. Lent, Journal of Applied Physics, 75 (3): 1818-25 (1994).
[3] A. O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, and G. L. Snider, Science 277, 928 (1997).
[4] I. Amlani, A. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, G. L. Snider, Science 284, 289 (1999).

0-7803-9040-7/05/$20.00 ©2005 IEEE

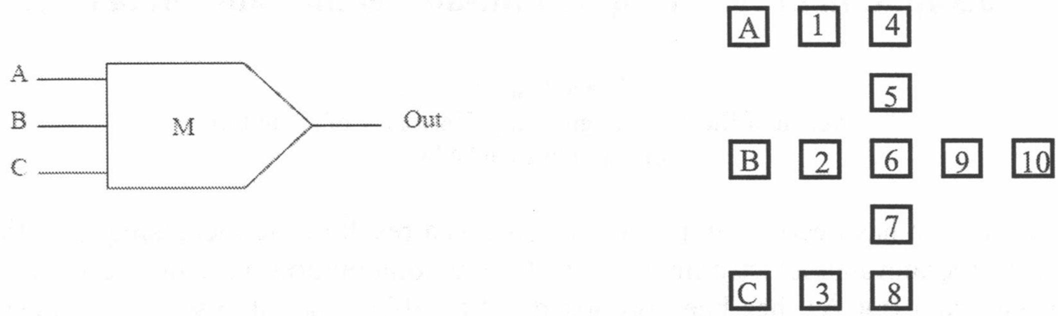

FIG. 1 . Layout of a three input QCA majority gate

(a) ABC: [1 1 1] (b) ABC: [1 0 1] (c) ABC: [1 1 0]

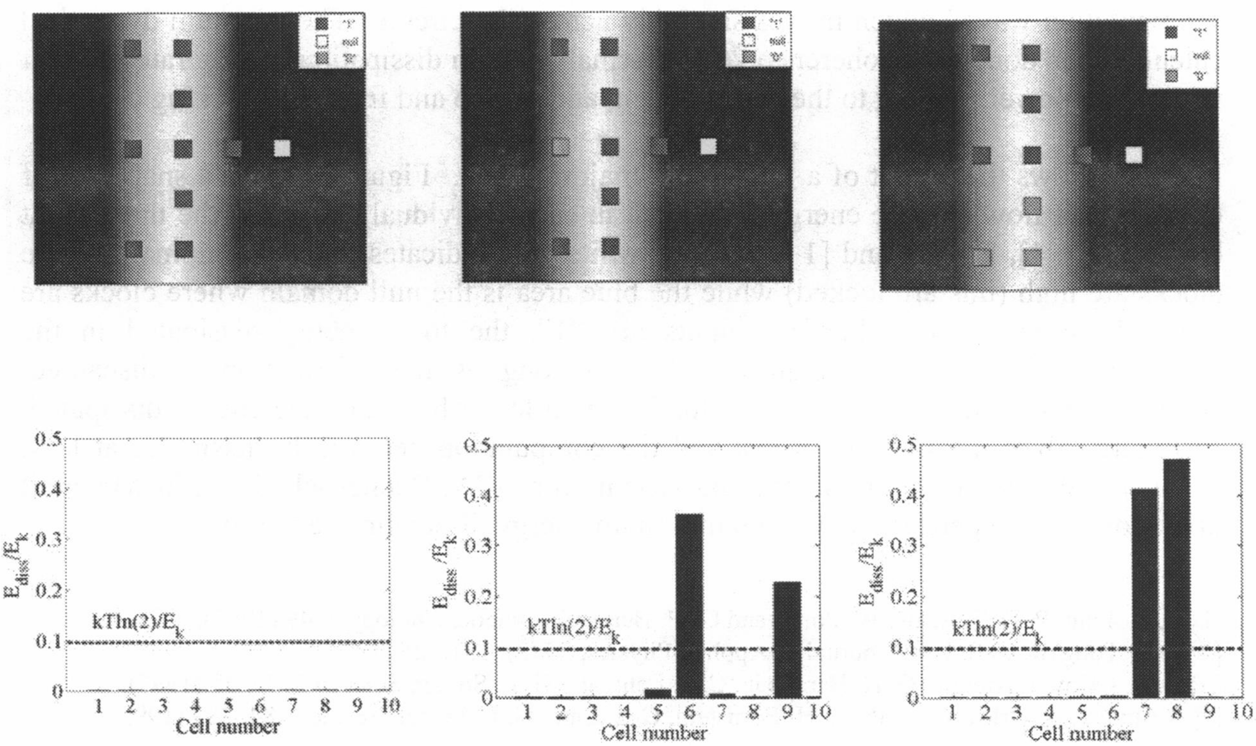

FIG. 2. The snap shot of data flow and energy dissipated in each individual cell when (a) ABC:[111], (b) ABC:[1 0 1], (c) ABC: [1 1 0]. The blue area is the null region, where clock is low. The white area is the active region, where clock is high. The white region forms the computation wave of the circuit. The red bar represents "1". The blue bar indicates "0". The white bar is the null state.