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Reliability and Defect Tolerance in Metallic Quantum-dot Cellular Automata

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Abstract. The computational paradigm known as quantum-dot cellular automata (QCA) encodes binary information in the charge configuration of Coulomb-coupled quantum-dot cells. Functioning QCA devices made of metal-dot cells have been fabricated and measured. We focus here on the issue of robustness in the presence of disorder and thermal fluctuations. We examine the performance of a semi-infinite QCA shift register as a function of both clock period and temperature. The existence of power gain in QCA cells acts to restore signal levels even in situations where high speed operation and high temperature operation threaten signal stability. Random variations in capacitance values can also be tolerated.

Keywords: QCA, molecular electronics, single electronics, quantum-dot cellular automata, nanoelectronics

1. Introduction

Conventional transistor-based CMOS technology faces great challenges with the down-scaling of device sizes in recent years. Issues such as quantum effects, dopant-induced disorder, and power dissipation may hinder further progress in scaling microelectronics. As the scaling approaches a molecular level, a new paradigm beyond using current switches to encode binary information may be needed. Quantum-dot cellular automata (QCA) [1–3, 6, 12, 13, 18, 21] emerges as one such a paradigm. In the QCA approach bit information is encoded in the charge configuration within a cell. Columbic interaction between cells is sufficient to accomplish the computation; no current flows out of the cell. It has been shown that very low power dissipation is possible [8].

A clocked QCA cell constructed with six quantum dots is shown in Fig. 1. Dots are simply places where a charge is localized. Two mobile electrons are present in the cell. The electrons will occupy antipodal sites in the corner dots because of Coulomb repulsion. The two configuration states correspond to binary information of "1" and "0." The electrons can also be pulled to middle dots if the occupancy energy in the middle dots is lower than corner dots. In this case we term the configuration "null," with no binary information present. The clock adjusts the relative occupancy energy between active dots in the corner and null dots in the middle, pushing electrons to either active dots or null dots. The cell therefore switches between null state and active state. When a cell is placed close to another cell (as shown in Fig. 1b), they will have the same polarization due to Coulomb coupling. Based on the cell-to-cell interaction, logical QCA devices like binary wires, inverters, majority gates and full adders can all be implemented [18].

QCA devices exist. QCA devices made of metal-dot cells have been successfully demonstrated at low temperatures. Majority gates, binary wires, memories, clocked shift registers and fan outs have all been fabricated [1–3, 12, 13, 21]. Figure 2 shows a schematic diagram and scanning electron micrograph of a clocked shift register. Aluminum islands form the dots and Al/AlO_x tunnel junctions serve as the tunneling path between dots. Tunnel junctions are fabricated with shadow evaporation technique. Multiple tunnel junctions are used instead of a single junction to suppress co-tunneling. The clock is implemented by simply applying voltage to leads capacitively coupled to the middle dots. Single electron transistors (SET's) are used as readout electrometers.

Though the operation of metal-dot QCA devices is restricted to cryogenic temperatures, they may be viewed as prototypes for molecular QCA cells that will operate at room temperature. It may well be that molecular QCA,

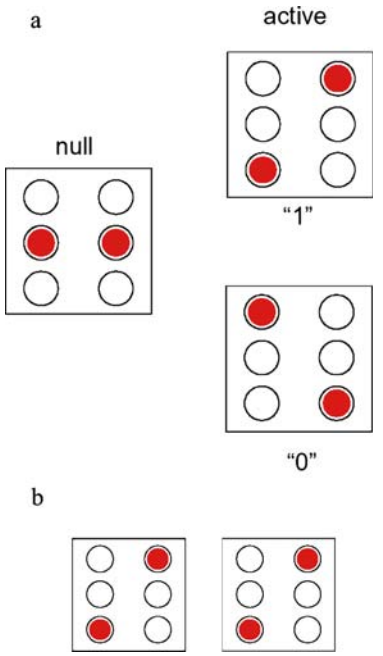


Fig. 1. Schematic of a QCA cell. **a** The *three states* of a single cell. **b** Coulomb interactions couple the states of neighboring cells.

with the possibility of enormous functional densities, very low power dissipation, and room temperature operation, is finally the most promising system [5, 9–11, 14, 16]. Metal-dot QCA do have the advantage of having been already created and tested, and we expect that understanding the details of robustness in the metal-dot system will yield benefits for designing molecular systems.

Here we focus on the robustness in metal-dot QCA circuits. In particular, we consider theoretically the effects of temperature, random variations in capacitance, and operating speed, on the performance of a semi-infinite QCA shift register. The paper is organized as follows: in Section II, we describe the application of single-electron tunneling theory to metal QCA devices. Section III describes the characterization of power gain in QCA circuits. In Section IV we analyze the operation of a semi-infinite QCA shift register. Finally, in Section V we calculate behavior of the QCA shift register in the limits of high speed, high temperature, and high defect levels.

2. Single Electron System Theory

Metal-dot QCA can be described with the orthodox theory of coulomb blockade [19]. The circuit is defined by charge configurations, which are determined by the number of electrons on each of the metal islands. Metal islands are regions of metal surrounded by insulators; at zero temperature they hold an integer number of charges. The islands play the role of QCA dots and are coupled to other islands and leads through tunnel junctions (i.e., quantum-mechanically leaky capacitors) and non-leaky capacitors. Leads by contrast are metal electrodes whose voltages are fixed by external sources. We define dot charge q_i as the charge on island i and q_k' as the charge on lead k. The free energy of charge configuration within the circuit is the electrostatic energy stored in the capacitors and tunnel junctions minus the work done by the voltage sources [20]:

$$F = \frac{1}{2}\begin{bmatrix} q \\ q' \end{bmatrix}^T C^{-1} \begin{bmatrix} q \\ q' \end{bmatrix} - v^T q' \qquad (1)$$

Here $\mathbf{C}$ is the capacitance matrix including all the junctions and capacitors, $\boldsymbol{v}$ is the column vector of lead voltages, and $\boldsymbol{q}$ and $\boldsymbol{q}'$ are the column vectors of dot charges and lead charges. At zero temperature, the equilibrium charge configuration is the one that has minimum free energy and the number of charges on each islands is exactly an integer. A tunneling event happens at zero temperature only if the free energy is lower for the

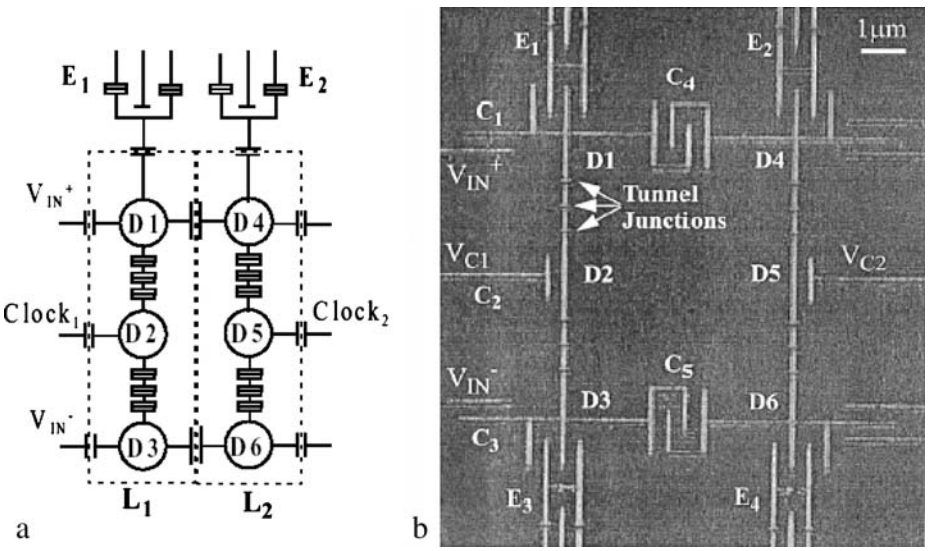


Fig. 2. **a** Schematic of a clocked shift register. **b** Scanning electron micrograph of a clocked shift register.

final state than for the initial state. At finite temperatures, a dot charge need no longer be an integer but is rather a thermal average over all possible configurations. A thermally excited tunneling event may happen even when the free energy increases. The transition rate of tunneling between two charge configuration states at a certain temperature T is given by

$$\Gamma_{ij} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - e^{-\Delta F_{ij}/(kT)}} \tag{2}$$

where R_T is the tunneling resistance, ΔF_{ij} is the energy difference between the initial state i and final state j.

The tunneling events can be described by a master equation—a conservation law for the temporal change of the probability distribution function of a physical quantity,

$$\frac{d\boldsymbol{P}}{dt} = \Gamma \boldsymbol{P} \tag{3}$$

where $\boldsymbol{P}$ is the vector of state probabilities and Γ is the transition matrix. From the solution $\boldsymbol{P}(t)$ we can obtain the ensemble average of the charge on each dot. We solve Eq. 3 directly and find the dot charge as a function of time; from this we can obtain any other voltage or charge in the circuit. In many systems direct solution of the master equation, which requires the enumeration of all the accessible states of the system is impractical due to the large set of accessible states. Because QCA operates so near the instantaneous ground state of the system, complete enumeration of the accessible states is possible and we need not resort to Monte Carlo methods.

3. Power Gain in QCA

A robust circuit must have power gain in order to restore signals weakened due to unavoidable dissipative processes. In conventional CMOS, the power supply provides the energy power gain. In QCA systems the energy needed for power gain is supplied by the clock. A weak input is augmented by work done by the clock to restore logic levels. Power gain has been studied theoretically in molecular QCA circuits [8] and measured experimentally in metal-dot QCA circuits [3]. Power gain is defined by the ratio of the work done *by* the cell on its neighbor to the right (the output of the cell), to the work done *on* the cell by its neighbor to the left (the input to the cell). The work done on a cell by an input lead coupled through an input capacitor C over a time interval T is given by

$$W = \int_0^T V(t) \frac{d}{dt} Q_c(t) dt \tag{4}$$

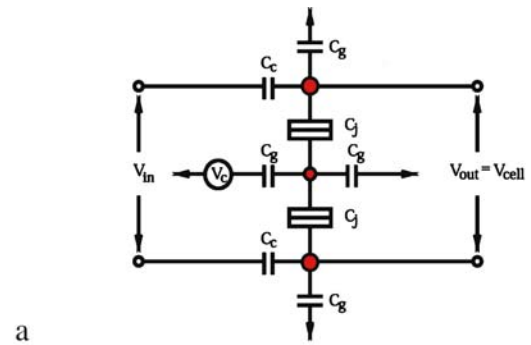
where $V(t)$ is the lead voltage, $Q_c(t)$ is the charge on the input capacitor. We consider the total work done over a clock period so the cell configuration is the same at t=0 and t=T. The power gain is thus the ratio of output to input signal power W_{out}/W_{in}, where each sums the work done by (on) all input (output) leads.

4. Operation of Semi-infinite QCA Shift Register

The schematic of a clocked half QCA cell is shown in Fig. 3a. The capacitances are taken to be C_j=1.6 aF, C_g=0.32 aF, C_c=0.8 aF, and the tunneling resistance R_T=100 kΩ. Each island is grounded through a capacitance of 0.32 aF. These are physically reasonable though somewhat better (meaning capacitances are smaller) than the experiments have so-far achieved. Input is applied to the top and bottom dot through coupling capacitors. The potential difference between the top and bottom dots is the output V_{cell}.

The phase diagram of the equilibrium charge state configuration of the cell shown in Fig. 3a is plotted in Fig. 4. The diagram shows the calculated stable regions of charge configuration as a function of input and clock potential. Each hexagonal region is labeled by three integers (n_1, n_2, n_3), the number of elementary charges in the top, middle, and bottom dot, respectively. A positive number indicates an extra hole and negative number represents an extra electron. Each hexagon represents the configuration state that has, for those values of input voltage and clock voltage, the lowest free energy.

The clocking cycle can be envisioned as follows. First, a small input bias is applied, when the clock is high (less



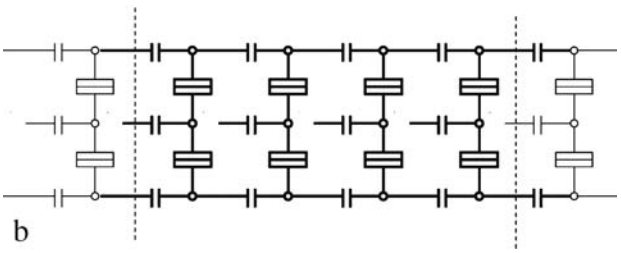


Fig. 3. **a** Schematic of a clocked *triple dot*. The input is applied to the *top* and *bottom dot*. The clock is set to the *middle dot*. The output defined as V_{cell} is the differential potential between the *top* and the *bottom dot*. C_j=1.6 aF, C_g=0.32 aF, C_c=0.8 aF. The capacitor to ground is 0.32 aF. R_T=100 kΩ. **b** Schematic of a shift register composed of a *line of identical triple dots* in **a**. The *thick line* described the actual four cells simulated.

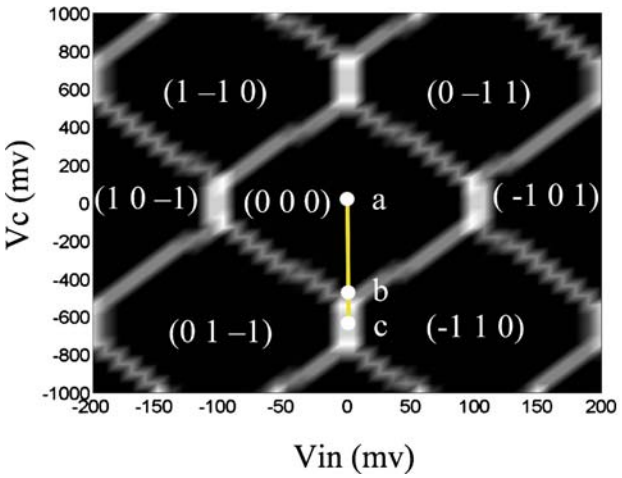


Fig. 4. The equilibrium state configuration of a *triple dot* cell described in Fig. 6. (n1, n2, n3) are the number of charges in the *top*, *middle* and *bottom dot*, respectively. The cell is in the null state in *point a*. The cell is in the active state in *point b*. The cell is in locked state in *point c*.

negative, in fact for this circuit 0). This situation corresponds to point a in Fig. 4; no electron switching event happens and the cell remains in the null state, holding no information. When the clock is then lowered (more negative) the system moves along the line shown through point b. An electron is switched to either top dot or bottom dot, decided by the input; the cell is then in the active state. If the clock is held very negative (point c), the electron is locked in the active state, since the energy barrier in the middle dot is too high to overcome. The locked cell is essentially a single bit memory—its present state depends on its state in the recent past, not on the state of neighbors. Varying clock potential gradually between point a and c will switch the cell between null, active and locked state adiabatically.

A QCA shift register can be constructed with a line of capacitively coupled half QCA cells shown in Fig. 3b, where the output from each cell acts as the input to its right neighbor. The transport of information from cell to cell is controlled by clock signals. Initially, all the cells are in the null state since the clocks are high. Then an input signal is applied to the first cell and the clock for the first cell is lowered. The first cell thus switches to the opposite state of the input and holds to that state even when input is removed. When the clock for the second cell is lowered, the second cell switches to the opposite state to the first cell accordingly and locks the bit. The information is thereafter propagated along the cell line by the clock signals. Each cell in turn copies (an inverts) a bit from its neighbor to the left when the left neighbor is in the locked state and erases the bit, i.e., returns to the null state, while its right neighbor still holds a copy (inverted) of the bit. The copying of the bit can be accomplished gradually so that the switching cell is always close to its instantaneously ground state and thus dissipates very little energy.

It's instructive to model a semi-infinite shift register in order to study the robustness in the QCA circuit. A four phase clocking scheme is adopted to achieve adiabatic switching, shown in Fig. 5. Each clock signal is shifted a quarter-period. As a bit moves down the shift register, we need model only a four QCA half-cells at a time, since by the time the bit is latched in the leading cell, the leftmost cell has returned to null. This is equivalent to viewing the simulation as occurring on a ring of four half-cells. Figure 6 shows the time evolution of cell potentials for four neighboring cells in a semi-infinite shift register. The shaded areas indicate stored bit information. Each cell has the opposite signal to its neighboring cells with a quarter period shift; the information is both copied and inverted. The arrow indicates the direction of the information flow. At the end of the first quarter clock period, the first clock is set to low so that the first cell latches the input and locks it while the second cell is in the null state. By the time the second clock is low, the first cell is still kept locked. The second cell thus copies the bit from the first cell. By the end of the third quarter period, the bit in the first cell is erased as its clock is set to high. The third cell copies the bit from the second cell and holds it. The process goes on and the bit information is transported along the chain. Note that there are always at least two copies of the bit at one time. When there are three copies of the bit, the cell potential in the middle cell decreases slightly (in absolute value) while the cell potential in its left and right neighbor increase slightly (thus the small "notch" in the center of the flat parts of the waveform).

5. Robustness in Semi-infinite QCA Shift Register

5.1. *Effect of Temperature and Speed*

Because of the difficulty of fabricating small capacitors, metal-dot QCA circuits operate at low temperatures. Thermal excitation is therefore a potential source of

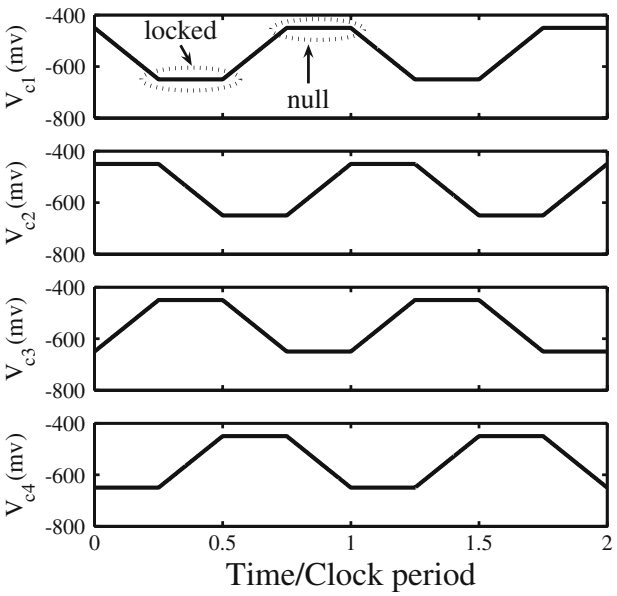


Fig. 5. A four phase clocking scheme in *metal-dot* QCA.

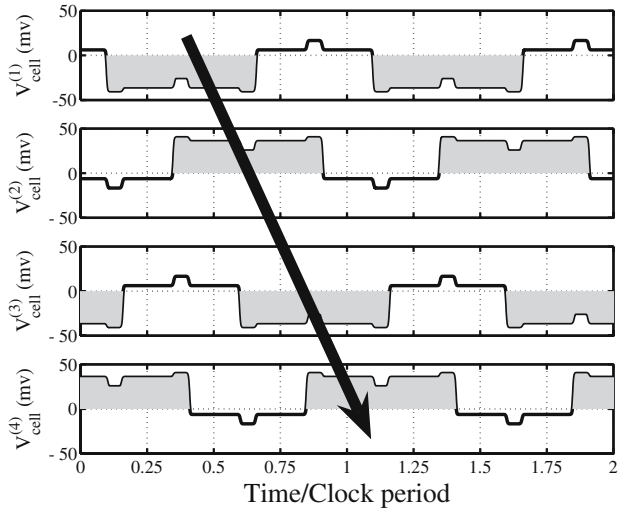


Fig. 6. Time evolution of cell potential in the neighboring cells. $V_{cell}^{(n)}$ is the differential potential between the *top* and the *bottom dot* of the *n*th cell.

random error in metal-dot QCA circuits, and it is clear that at high enough temperatures the circuit will fail. It is tempting to conclude that for a long line of cells, failures are unavoidable at any non-zero temperature. It is well known that there is no long-range order in one-dimensional systems [15]. While the energy for a mistake might be higher than k_BT, the degeneracy (and therefore entropy) of mistake states increases as the system size expands. For a system in thermal equilibrium therefore, the free energy of the mistake states eventually become lower than the mistake-free zero-entropy ground state [7]. A static (unclocked) chain of QCA cells therefore has, for any non-zero temperature, a characteristic length ($\sim e^{E_k/k_BT}$) after which mistakes become very likely. But a clocked line is not in thermal equilibrium—it is actively driven. The clock can supply energy to the system to restore signal states.

To see the effect of temperature on the performance of the clocked semi-infinite shift register, we here solve the time-dependent problem of the clocked shift register using the master-equation (Eq. 3) approach described in Section II. The calculated cell potential (see Fig. 3) of the kth cell in the chain at time t is $V_{cell}(k,t)$. When each cell in the chain in turn latches the bit the cell potential is at its largest magnitude. Figure 7 shows this maximum cell potential $V_{cell}(k)=\max(|V_{cell}(k,t)|)$ as a function of cell number k down the chain. The calculated response is plotted for various values of the temperature. The cell potential is higher at the very beginning of the chain simply because the first cell is driven by an input voltage which is a stronger driver than subsequent cells see; they are driven by other cells. At temperatures above 10 K the cell potential decays with distance as information is transported along the chain. At each stage the signal deteriorates further, and for a long shift register the

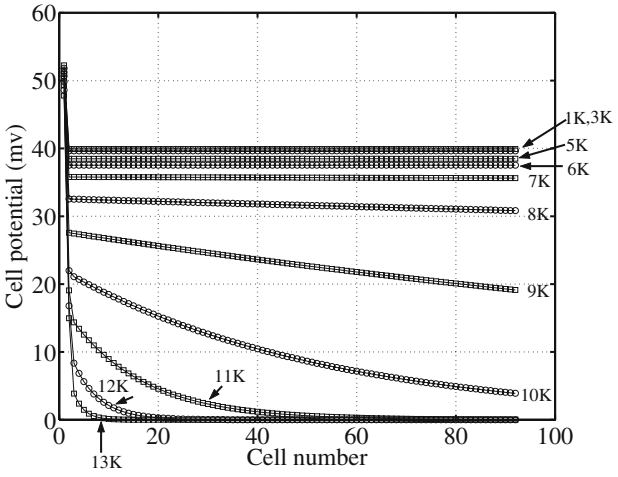


Fig. 7. Cell potential as a function of cell number at different temperatures.

information will be lost. For individual cells, this means errors due to thermal fluctuations become increasingly more likely. As the temperature is lowered the signal decay-length increases. At temperatures below 5 K, however, the behavior appears qualitatively different—the cell potential remains constant along the long the chain. To the accuracy of our calculation for a large but finite number of cells, no signal degradation appears at all.

The degradation of performance with increasing temperature can be explained in terms of power gain. We calculate the power gain of each individual cell in the chain by directly calculating the work done on the cell by its neighbor to the left, and the work done by the cell on its neighbor to the right. For each operating temperature the power gain is the same for each cell (apart from those very near the beginning of the line). If the power gain is precisely 1 (or greater), then there is no signal degradation moving down the line. At each cell, power is drawn from the clock sufficient to completely restore the signal as it is copied to the next cell. We refer to the situation in

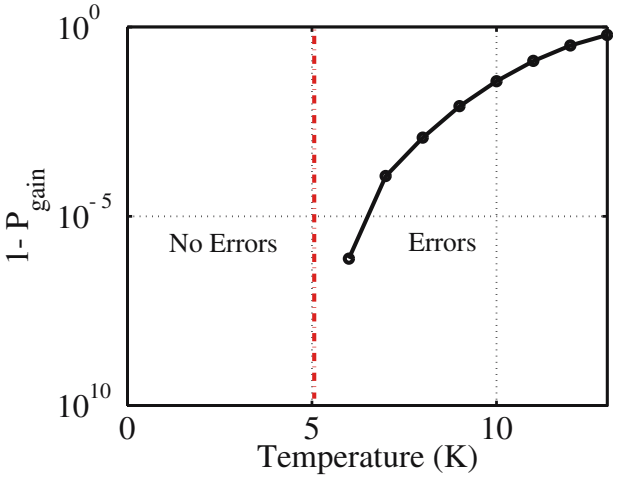


Fig. 8. Deviation from unity power gain for an individual cell as a function of temperature.

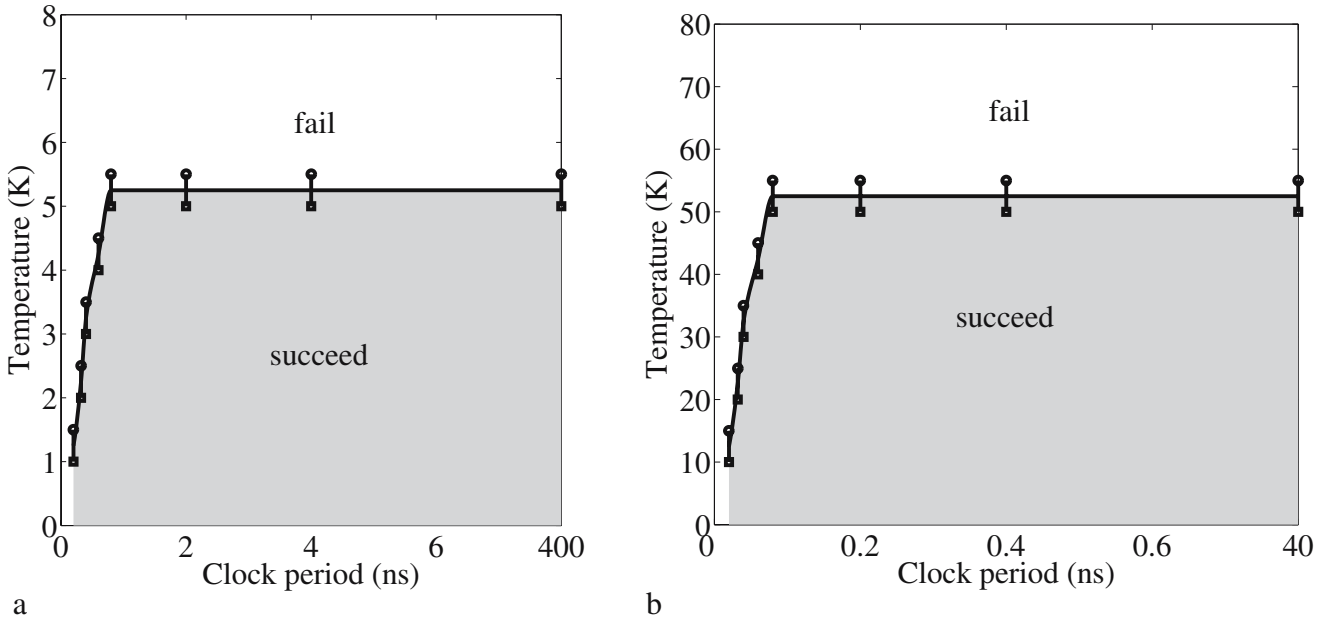


Fig. 9. The phase diagram of the operation space as a function of temperature and clock period when **a**. *C*j=1.6 aF, and **b**. *C*j=0.16 aF. The *shaded area below the curve* is where the circuit succeeds and the *white area* is where the circuit fails.

which unity power gain enables transmission of signals over arbitrarily long distances as "robust" operation. If the power gain is less than 1, then the signal will be degraded as it moves down the line. Figure 8 shows the deviation from unity power gain as a function of temperature on a logarithmic scale. For temperatures below 5 K the power gain is 1; above 5 K, the power gain is less than 1. At higher temperatures, the flow of energy from the clock can no longer compensate for the energy loss to the thermal environment, with the result that the signal decays at each stage. As the difference between the power gain and 1 becomes small our analysis is limited by the numerical accuracy of the calculation. Nevertheless, the exponential character of the approach to unity power gain supports the interpretation that this transition is a qualitative change between robust and non-robust behavior, analogous to a phase transition.

The time-dependent calculation above is repeated for various temperatures and clock speeds to generate the phase diagram of the operational space of the circuit shown in Fig. 9. We display the results for the circuit with our standard parameters, with C_j=1.6 aF in Fig. 9a and for more aggressively scaled parameters, with C_j=0.16 aF in Fig. 9b. All capacitances and voltages in the circuit are scaled appropriately with C_j. The aggressively scaled parameter calculation illustrates scalability of QCA circuits. The performance of the circuit will increase with smaller capacitances. The shaded area below the curve indicates speeds and temperatures for which the circuit is robust. The white area represents non-robust operation for

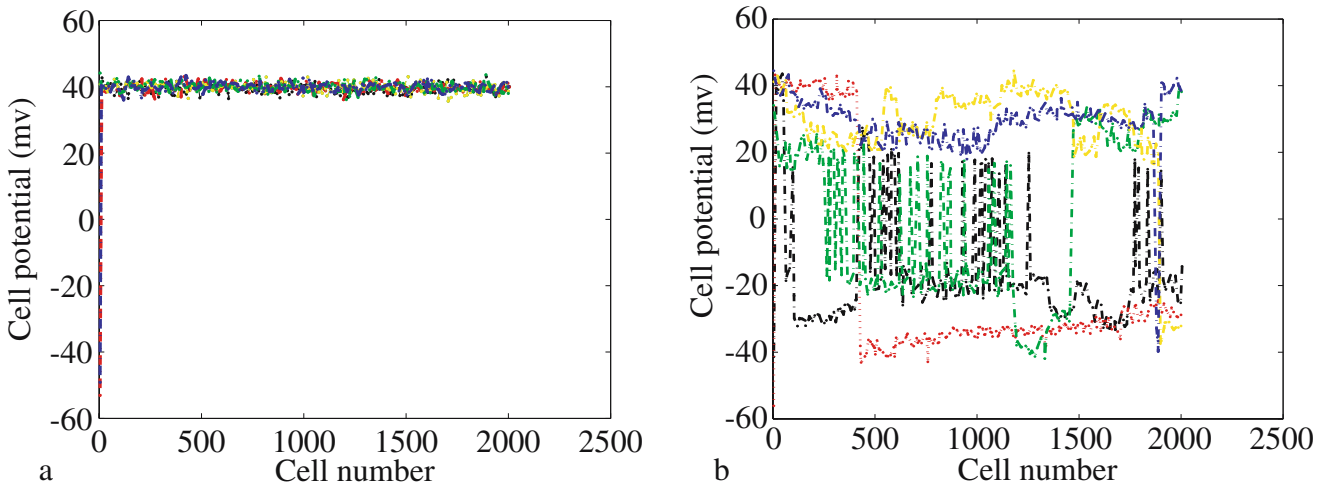


Fig. 10. Cell potential as a function of cell number at 4 K when capacitance variation is **a** ±10% **b** ±15%.

which bit information decays along the chain. The two figures are identical except for the scale: the aggressively scaled circuit of Fig. 9b operates ten times faster and at a temperature ten times higher than the circuit in Fig. 9a.

The area of robust operation is limited by both speed and temperature. In Fig. 9a, when the clock period is less than about 0.2 ns (corresponding to 5 GHz), the circuit fails (is not robust) even at zero temperature. This occurs as the clock period approaches the electron tunneling rate. When the clock speed is too fast, the electrons do not have enough time to tunnel reliably from one dot to another. The error probability accumulates as the information moves along the chain. Increasing the clock period increases the probability of electrons being in the "right" states. This improvement quickly saturates and further increasing the clock period has no effect since the electrons have had enough time to be in the correct state. The tunneling rate is related to the tunnel resistance, so this description is equivalent to the observation that the speed is limited to the RC time-constant of the circuit.

5.2. Defect Tolerance in the QCA Shift Register

A robust circuit must be tolerant of defects that introduce variations in the values of the designed parameters. We consider the situation of a very long shift register in which the value of each capacitor in the circuit is varied randomly within a fixed percentage range from its its nominal value. The circuit is robust if the perturbation of the capacitances does not influence the performance of the circuit. We choose a working point in Fig. 9a where clock period is 5 ns, the temperature is 4 K, and vary all the capacitances randomly by ±10 and ±15%. Figure 10 shows the cell potential as a function of cell number with random capacitance variation. Different color represents different capacitance variation within the certain percentage range. When the deviation is ±10%, the circuit is robust and transmits bit information with no errors. The bit information is carried on correctly even at the 2,000th cell. When the deviation increases to ±15%, the circuit is fragile since cells are flipped to the wrong states during propagation. This calculation demonstrates, again as a result of the power gain in each cell, that QCA circuits can tolerate considerable variation in parameter values and still function correctly.

6. Conclusion

The QCA approach represents an entirely new way of encoding, moving, and processing binary information. As more experimental realizations of devices appear, attention naturally turns to the broader circuit behavior of these new devices. While molecular QCA may represent the most realistic long-term system for robust room temperature operation, the metal-dot QCA system provides an extremely valuable prototype system in which to explore QCA properties. Metal dot systems also have the advantage of being realizable now.

We have explored here the behavior of metal-dot QCA systems under stress—stressed by high temperature operation, high speed operation, and random variation in parameter values. In each case enough stress destroys the correct operation of the circuit. What we observe however is that these systems are not terribly fragile, they can survive in a broad range of operational space. In each case small errors threaten to accumulate over many cells and result in signal loss. The key feature is power gain from the clocking circuit which provides considerable robustness against these error mechanisms, restoring signal levels at each stage.

References

1. I. Amlani, A. Orlov, G. Toth, G.H. Bernstein, C.S. Lent, and G.L. Snider, *Science*, vol. 284, p. 289, 1999.
2. R.K. Kummamuru, J. Timler, G. Toth, C.S. Lent, R. Ramasubramaniam, A. O. Orlov, G.H. Bernstein, and G.L. Snider, *Appl. Phys. Lett*., vol. 81, pp. 1332–1334, 2002.
3. R.K. Kummamuru, A.O. Orlov, C.S. Lent, G.H. Bernstein, and G.L. Snider, *IEEE Trans. Electron Devices*, vol. 50, pp. 1906–1913, 2003.
4. R.K. Kummamuru, M. Liu, A.O. Orlov, C.S. Lent, G.H. Bernstein, and G.L. Snider, *Microelectron. J*., vol. 36, 2005.
5. C.S. Lent and B. Isaksen, *IEEE Trans. Electron Devices*, vol. 50, pp. 1890–1896, 2003.
6. C.S. Lent, P.D. Tougaw, W. Porod, and G.H. Bernstein, *Nanotechnology*, vol. 4, p. 49, 1993.
7. C.S. Lent, P.D. Tougaw, and W. Porod, *PhysComp'94, The Proceedings of the Workshop on Physics and Computing*, pp. 5–13, Dallas, TX: IEEE Computer Society Press, Nov. 17–20 1994.
8. C.S. Lent, B. Isaksen, and M. Lieberman, *J. Am. Chem. Soc*., vol. 125, pp. 1056–1063, 2003.
9. Z. Li and T.P. Fehlner, *Inorg. Chem*., vol. 42, pp. 5715–5721, 2003.
10. Z. Li, A.M. Beatty, and T.P. Fehlner, *Inorg. Chem*., vol. 42, pp. 5715–5721, 2003.
11. M. Lieberman, S. Chellamma, B. Varughese, Y.L. Wang, C.S. Lent, G.H. Bernstein, G.L. Snider, and F.C. Peiris, *Ann. N.Y. Acad. Sci*., vol. 960, pp. 225–239, 2002.
12. A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent, and G.L. Snider, *Science*, vol. 277, p. 928, 1997.
13. A.O. Orlov, I. Amlani, R.K. Kummamuru, R. Ramasurbramaniam, G. Toth, C.S. Lent, G.H. Bernstein, and G.L. Snider, *Appl. Phys. Lett*., vol. 77, pp. 295–297, 2000.
14. H. Qi, S. Sharma, Z. Li, G.L. Snider, A.O. Orlov, C.S. Lent, and T.P. Fehlner, *J. Am. Chem. Soc*., vol. 125, pp. 15250–15259, 2003.
15. D.J. Thouless, *Phys. Rev*., vol. 187, pp. 732–733, 1969.
16. J. Timler and C.S. Lent, *J. Appl. Phys*., vol. 91, pp. 823–832, 2002.
17. G. Toth and C.S. Lent, *J. Appl. Phys*., vol. 85, pp. 2977–2984, 1999.
18. P.D. Tougaw and C.S. Lent, *J. Appl. Phys*., vol. 75, no. 3, pp. 1818–1825, 1994.
19. C. Wasshuber, *Computational single-electronics*, Berlin Heidelberg New York: Springer, 2001.
20. C. Wasshuber, H. Kosina, and S. Selberherr, *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst*., vol. 16, p. 9, 1997.
21. K.K. Yadavalli, A.O. Orlov, R.K. Kummamuru, C.S. Lent, G.H. Bernstein, and G.L. Snider, "Fanout in Quantum-dot Cellular Automata," *63rd Device Research Conference*, Santa Barbara, CA, 2005.

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