Challenges and Innovations in Nano-CMOS Transistor Scaling

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Nikkei Presentation
Outline

• **Traditional-Scaling**
  - Traditional Scaling Limiters, Device Implications
  - Intel’s Response

• **Post “Traditional-Scaling” Innovations**
  - Mobility Booster: Uniaxial Strain
  - Poly Depletion Elimination: Metal Gate
  - Gate Leakage Reduction: HiK

• **Future Challenges and Options**
  - Power Limitation
  - Potential New Transistor Structures and Materials
40+ Years of Moore’s Law at INTEL: From Few to Billions of Transistors

Transistor Count has Doubled Every Two Years
40+ Years of Moore’s Law at INTEL: From Few to Billions of Transistors

END OF TRADITIONAL SCALING ERA ~ 2003
Lasted ~40 YEARS
Top “Traditional-Scaling” Enablers

• **Gate Oxide Thickness Scaling**
  - Key enabler for Lgate scaling

• **Junction Scaling**
  - Another enabler for Lgate scaling
  - Improved abruptness ($R_{EXT}$ reduction)

• **Vcc Scaling**
  - Reduce $X_{DEP}$ (improve SCE)
  - However, did not follow const E field

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1990’s: Golden Era of Scaling
Vcc, Tox & Lg scaling & increasing $I_{dsat}$

R. Dennard et.al.
IEEE JSSC, 1974
Year 2000: INTEL 90nm CMOS Pathfinding
End of “Traditional-Scaling” Era

- Gate Oxide Running out of atoms
  - Gate Oxide Leakage direct tunneling limited

- Mobility degrades with scaling
  - Universal Mobility Model
  - Ionized impurity scattering

T. Ghani et. al. VLSI Symposium 2000
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Innovations Pioneered by Intel to Overcome “Traditional-Scaling” Limiters

• Mobility enhancement through uniaxial strained silicon technology innovation introduced at 90nm node
  - Epitaxial SiGe S/D
  - SiN Capping Layers

• HiK gate insulator introduced at 45nm CMOS node to reduce gate leakage

• Metal Gate introduced at 45nm CMOS node to eliminate poly depletion
Uniaxial Strain Silicon Transistors
Intel: IEDM 2003

These transistor structures introduced first at Intel’s 90nm CMOS node. These structures have now become industry standard for strain implementation.
Strained SiGe S/D PMOS Transistor

• SiGe film **embedded** into source/drain
• SiGe film deposited by selective epitaxy
• Induces large **uniaxial** compressive strain in channel
• This strain leads to dramatic hole mobility enhancement
How Strain Impacts Mobility?

Strain impacts mobility through:

- Energy/subband spacing which affects scattering ($\tau$)
- Valley repopulation which changes transport mass ($m_{\text{eff}}$)
- Band warpage which changes transport mass ($m_{\text{eff}}$)

\[
\mu = \frac{q < \tau >}{m_{\text{eff}}}
\]

M. Stettler, 2006 SINANO Device Modeling School
Performance Gains with Uniaxial Strain

2nd Gen PMOS: 65nm
Ref: Unstrained Silicon

2.2x Mobility

Idsat

Drive Gain (%)

Source: Intel
(100)/<110>
Channel=Si

E_{EFF}=1MV/cm

Significant headroom left to increase PMOS mobility in future (> 5x)
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Year 2003: INTEL 65nm CMOS Pathfinding
Gate Oxide Runs out of steam

Intel 65nm production: 2005
• Gate Oxide only 3-4 atomic layers thick.
• Gate depletion also a limiter

• Gate Oxide Leakage
direct tunneling limited

T. Ghani .et. al. VLSI Symp. 2000
High-k + Metal Gate Benefits

• High-k gate dielectric
  – Reduced gate leakage
  – $T_{OX}(e)$ scaling

• Metal gates
  – Eliminate polysilicon depletion
  – Resolves $V_T$ pinning and poor mobility for high-k dielectrics
High-k + Metal Gate Challenges

- **High-k gate dielectric**
  - Poor mobility
  - Poor reliability

- **Metal gates**
  - Dual band edge work functions
  - Thermal stability
  - Integration scheme
Transistor Process Flow

• **Key considerations**
  – Integrate hafnium-based high-k dielectric, dual metal gate electrodes, strained silicon
  – Thermal stability of metal gate electrodes

• **High-k First, Metal Gate Last**
  – Metal gate deposition after high temperature anneals
  – Integrated with strained silicon process
Hafnium-based high-k + metal gate transistors are the biggest advancement in transistor technology since the late 1960s.
45 nm High-k + Metal Gate Transistors

Benefits compared to 65nm node

>25x lower gate oxide leakage

>30% lower switching power

~30% higher drive current, or

>5x lower source-drain leakage

*Intel is only company with high-k + metal gate transistors in production, starting in Nov. ‘07*
Scaling of Vt Variation

\[ \sigma_{V_{\text{Tran}}} = \left( \frac{4q^2 \epsilon_r \phi_B}{2} \right) \frac{T_{\text{ox}}}{\epsilon_{\text{ox}}} \times \left( \frac{4\sqrt{N}}{\sqrt{\text{Leff} \cdot \text{Zeff}}} \right) = \frac{1}{\sqrt{2}} \left( \frac{c_2}{\sqrt{\text{Leff} \cdot \text{Zeff}}} \right) \]  

HK+MG reduces random Vt variation  
Critical to SRAM Vmin
Replacement Metal Gate Flow

Standard transistor process through source-drain formation, but including atomic layer deposition high-k dielectric
Replacement Metal Gate Flow

Deposit and planarize oxide layer
Replacement Metal Gate Flow

Etch out sacrificial polysilicon gate
Deposit separate NMOS and PMOS WF metal layers
Replacement Metal Gate Flow

Deposit Al fill metal, planarize surface
RMG PMOS Strain Benefit

RMG process provides significant additional PMOS performance gain by increasing channel strain
45 nm Microprocessor Products

- Single Core
- Dual Core
- Quad Core
- 6 Core
- 8 Core

>200 million 45 nm CPUs shipped to date
<table>
<thead>
<tr>
<th>Process Name</th>
<th>Products</th>
<th>1st Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>45 nm</td>
<td>CPU</td>
<td>2007</td>
</tr>
<tr>
<td>32 nm</td>
<td>CPU</td>
<td>2009</td>
</tr>
<tr>
<td>22 nm</td>
<td>CPU</td>
<td>2011</td>
</tr>
</tbody>
</table>

**Intel 32nm**: 2nd generation high-k + metal gate transistors
Transistor Density

Intel 32 nm transistors provide the tightest gate pitch of any reported 32 nm or 28 nm technology
Intel 32 nm transistors provide the highest drive currents of any reported 32 nm or 28 nm technology.
SRAM Cell Size Scaling

Transistor density continues to double every 2 years.
Intel’s 32 nm process is certified and CPU wafers are moving through the factory in support of planned Q4 revenue production.
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CPU Transistor Count & Power Trend

Power Dissipation Limited to ~100W
BUT increased transistor count needed in Multi-Core CPU Era !!!
Multi-Core CPU Power Limited Era

\[ P = \text{Switching Power} + \text{Leakage Power} + \ldots \]

\[ \sim (fC_{gate} V_{CC}^2 \alpha) \times N \]

\[ V_{CC} \text{ scaling required for continued increase in transistor count in power limited world} \]

**Future Transistors will need to continue to achieve Higher Performance while Scaling Power Supply Voltage**
Possible Future Transistor Options

- Advanced Channel Materials
  - III-V and Ge channel materials

- Multi-Gate Fin Transistors
  - Non planar architecture

- Tunnel Transistors
  - New transport mechanism

Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET.
Ultimate Channel Materials: Ballistic Transport

Ultimate Ballistic Regime:
\[ I_{\text{DSAT}} \sim Q_{\text{inv}}^* \nu_{\text{inj}} \]

1. Need low \( m_t^* \) in channel direction to achieve high \( \nu_{\text{inj}} \) and maximize \( I_{\text{DSAT}} \)

Quantum Capacitance very important at thin \( T_{\text{OX}} \)

2. Need high \( m^*_\text{DOS} \) to achieve high \( C_{\text{GATE}} \) and \( Q_{\text{inv}} \) to maximize \( I_{\text{DSAT}} \)

\[ C_{\text{INV}} \sim \frac{q^2 m^*_\text{DOS}}{\pi \hbar^2} \]
III-V Materials for NMOS Channel?

+ Low $m^*$ $\Gamma$ valley $\Rightarrow$ High $\nu_{\text{inj}}$
- Low $m^*$ $\Gamma$ valley $\Rightarrow$ Low $m_{\text{DOS}}^{*}$
  $\Rightarrow$ Low $Q_{\text{INV}}$

- 2-D Quantization:
  $\Rightarrow$ Charge transfer from low mass $\Gamma$ to high mass $X$ & $L$ valleys
  $\Rightarrow$ Lowers $\nu_{\text{inj}}$

- Low $E_g$ $\Rightarrow$ Large $I_{\text{off}}$ (junction)
- High $\varepsilon$ $\Rightarrow$ Poor SCE

Projecting III-V NMOS performance based on simplistic models could lead to erroneous performance assessment.

K. Saraswat et.al., IEDM 2006

<table>
<thead>
<tr>
<th>Material/P. property</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_{\text{eff}}^{*}$</td>
<td>0.19</td>
<td>0.08</td>
<td>0.067</td>
<td><strong>0.023</strong></td>
<td><strong>0.014</strong></td>
</tr>
<tr>
<td>$\mu_{\text{n}}$ (cm$^2$/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td><strong>40,000</strong></td>
<td><strong>77,000</strong></td>
</tr>
<tr>
<td>$E_g$ (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td><strong>0.36</strong></td>
<td><strong>0.17</strong></td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.8</td>
<td>16</td>
<td>12.4</td>
<td>14.8</td>
<td><strong>17.7</strong></td>
</tr>
</tbody>
</table>
The Grand Challenges for III-V CMOS

- InGaAs Quantum Well channel
- InAlAs insulator (poor Jox)
- Ti/Pt/Au gate
- Non-self aligned contacts

Energy Band Diagram

- high-K dielectric gate insulator
- J. Del Alamo
- IEDM 2007

III-V p-type channel device

Scalable, self-aligned, E-mode device architectures

III-V epitaxy on large-area Si wafers
Ge Transistor - Back to the Future?

**Advantages:**
+ Best hole mobility (unlike III-V)
+ Si(Ge) already used in logic tech
+ Col-IV: Non-Polar

**Challenges:**
- Reference device is highly strained silicon
- Poor HiK interface:
  * Need better understanding
  * Buried strained QW Ge
- Higher dielectric constant
  * Poorer SCE
- Worse parasitic resistance
  * Worse dopant activation

![Material Property Table]

<table>
<thead>
<tr>
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<th>Ge</th>
<th>GaAs</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron mobility</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>Hole mobility</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>Bandgap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.424</td>
<td>0.36</td>
<td>0.17</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.8</td>
<td>16</td>
<td>12.4</td>
<td>14.8</td>
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K. Saraswat et.al., IEDM 2006.

**Buried Strained Ge Quantum Well**

(U. Tokyo, APL 2002)
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  - Non planar architecture

- Tunnel Transistors
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Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET.
Multi-Gate Transistor Architecture

\[ \frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \]

Multi-Gate Transistors have better SCE:
- Gates reduce spread of \( V_{\text{drain}} \)
  Enables lower threshold voltage (\( \uparrow I_D \))
- Enable lower channel doping (\( \uparrow \mu \))

Multi-Gate Transistors have lower \( E_{\text{EFF}} \):
- Optimum gate work function is away from band-edge leading to lower \( E_{\text{eff}} \) (\( \uparrow \mu \))
Multi-Gate Transistors Implementation

Multi-Gate Fin Transistor:
++ Self Aligned structure for S/D
-- Non-Planar structure

Multi-Gate Fin Transistor
Top Challenges for Multi-Gate Fin Transistors

➢ Implement High Strain in Fins?
   Planar Ref= Highly strained 4-5x p-mobility enhancement
   High level of fin strain NOT published to date

➢ High Parasitics in Fin Transistors
   Narrow fins lead to high Rext
   Fin architecture may also lead to higher fringe capacitance

➢ Manufacturing worthy Patterning
   Fin, Gate and Spacer patterning will be extremely challenging in a manufacturing environment

➢ Design
   Device Z increments quantized

• Best published drive currents for Multi-Gate Fin Transistors are significantly lower than best published planar transistors to date
• Many significant challenges remain to be resolved for Fin Transistors
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Why we Need to Beat Sub-Threshold Slope of 60mV/decade?

\[ I_D \sim (V_{CC} - V_{TH}) \]

At very low Vcc we need small \( V_{TH} \) for reasonable drive

BUT

Sub-threshold slope is limited by thermal \( kT/q \) limit

\( \Rightarrow \) \( I_{off} \) increases exponentially with \( V_{TH} \) scaling.

\[ S = \left( \frac{d \log I_d}{d V_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}}\right) \geq 2.3 \frac{kT}{q} \]

Leakage current increases \textit{exponentially} as device is scaled.
Ultimate Frontier: Overcoming Thermal $kT/q$ Limit

Electrons go over a potential barrier. Leakage current is determined by the Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET...

How to overcome the limit:
Let electrons go through the energy barrier, not over it → Tunneling
Semiconductor Band-to-Band Tunneling

- Esaki demonstrated this experimentally in 1958
- Can lead to negative resistance- Esaki diode
- Transistor: Tunneling can be controlled by gate!!
Tunnel Transistor Concept and Challenges

• Device behaves like reverse bias pin diode
• Positive Vgs induces electron electron channel
• Band bending allows tunneling at source channel interface ➔ Gate controlled band tunneling
• BTBT Transistor suffer from extremely poor drive current ➔ Need materials with more efficient tunneling

Key Messages / Summary

• **Intel’s Response to end of “traditional-scaling”:**
  - Uniaxial Strain (90nm and beyond): 32nm is 4th generation of uniaxial strain at Intel
  - HiK + Metal Gate (45nm and beyond at Intel)

  These innovations have enabled Intel to maintain historical performance gains on recent nodes

• **Future Novel Transistors:**
  - **New Channel Materials:**
    Integrate Ge & III-V on top of Silicon. Many device and material challenges remain
  - **Multi-Gate Fin Transistors:**
    Scaling benefits BUT need to demonstrate effective strain implementation, matched parasitic resistance to planar and overcome patterning challenges
  - **BTBT (Tunnel) Transistors:**
    Ultimate transistors may need tunnel injection at ultra-low Vcc. Would need new materials with more efficient tunneling and atomic scale fabrication control

  Many exciting materials, physics and integration challenges left to continue CMOS scaling