Control in Semiconductor Wafer Manufacturing

Abbas Emami-Naeini and Dick de Roover

Abstract: A semiconductor wafer undergoes a wide range of processes before it is transformed from a bare silicon wafer to one populated with millions of transistor circuits. Such processes include Physical or Chemical Vapor Deposition, (PVD, CVD), Chemical-Mechanical Planarization (CMP), Plasma Etch, Rapid Thermal Processing (RTP), and photolithography. As feature sizes keep shrinking, process control plays an increasingly important role in each of these processes. A model-based control approach is an effective means of designing commercial controllers for advanced semiconductor equipment. We will give an overview of the applications of advanced control in the semiconductor industry. It is our experience that the best models for control design borrow heavily from the physics of the process. The manner in which these models are used for a specific control application depends on the performance goals. In some cases such as RTP and lithography, the closed-loop control depends entirely on having very good physical models of the system. For other processes such as CMP, physical models have to be combined with empirical models or are entirely empirical. The resulting multivariable controllers may be *in-situ* feedforward-feedback or run-to-run controllers, or a combination thereof. The three case studies that are presented in this paper (RTP, CMP, and lithography) are representative of the leading edge applications of advanced control in the semiconductor industry.

I. Introduction

A semiconductor wafer undergoes a wide range of processes steps before an integrated circuit is produced [1]-[3]. Figure 1 illustrates some of the steps in the manufacturing of an Ultra Large Scale Integrated (ULSI) Circuit such as a microprocessor [4]. The key steps are Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD), photolithography, Plasma Etch, Rapid Thermal Processing (RTP), and Chemical-Mechanical Planarization (CMP). The standard practice for many years was to perform these steps in batches on many wafers at a time to produce large numbers of identical chips. In response to the demand for ever smaller critical dimensions (CD) of the devices on the chip, and to give more flexibility in the variety and number of chips to be produced, the makers of the tools for fabrication of integrated circuits have turned to single-wafer processes which require precise control. *Interestingly, the processes that make the chip are now beginning to use controllers which require the computational power of the chips being fabricated.* Another trend is to conduct several related steps in a "cluster" comprising of several chambers integrated into a single machine.

The authors are with SC Solutions, Inc., 1261 Oakmead Pkwy, Sunnyvale, CA 94085. A. Emami-Naeini is also a Consulting Professor of Electrical Engineering at Stanford University. Corresponding author's e-mail: emami@scsolutions.com.

The processes that deal with producing the integrated circuit (IC) on the wafer are commonly referred to as "front-end" processes, whereas "back-end" processes deal with wire bonding and packaging the IC. In this paper, we will focus on the "front-end" processes that produce the IC on the silicon wafer, and the increasingly important role of control. Front-end tools are used in a few hundred process steps to produce a ULSI circuit on a wafer. Thin layers of electrical conductors, semiconductors, and insulators are deposited with intervening steps that implant and activate dopants, anneal, etch patterns, or polish the wafer surface. A thin film deposition process may be a Physical Vapor Deposition where the source atoms are transported to the wafer by various means or may involve chemical processes in which case it is called Chemical Vapor Deposition. Both PVD and CVD can be driven by thermal processes such as Rapid Thermal Processing for post-implant anneal and Rapid Thermal CVD for oxidation, silicon epitaxy, etc. Plasmas are also used to drive PVD and CVD processes, and used for etching dielectrics and metal in building the ICs, see Figure 4.

For several decades, semiconductor manufacturers focused on finding processes that were passively stable (i.e., processes that were insensitive to input variations). The process engineer used experimental trial-and-error approaches to specify processing protocols (*recipes*) for various process steps. But this approach has become increasingly difficult to sustain over the last decade as the semiconductor industry extended Moore's Law well into the future by increasing the spatial density of ICs as well as increasing the size of wafers to 300 mm in diameter. For example, Intel's new Tukwila microprocessor packs over two billion transistors on a die size of 21.5x32.5mm^2. These integrated circuits are fabricated with 65 nm feature size. Such increasing densities and shrinking feature sizes result in increasingly tighter tolerances, which means there is less slack (i.e., "error budget") available in the manufacturing

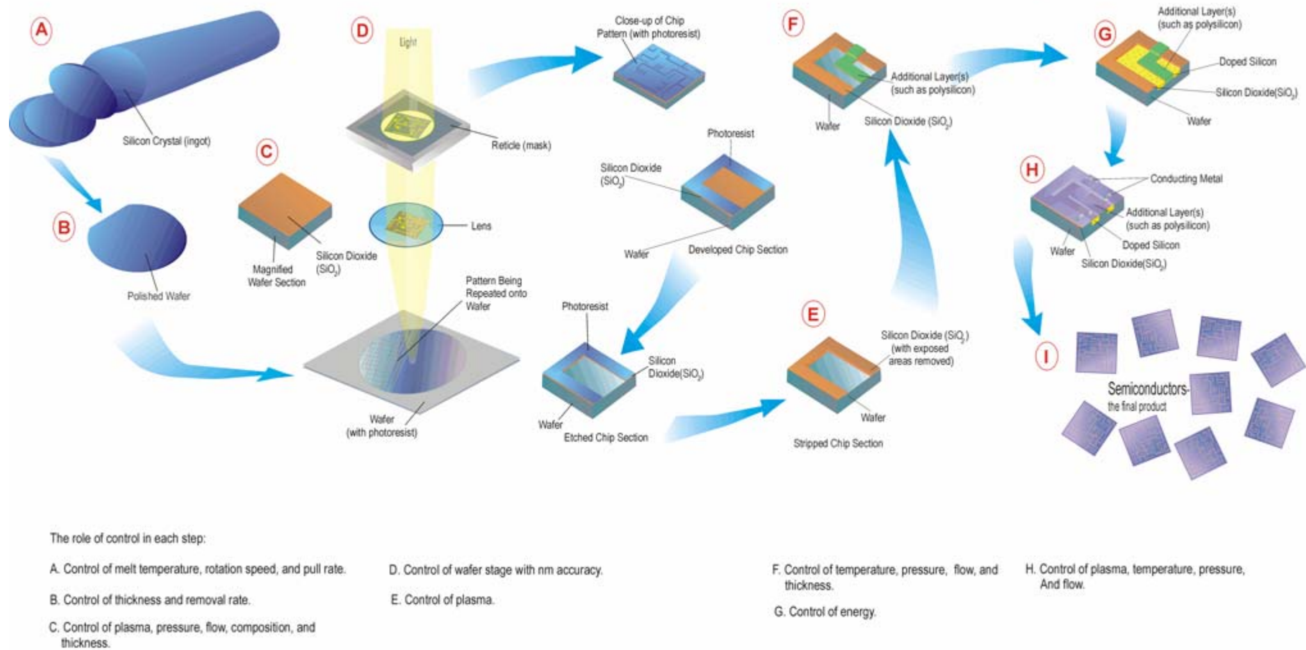

Figure 1. Steps in making an integrated circuit [4].

process. Hence precision control is becoming a necessity. As a result, integrated computer-controlled wafer fabrication is playing an increasingly important role in the semiconductor industry [5-12].

Control is ubiquitous in semiconductor manufacturing as shown in Figure 1 which shows the major steps in the fabrication of ultra large-scale integrated (ULSI) circuits such as microprocessors along with some of the associated control aspects. In production of the silicon ingot, control of melt temperature, rotation speed, and pull rate is required. In CMP, control of film thickness and removal rate is necessary. In etch, the control of plasma power and uniformity is required in addition to control of the temperature of the chuck. In lithography control of position of the wafer stage with nm accuracy is necessary and control of temperature for the bake process is very important. In RTP, precise control of temperature is a must. Control of pressure, temperature, and flow is ubiquitous. Robotics (wafer handling) is omnipresent in the fab.

The semiconductor manufacturing process flow, when highly simplified, can be divided into two primary cycles of transistor and interconnect fabrication. The transistor cycle is the basis of the most advanced chips, see Figure 2. With a wafer as the starting point, it involves epitaxial silicon (Epi), dielectric deposition, photolithography, etch, wafer cleaning, ion implantation, and RTP processes. The interconnect cycle is the one used with high performance copper interconnects that have replaced the conventional aluminum interconnects, see Figure 3. It involves dielectric deposition, photolithography, etch, metal deposition using PVD, electroplating, and CMP leading to the finished chip. After processing the chips are coated with plastic or ceramic packaging to seal them tightly.

The starting point for a model-based control design strategy is to understand these physical processes, followed by derivation of mathematical models. The high-order models are tailored for control through model-order reduction and are validated using experimental data. Finally, feedback controllers are designed using these reduced-order models and tested in closed-loop simulations before the control code is downloaded on to the real-time computer used for equipment control.

In this paper, we briefly survey the control issues for some of the important front-end tools followed by discussions on modeling for control and some of the control strategies adopted in the industry including feedback and run-to-run control. In the three following sections we describe in greater detail the application of modeling and model-based control to three processes: RTP, CMP, and lithography coater/developer systems.

II. Overview of Typical Wafer Processing Equipment

As described earlier, there are many process steps required to produce a ULSI circuit on a wafer. The physical processes can be organized into groups that approximately correspond to the type of equipment that would be used to perform that process. In this section we discuss some of the important types of semiconductor processing equipment and the related control issues.

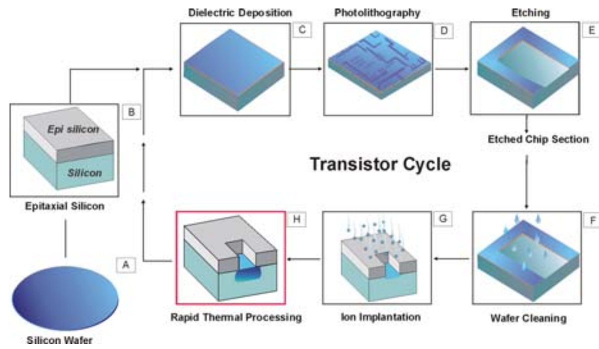

Figure 2. The transistor cycle in manufacturing an integrated circuit.

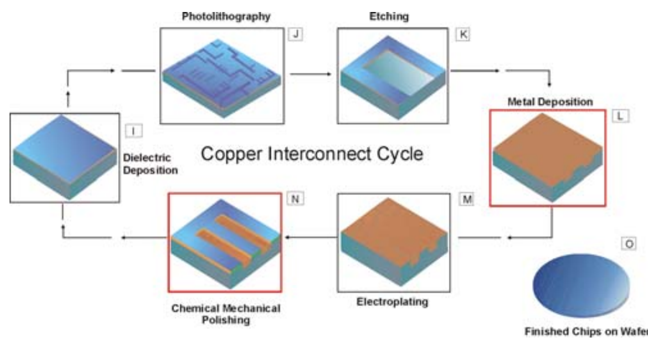

Figure 3. The copper interconnect cycle in fabricating an integrated circuit.

Specifically we discuss PVD, CVD, thermal, etch, photolithography, and CMP systems.

An understanding of the aims of various semiconductor processes helps one better understand the function of the associated equipment (see Figures 1- 3). At the start of the wafer processing chain, large cylinders of single-crystal silicon, ingots, are sliced into wafers, ground to a specific thickness (e.g., 300 mm diameter wafers are 0.775 mm thick) and polished to be smooth. A thin layer of epitaxial (i.e., single crystal) silicon, or "epi", is deposited using CVD and the wafer is ready for use in a fabrication facility (commonly called a *fab*). All the transistors (and diodes, resistors, etc.) are fabricated on this epi layer. After fabrication, the transistors are electrically interconnected. Figure 4 shows a sample sequence of the processing steps. This example illustrates how one can produce a localized region in the wafer that has different electrical properties (P- or N-doped) than its surroundings. Figure 4 shows an oxide layer being deposited (or formed by oxidizing surface silicon), a pattern being etched into the oxide to expose a specific pattern of silicon, impurities being subsequently implanted into the exposed silicon, and finally those impurities being diffused to form a localized region that is electrically distinct. In a typical IC there can be hundreds of steps and multiple layers of metal interconnect inlayed into patterned dielectric [1]-[3].

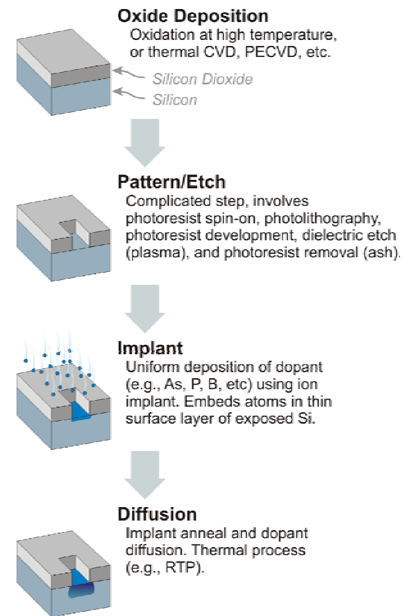

Figure 4. Some representative process steps for producing an integrated circuit.

However, the main point to be made here is that many iterations of deposition, planarization, photolithography, etch, and more 'deposition and planarization' is a central characteristic of integrated circuit fabrication. A more detailed exposition here is beyond the scope of this paper, and the interested reader should consult a standard book on this subject, e.g., [1]-[3].

For the control engineer interested in controlling the processing equipment, the main issues can be summarized with the following five questions:

1. What are the processes involved (physics)?
2. What are the actuators (inputs)?
3. What sensors are available (outputs)?
4. What are the performance metrics?
5. What are the disturbances and uncertainties?

In the remainder of this paper, we will briefly discuss these five aspects for the three classes of semiconductor equipment that were noted earlier: RTP, CMP, and lithography processes.

III. Control of Semiconductor Processes

Figure 5 shows a general control structure that addresses the process control requirements. The three components of the controller are (1) the planner, (2) the regulator, and (3) the estimator. The feedback controller consists of the regulator and the estimator. The *planner* translates the desired product characteristics into an ideal (or nominal) set of process inputs (controls) and reference signals and is the feedforward controller. Depending on the process, the inputs might be constant or follow a very complex time

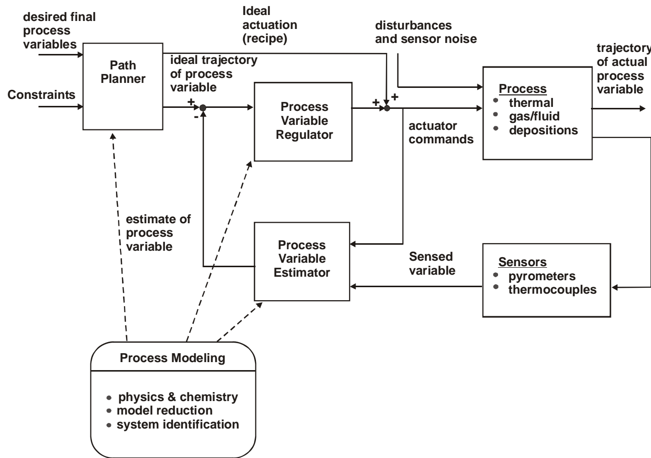

Figure 5. General control structure for semiconductor industry.

history. If the model and the planner were perfect *and* there were no process disturbances, the planner would be all that would be required—but in the real world this is never the case. Thus, the *regulator* uses the difference between the desired product characteristics and those actually being produced to compute corrections to the nominal process inputs computed by the planner; this is the feedback controller. Together, the planner and the regulator constitute the model-based control portion of the solution. A further complication arises because in many cases it is impossible to measure the relevant product characteristics *in-situ* (either because it is too expensive or the sensor has nor been invented yet). Thus, the *estimator* uses a model of the process conditions that can be measured in real-time. The estimator constitutes the model-based sensing portion of the solution. By using a process model, the estimator can be designed to infer the critical variables from the sensed variables. Hence, model-based estimation is a means to "transcend" inadequacies in sensing. The regulator and the estimator have to be on-line (real-time) functions. The planner is nominally designed off-line, but it could also be constructed to utilize feedback on a run-to-run basis.

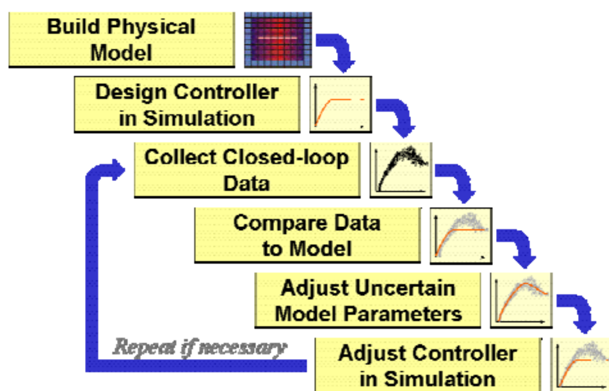

Figure 6. Model-Based control system design.

A. *Model-Based Control*

There are many advantages of the model-based control approach. The controller can be "tested" for a wide range of wafer/process variations in simulation. A physical model of the system can be modified to answer "what if" tests for equipment/process modifications. The approach provides the ability to perform controller development in parallel with chamber (reactor) development. In the semiconductor industry access to the equipment is a premium and it is a great advantage to be able to carry out the control system design without access to the equipment. The approach provides a tool for trouble shooting to respond to problems in the field. The model-based approach provides the opportunity for model-based fault detection isolation accommodation. It is generally true in the semiconductor industry that the next generation equipment is a modification of the current system. Hence the availability of the model provides a path for continued product improvement.

Figure 6 shows the model-based control design cycle. The first step in the development of a model-based controller is the development of a *physical* model which accurately reflects the actual behavior of the system to be controlled. For example, for a Rapid Thermal Processing System (RTP) a detailed thermal model of the system is developed. The model contains unknown physical variables that are identified from experimental data. A comparison of the model response with the actual system output provides a measure of model accuracy. The next step in the cycle is the development of a model-based controller. Using the model, we use a variety of advanced feedback control designs to derive candidate controllers. The closed-loop system is then simulated in a graphical block diagram simulation environment to assess the merits of various candidate controllers. Once a satisfactory controller has been identified which meets the specifications (e.g., temperature uniformity for RTP), real-time code can be generated automatically to run on a rapid prototyping platform which will control the equipment directly. The controller's performance on the actual equipment can be determined and design iterations can be carried out if necessary. When satisfied with the controller performance, the controller can be targeted to a variety of computers or embedded microprocessors.

B. *Types of Control*

At the highest level, control of a fab involves the control of wafer movements and scheduling of the individual pieces of processing equipment. Highly sophisticated and flexible manufacturing can only be achieved by a combination of complex scheduling and real-time control systems. The nature of the scheduling involves discrete event systems theory and related optimization. Robots are routinely used to automate wafer transport between process equipment, wafer handling within process equipment, and within a

cluster. Hence robotic control plays an important role in a fab. The next level is the control of the individual pieces of process equipment, which is the main focus of this paper. Finally there are control of fluid and material flow, temperature, and pressure where the use of Proportional plus Integral (PI) [4] is ubiquitous. As already mentioned, there are at least five types of control strategies employed in the use of the process equipment: open-loop, end-point, *in-situ* feedback, feedforward, and run-to-run control.

Open-loop control has been the most common strategy until recently; actuators are held constant. End-point control uses an *in-situ* sensor to detect the end-point of the process, i.e., to detect when the desired process result has been achieved, at which point in time the process is stopped. This type of control is common in processes such as etch.

In-situ feedback control is used for real-time feedback control using real-time sensors. Examples include temperature control in RTP using pyrometers and metal layer thickness control in CMP using eddy current sensors.

Feedforward control is employed through provision for nominal control settings as discussed above. Since we wish to move the system from one operating point to another along a specified trajectory, we can determine the approximate inputs to accomplish this. Consequently, we can apply this input directly to the system. The feedforward controller should approximate the inverse dynamics of the plant. An example in RTP is the use of nominal lamp settings and the associated temperature profiles. Another form of feedforward is the use of information on the end product from the previous equipment. An example in CMP is the use of incoming copper profile from the electroplating for the start of the planarization step.

Run-to-run control is a form of discrete process control in which a product recipe is modified using *in-line* or *ex-situ* metrology between "runs" to minimize or eliminate process drifts, and variability (due to the nonlinear nature of the relationship between product characteristics and what can be measured in real-time in the system) [13]. In effect the discrete process "sample rate" is the length of the process run. An example of run-to-run control is adjustment of sensor or reference temperature "bias" in RTP or adjustment of polish time in CMP.

IV. RAPID THERMAL PROCESSING: RTP

A broad class of semiconductor processing is *thermal processing*. Thermal processing systems typically involve ramping up and ramping down the wafer temperature in a controlled way to facilitate some thermally-driven process such as oxidation, anneal, diffusion, or chemical vapor deposition (CVD). In the case of implant anneal, an ion implant system (a type of PVD process) first implants a layer of dopant (e.g., boron or arsenic atoms) into the surface layers of a wafer. The impact of these atoms (ions) causes damage to the crystal structure that must

Figure 7: Applied Materials' RTP system (Courtesy Applied Materials).

subsequently be annealed using a thermal process where crystal defects diffuse out of the wafer. To prevent excess diffusion of the dopant away from the surface and provide the thinnest possible layer of doped (and activated) semiconductor material, it is desirable to use RTP to anneal the damage.

In RTP equipment, one can typically raise the temperature quickly (200°C/s or more) from a relatively low temperature to a temperature above 1000°C while maintaining good within-wafer uniformity, see Figure 7. In addition to rapid thermal anneal (RTA), rapid thermal oxidation (RTO) and other processes use RTP equipment. Modified single wafer RTP-like systems are also used for CVD (RTCVD). Other types of thermal processing are done using furnaces where large numbers (25+) of wafers (batch) can be processed at once. These batch furnace systems tend to be slower in terms of ramp-up, ramp-down, and process times, but the time per wafer can be high if enough wafers are processed at a time. Historically almost all thermal processing was done using batch furnaces, but the trend is increasingly toward single wafer systems, because of better control of the individual wafers.

A schematic cross section diagram of an RTP system is shown in Figure 8 [14]. A bank of over 400 tungsten halogen lamps is arranged in a honeycomb pattern which constitutes the actuators of the system. Seven pyrometers are used to measure the temperature on the backside of the wafer at a rate of 100Hz. The wafer is lifted by magnetic levitation and is rotated during processing. The dominant physical phenomenon in RTP is radiative heat transfer. Actuators in RTP are the lamps that heat the wafer. Typically multiple lamps are used to provide a high spatial resolution across the wafer as well as high power to quickly heat the wafer. Sensors typically include pyrometers, which are ideal sensors for measuring radiation of moving objects (rotating wafer). Uncertainties in RTP include radiative properties of wafer and chamber walls.

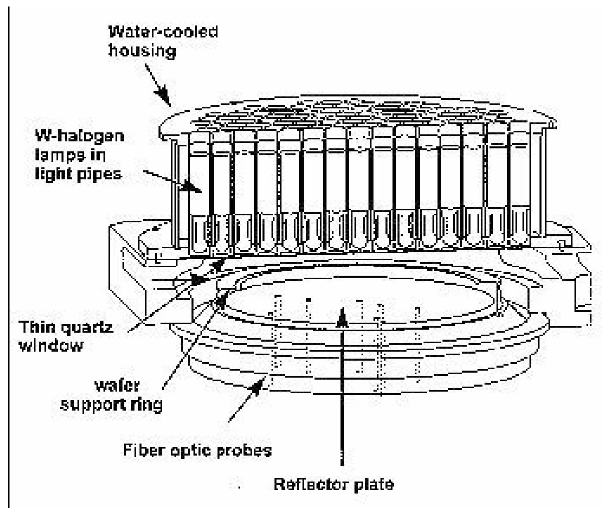

Figure 8. Cross sectional diagram of Applied Materials' Radiance Plus RTP system [14].

We describe our strategy to design controllers for the RTP system next. Precise temperature control is critical to obtaining required high performance. In an RTP chamber, many heaters affect the temperature at each location where it is measured. Multi-Input Multi-Output (MIMO) control that explicitly accounts for the influence of each heat source on each temperature sensor is needed for high performance. With such strong physical coupling, it is difficult to obtain high performance control of the temperature profile using single loop conventional controllers commonly used in industrial applications. Moreover, since previous approaches relied heavily on precise calibration, small changes in chamber design or wafer geometry can require substantial and time-consuming efforts in control re-design. The necessity for meeting extremely high performance specifications requires that the control system be optimal with respect to the specific process being controlled, and be robust to cope with variations in the system components.

Control Problem Formulation

To be able to design temperature controllers that achieve the desired wafer thermal performance, it is important to consider the performance specifications in terms of temperature control quality. The temperature control problem in an RTP system typically has the following demands to ensure uniform wafer properties:

1) Steady-state tracking, better than 1°C, preferably zero error;
2) Insensitivity to sensor noise, process disturbance and variations, such as wafer-to-wafer variations (e.g., variation in wafer emissivity), changes in temperature set points, etc.

These demands pose a substantial challenge for controller design, since very high precision has to be obtained while retaining sufficient robustness in the design. It is noted that even if the controller has zero-tracking errors at points on the wafer where the temperatures are sensed (usually five points or less), there could be large departures from the recipe temperature at several points where the temperatures are not measured. Our controller solves the problem using an estimate of the maximum error based on model prediction. This is a very important advantage in applying model-based control to RTP.

We approach the control problem by using linear design techniques [5]. Hence, we have to derive a linearized model of the system from the nonlinear discretized model. Two alternatives are possible. The first option is to directly linearize the reduced nonlinear model of the system. The second option is to linearize the full nonlinear model, and then use the POD reduction algorithm [5].

Controller structure

The controller structure for RTP is similar to the general structure shown in Figure 5. The *feedforward* controller takes advantage of the known reference temperatures to compute a suitable control signal that is injected in the closed-loop. Due to the relatively simple structure of a feedforward controller, it can be nonlinear and can be based directly on the nonlinear RTP model. An important practical consideration is whether the reference is known to the feedforward controller *a priori*, or if it is provided in real-time. The latter case is the most common in practice, but the first option allows a global optimization of the trajectory rather than point-to-point optimal commands. It is assumed here that the reference will be provided in real-time.

The *feedback* controller is based on a linear design, as dynamic output feedback is required. Its task is to address any mismatch that arises from the limited fidelity of the feedforward controller, and to deal with the process disturbances. The feedback controller includes logic to deal with integrator anti-windup due to lamp saturation nonlinearities [4].

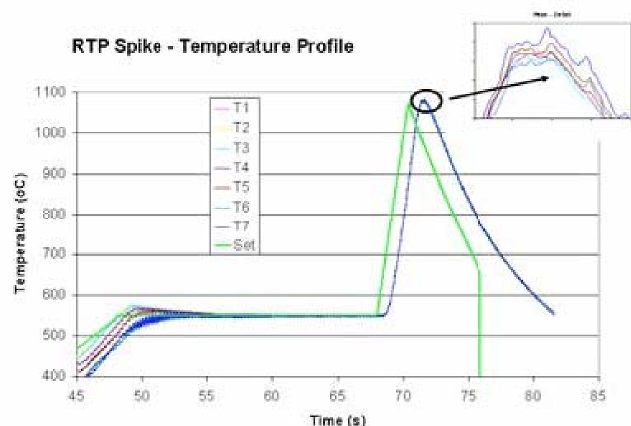

Figure 9. RTP spike anneal temperature profile [14].

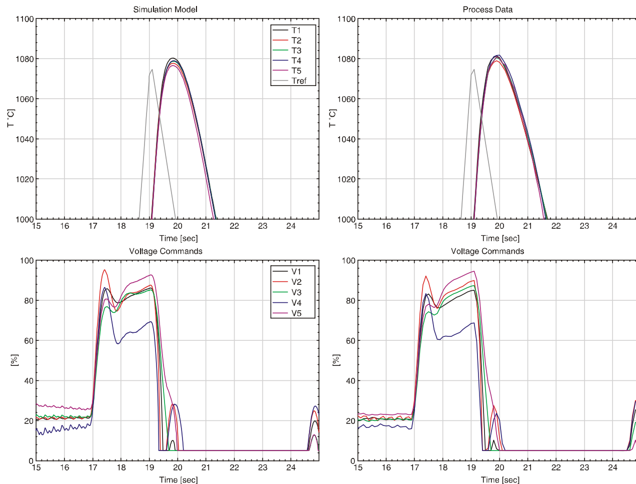

Figure 10: Comparison of model simulation (left column) with actual measurements (right column) on a 200 mm single-wafer RTP chamber during a fast-ramp process [5].

The *prefilter* smoothes the temperature reference, the latter being piecewise linear and thereby having discontinuities in the rate of change. If the "raw" reference is tracked closely by the controller, it will inevitably result in overshoot, because finite lamp dynamics introduce delays between the feedback signal and the actuator (i.e., the system is at least of second order). In addition, the prefilter reduces excessive control action due to the sudden changes in rate.

Figure 9 shows closed-loop response of the system for a temperature spike anneal. Figure 10 shows a comparison of the closed-loop simulation and actual closed-loop performance of the system. It shows excellent agreement between the model and the data from the RTP system.

V. CHEMICAL-MECHANICAL PLANARIZATION: CMP

Chemical-Mechanical Planarization (CMP) is a critical and enabling step for semiconductor fabrication interconnects technology. At the 45 nm, 32 nm, and 22 nm nodes, the planarization process must take into account the increasingly more stringent requirements on thickness, spatial uniformity, planarity, conformality, thermal stability, and mechanical integrity.

When multiple layers of oxide and metal are deposited onto etched surfaces the resulting surface is typically not flat. CMP is used to produce a planar mirror-like wafer surface for subsequent processing by smoothing a nominally macroscopically flat wafer to almost atomic level. A typical rotary CMP machine consists of a rotating wafer pressed onto a grooved rotating platen containing abrasive slurry. The slurry chemically reacts with the wafer surface to be polished, and the pressing rotating action typically abrades the surface atomic layer-by-atomic layer. The major problems in CMP are controlling the material removal (or, equivalently, the material removal rate) and the uniformity on each run, and reproducibility from run-to-run. The goal of CMP processing is to achieve a specified thickness and uniformity in a repeatable fashion. Actuators for a rotary CMP machine are applied pressures, wafer and platen rotation speeds and slurry flow rate. Sensors for CMP include eddy current and optical sensors for measuring film thickness, motor current sensors for measuring friction, and temperature sensors.

Currently, Chemical-Mechanical Planarization (CMP) remains the wafer planarization technique for semiconductor manufacturing. There are more than 500 processing steps involved in manufacturing advanced semiconductor chips, of which 10 to 20 steps involve CMP processes. Furthermore, many of the CMP steps occur in the late stages in the processing of the wafer, thus making any re-processing very costly. The adoption of copper damascene technology by the industry has resulted in the need for copper CMP processes spanning three semiconductor technology nodes: copper/silicon dioxide, copper/low-k, and copper/ultra-low-k (k is the dielectric constant). Each of these technologies presents unique challenges to the industry. The characteristics of the problems are smaller features, new materials, and more layers to control. The issues involve, dishing, erosion, planarity, zonal control, multi-point control, and stress-free CMP.

A schematic diagram of a rotational CMP system is shown in Figure 11. Figure 12 shows a typical CMP architecture with three platens for planarizing bulk copper, barrier and residual.

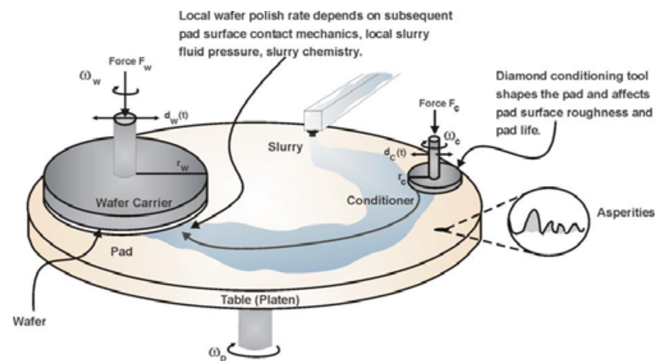

Figure 11. Schematic of a typical rotational CMP System.

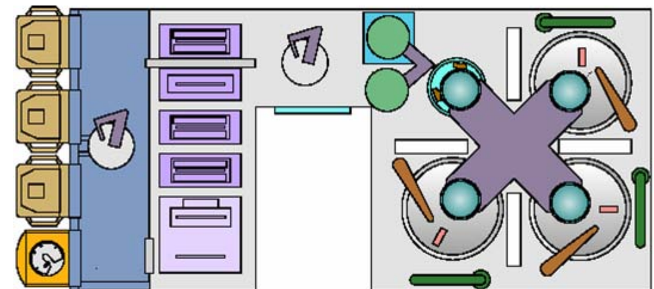

Figure 12: CMP system architecture showing 3 platens for Applied Materials Reflexion LK system [15].

A. *Dynamic CMP Model* [8]

We have developed a *static* three-dimensional (3D) contact mechanical model that determines the interfacial contact pressure between wafer and platen, based on specific values for load pressure, ring pressure and average friction coefficient. In addition, a static kinematic relationship was obtained between the platen rotational speed and wafer rotational speed, and the relative velocity between wafer and platen at a given point on the wafer. These static models were combined to compute the static removal rate according to Preston's equation [16]:

$$\frac{dh^i(t)}{dt} = K_p p_c^i(t) v_r^i(\omega_p, \omega_w), \qquad i = 0,1,\ldots,N$$

where K_p is Preston's coefficient (proportionality constant), $p_c^i(t)$ is the contact (interface) pressure at node *i* along the radius, and time *t*, and v_r^i is the time averaged relative speed between the point of interest on the wafer (*i*) and its point of contact on the pad. The static models were integrated into a dynamic model that predicts the wafer thickness as a function of time-dependent inputs. The dynamic model is shown in Figure 13.

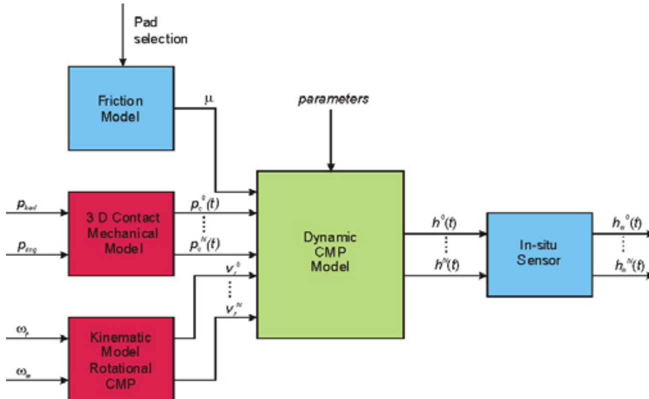

Figure 13. Schematic of dynamic CMP model. ***h^i(t), i***=0,1,...,N represents the wafer thickness in Angstrom for each node ***i***, as a function of time [8].

In addition to the 3D contact mechanical model (red) and kinematic model (red), a model has also been added for friction, based on pad selection (blue), a CMP *in-situ* sensor model (blue), and a model that computes the CMP dynamics (green) based on customizable model parameters. Planarization performance is based on Within-Wafer- Non-uniformity (WIWUN) and Within-Die-Non-uniformity (WIDNU) thickness uniformity.

As most feedback techniques are based on linear models, a linear model has been derived from the non-linear dynamic CMP model that describes the linear CMP behavior in a specific operating point (a selection of constant input values). Comparison of the dynamic behavior between the linear and nonlinear model shows a good match in the operating point, and gradual performance degradation when moving away from the operating point. The full-order linear model was further reduced to a 4-output, 4-state, 4-input model for feedback control design. The reduced order linear model was used for feedback controller design using a Linear Quadratic Gaussian (LQG) design technique. Figure 14 shows the closed-loop performance using a model-based feedback controller that meets the specifications in terms of WIWUN and WIDNU.

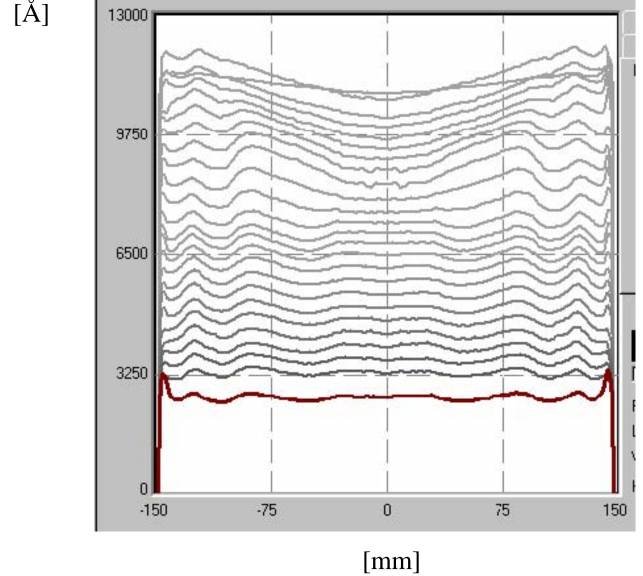

Figure 14: CMP closed-loop performance for a 300mm wafer: copper thickness in [Å] vs. radius in [mm] [15].

One of the biggest challenges faced by the semiconductor manufacturing industry today is the integration of low-k and ultra low-k materials with copper interconnects for 45 nm, 32 nm, and 22 nm technology nodes to replace conventional SiO_2. The low mechanical strength of these dielectric materials reduces their resistance to mechanical damage. Mechanical damage, including cracked dielectric and lifted copper lines, can be reduced by decreasing down force during the CMP processing, which reduces the frictional shear forces that cause such damage. Conventional planarization using CMP can damage low-k (and ultra low-k) dielectric materials used with copper interconnects. Development of next-generation low-pressure CMP technologies and advanced slurries are required.

VI. Lithography

Lithography is the semiconductor industry's key enabling technology. The lithography step is the most critical of the semiconductor wafer manufacturing steps and a key enabler in fabrication of ULSI circuits. It is directly responsible for increasing transistor densities and shrinking feature sizes. Optical lithography continues to extend its application with

the use of 157nm technology for 65nm to 45nm nodes. Lithography is the process of defining useful shapes on the surface of a semiconductor wafer. Typically this consists of several pre-exposure steps, a patterned exposure into a photosensitive material (photoresist), and several post-exposure steps, see Figure 15.

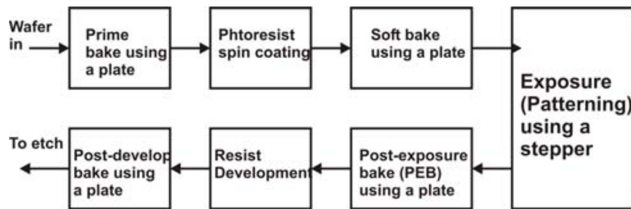

Figure 15. Steps in lithography processing [17].

During the exposure step, ultraviolet light from an arc lamp passes through a mask bearing the image of the circuit. A complex lens apparatus reduces this image and projects it onto the photoresist. The photoresist, a polymer coating, reacts to the light; the exposed area is then removed with a solvent. This technique is called photolithography, and lithography machines are called wafer steppers, because a wafer is processed in an alternating fashion of moving (stepping) the wafer and exposing that part which is underneath the lens.

The positioning of a wafer under the lens is performed by a wafer stage, and the mask can be moved as well using a reticle stage. Since the positioning of a wafer has a large impact both on the achievable throughput and yield, in addition to the optics, the overall performance of a wafer stepper is largely determined by its stages. Consequently, these stages need to have extremely high positioning performance. Laser interferometry is used to measure the position of a stage with sub-nanometer accuracy. Typically, (linear) electro-motors are used to drive a stage. Control problems include aligning the wafer with the optics, stepping the wafer with high speed, synchronizing the wafer and the reticle stage, and suppressing disturbances such as friction and thermal disturbances [18]-[19].

In the sequel we discuss wafer stage positioning during the exposure step as well as temperature control for the bake plate used in pre- and post exposure steps.

A. Lithography Wafer Stage Positioning Systems

In this section we briefly summarize the relevant technical aspects of step-and-scan systems. Successful semiconductor fabrication requires high performance for each step in the manufacturing process itself. Lithography is one of the most important steps in semiconductor manufacturing.

Figure 16 shows a picture of a step-and-scan machine. The number of ICs on a wafer varies from approximately 200 to 500 (for a 300mm wafer). Due to limited lens sizes only a small part of the wafer can be exposed at a time. In older machines, one IC at a time was exposed, and the wafer was moved from one IC to another after exposure.

Figure 16. PAS 500/500 Step & Scan System.

In newer machine designs, a *scan* principle is applied. In these machines, a rectangular area of the wafer is exposed *while the wafer is moving*. In order to have the correct image exposed, the mask is now also moved, over a so-called "slit" the size of which determines the area of exposure. The positioning of a wafer under the lens is performed by a *wafer stage*, and the mask is moved over the slit by a *reticle stage*, see Figure 17. In order to obtain a high quality image, the movements of the wafer stage and the reticle stage need to be synchronized accurately during exposure.

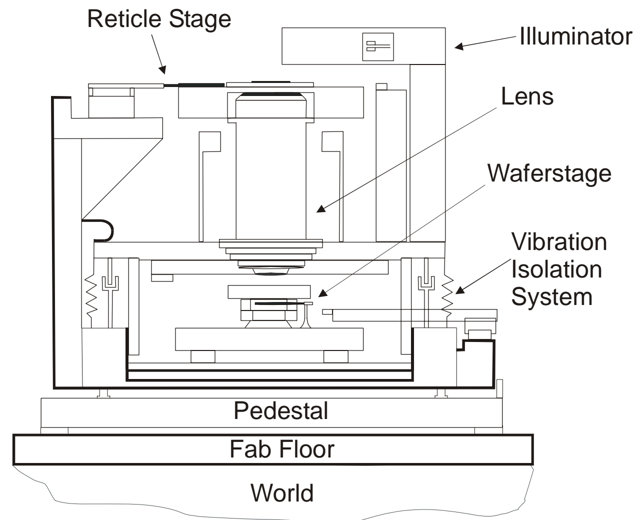

Figure 17. Schematic cross-section of the PAS 5500/500 Step & Scan System.

The slit is narrow in the direction of motion of the wafer, and is approximately 120 mm in the perpendicular direction. The stroke of the reticle stage is limited to approximately 400 mm. Because of this limited stroke and the image reduction by the lens, only a *field* of about 30×45 mm is exposed in one scan. The complete wafer has to be exposed in several scans. In between scans, the wafer has

to be moved ('*stepped*') from one field to another. The procedure of alternately moving and exposing is called *step & scan*. During this procedure, the wafer stage makes a typical movement that is called *meandering*, see Figure 18. An instructive animation of the whole process can be seen at ASML's Website.

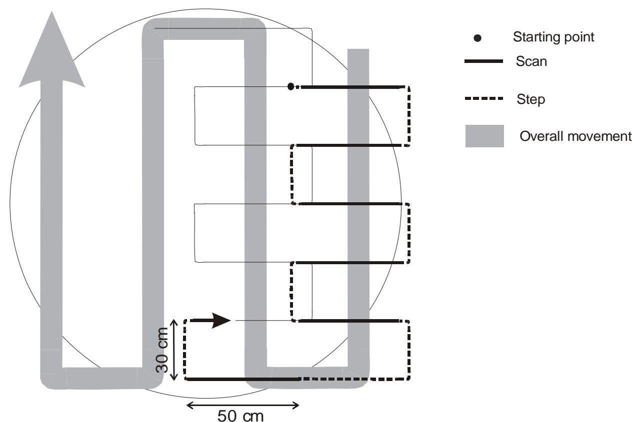

Figure 18. *Meandering*: movement of the wafer relative to the center of the lens.

For proper exposure, both the reticle stage and the wafer stage movements need to be almost error-free. The error budget is 10% for the motion system and 90% for the other subsystems (optical, alignment, thermal effects, etc.).

Two main performance characteristics of a wafer stepper are *throughput* (the number of processed wafers per hour) and *yield* (the number of acceptable ICs per wafer). Since the positioning of a wafer has a large impact both on the achievable throughput and yield, the overall performance of a wafer stepper is largely determined by its wafer stage. Figure 19 shows how model-based actuation using input shaping can improve the throughput of the wafer positioning process [18].

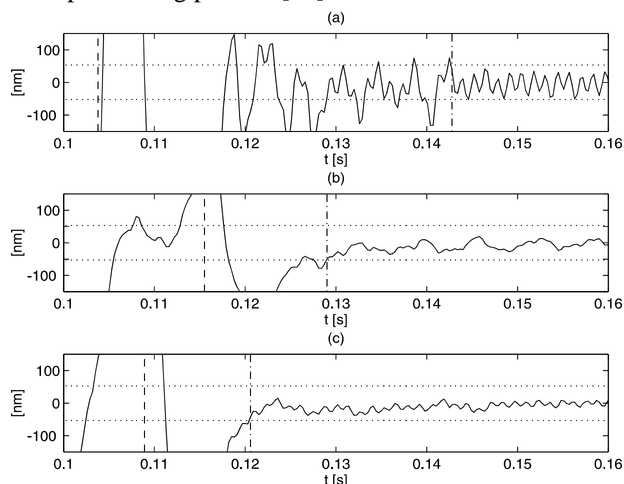

Figure 19. Wafer stage performance. (a) Vibration inducing actuation, (b) Standard industrial actuation, (c) Model-based actuation using input shaping.

Step & Scan technology puts even greater demands on the mechanical tolerances of the stage motion as compared to the previous generation systems. The traditional step & repeat only needs to move the wafer rapidly to a new position, and maintain it accurately in the same position during exposure, see Figure 19. In contrast, the Step & Scan mechanism has to move both the wafer and mask simultaneously while holding the position accuracy continuously within nanometers during the scan.

B. *Lithography Coater/Developer Systems*

A typical lithography process involves seven major steps: priming, spin coating of resist, soft bake, exposure using a stepper, post exposure bake (PEB), development, and post-development bake (refer back to Figure 15). The priming step used to promote adhesion of the polymer photoresist and decreases the likelihood of the features lifting during the develop process. This is followed by a thin layer of photoresist spin coated on the wafer. The solvent is evaporated from the resist using the hot plate by a "soft-bake" step. After patterning by a stepper using exposure of the resist, a post-exposure bake process is carried out. The image is developed next forming the desired pattern. Baking the wafer after development can improve the thermal stability of the pattern prior to subsequent processing such as etch. The overall goal is to produce printed lines with the smallest line widths — referred to as Critical Dimension (CD) — that meets a tight specification. The response of the PEB resist sensitivity to temperature, both transient and steady-state, has been identified as a significant factor contributing to the overall performance.

Figure 20 shows a standard commercial bake-plate. The bake step consists of placement of the wafer on the substrate. The wafer may be placed directly on the plate or can be held up by several proximity pins. The bake temperature is typically between 70°C to 180°C and the processing time is between 1-10 minutes. After processing, the substrate is cooled by a chill plate or cold air. The plate is typically divided into approximately half a dozen zones that use resistive heaters. Temperature sensors are placed near the top of the bake plate in each zone. The control involves the interaction of the wafer and the hot plate.

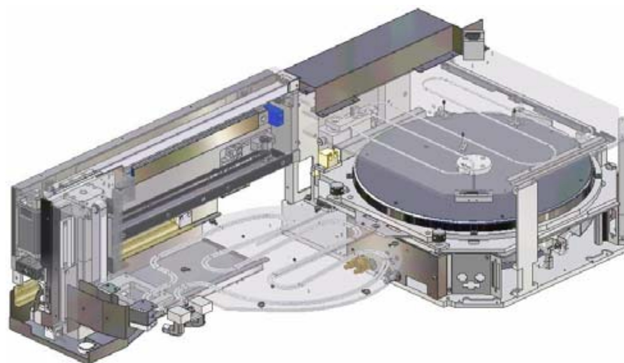

Figure 20. Picture of a lithography bake plate for a 300mm wafer.

A multivariable feedback controller is required to achieve the proper temperature uniformity (0.2°C). When the cold wafer is placed onto the hot plate, the hot plate must react to and reject this disturbance, see Figure 21.

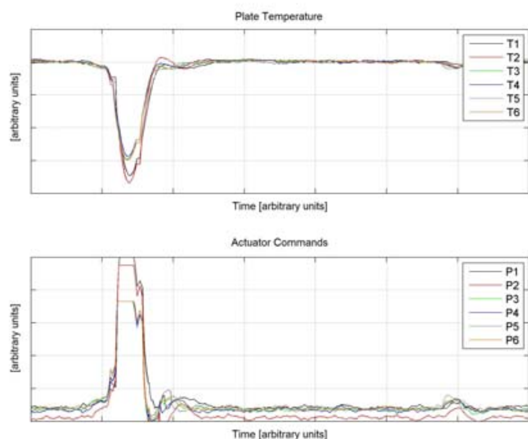

Figure 21. Temperature and actuator performance in response to placing a cold wafer onto a hot plate.

It is desired that the disturbance response be fast and accurate, typically without any overshoot. The wafer then needs to be heated to the proper process temperature and temperature uniformity is critical so all the temperatures must reach the steady-state together. During cool down, the feedback controller must also be active to achieve a controlled cool down.

The physical model for the bake plate is a conduction convection model and may be written in the standard state space form

$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

where x is the state vector of temperatures, u is a vector of heater powers, and y is a vector of temperature measurements. A multivariable LQG feedback controller was designed for this system that meets the control system specifications.

VII. Summary and Conclusions

We have provided a brief overview of the process modeling and control system design issues for some of the important semiconductor manufacturing equipment, highlighting three important processes RTP, CMP, and lithography. Due to increasingly stringent performance requirements, model-based feedback-feedforward control system design is becoming more prevalent, in addition to run-to-run control, which is now commonly used in the fabs. It is anticipated that during the current decade many more of the semiconductor fabrication equipment will employ sophisticated *in-situ* feedback control as new sensors become available. In parallel, sophisticated fault detection isolation accommodation algorithms will be implemented throughout the fab. It is anticipated that some process equipment, such as photolithography, will employ sophisticated iterative learning controllers [19]. This adoption of complex closed-loop control systems by the semiconductor industry presents new challenges and opportunities for control system engineers especially for the upcoming 450 mm wafers. Progress in equipment scheduling and Advanced Process Control (APC) promise to bring the industry closer to the dream of “all light out” automated fab operations. It is important to emphasize that success depends on a multidisciplinary approach with material scientists, mechanical design engineers, process engineers, physicists, chemists, and control engineers all working closely toward providing an overall optimized system.

Acknowledgement

We are grateful to our colleagues J. L. Ebert, R. L. Kosut, L.L. Porter II, G.W. van der Linden, and S. Ghosal who have made an interdisciplinary collaboration amongst modelers, control engineers, and semiconductor process engineers successful. We are also grateful to NSF SBIR program for funding our research.

References

[1] S. M. Sze, *VLSI Technology*, Second Edition, McGraw-Hill, Inc., 1988.

[2] S. Wolf, *Microchip Manufacturing,* Lattice Press, 2004.

[3] *Handbook of Semiconductor Manufacturing Technology*, Y. Nishi and R. Doering, Eds., Marcel Deckker, 2000.

[4] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 5th Ed. Prentice-Hall, 2006.

[5] A. Emami-Naeini, et al., “Modeling and Control of Distributed Thermal Processes,” *IEEE Trans. Control Systems Technology*, Vol. 11, No. 5, pp. 668-683, September 2003.

[6] A. Emami-Naeini, J. L. Ebert, D. de Roover, and S. Ghosal, “Model-Based Control for Semiconductor and Advanced Materials Processing: An Overview,” in *Proc. American Control Conference*, 2004.

[7] J. L. Ebert, et al., “Model-Based Control of Rapid Thermal Processing for Semiconductor Wafers,” in *Proc. American Control Conference*, 2004.

[8] D. de Roover, A. Emami-Naeini, J. L. Ebert, “Model-Based Control for Chemical-Mechanical Planarization (CMP),” in *Proc. American Control Conference*, 2004.

[9] S. Ghosal, R. L. Kosut, J. L. Ebert, and L. L. Porter, II., “Multiscale Modeling and Control of RF Diode

Sputter Deposition for GMR Thin Films," in *Proc. American Control Conference*, 2004.

[10] T. F. Edgar, S. Butler, W. J. Campbell, C. Pfeiffer, C. Bode, S. B. Hwang, K. S. Balakrishnan and J. Hahn, "Automatic Control in Microelectronics Manufacturing: Practices, Challenges, and Possibilities," *Automatica*, Vol. 36, No. 11, pp. 1567-1603, 2000.

[11] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 2007.

[12] J. Baliga, "Advanced Process Control: Soon to Be a Must," *Semiconductor International*, July 1999. Available at http://www.einsite.net/semiconductor/index.asp?layout=article&articleid=CA170290.

[13] E. D. Castillo, A. M. Hurwitz, J. Moyne, *Run-to-Run Control in Semiconductor Manufacturing*, CRC Press, 2000.

[14] V. Vitale, et al., "Use of Virtual Metrology for *in-situ* Visualization of Thermal Uniformity and Handoff Adjustment in RTP Critical Anneals," *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, pp. 349-353, 2008.

[15] L. Karuppiah, et al., "Overview of CMP Process Control Strategies," *CMP-MIC Conference*, pp. 45-54, February 2006.

[16] Preston, F., "The theory and design of glass polishing machines," *J. Soc. Glass Technology*, IX, 11, 214-256, 1927.

[17] C. D. Schaper, K. El-Awady, A. Tay, and T. Kailath, "Control Systems for he Nanolithography Process," in *Proc. 38th Conference on Decision and Control,* pp. 4173-4178, December 1999.

[18] D. de Roover, *Motion Control of a Wafer Stage – A Design Approach for Speeding Up IC Production*. Ph.D. Dissertation, Mech. Eng. Systems and Control Group, Delft Univ. of Technology, The Netherlands, 1997.

[19] D. de Roover, O.H. Bosgra, M. Steinbuch, "Internal model-based design of repetitive and iterative learning controllers for linear multivariable systems," *Int. J. Control*, Vol. 73, No. 10, pp .914-925, 2000.