Probabilistic Analysis of a Quantum-Dot Cellular Automata Multiplier
Implemented in Different Technologies

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Abstract

Since nanoelectronic devices are likely to be defective and error-prone, developing an understanding of circuit reliabilities and critical components will be required. In this paper, probabilistic transfer matrices are used to compare the reliability of a small multiplier circuit when considering both magnetic and molecular QCA implementations. These implementations are considered since the circuit designs may differ depending on the implementation. The magnetic multiplier has a higher reliability, but it still requires component error rates of less than $10^{-4}$ to achieve a reliability of above 99%. Additionally, to increase the reliability of the multiplier, the components that should be made defect tolerant first are identified as the wire, majority gate, and fanout. The need to make these specific components, two of which are interconnect, defect tolerant is independent of the implementation technology.

1 Introduction

As Moore’s law continues to march forward, many nanoelectronic devices are being investigated to determine their fitness for adding to or replacing CMOS technology. One fact is nearly certain for all of these devices: defects will be inevitable. For this reason, these emerging technologies will need to consider defect and/or fault tolerance as they are integrated into larger circuits and systems.

One thing that may impact the reliability of certain nanotechnologies is the technology used to implement the specific device. For example, in quantum-dot cellular automata (QCA), metal-dot, molecular, and magnetic implementations have all been considered and tested experimentally. Should there be implementation specific differences in the components available to design QCA circuits, circuit reliabilities may vary significantly. In this work, a moderately sized combinational circuit, a 4x2 multiplier, is designed in QCA while considering implementation specific component differences.

The reliability of the multiplier, with unsigned input vectors of four and two bits, is examined with the probabilistic transfer matrix (PTM) method [11]. Magnetic and molecular QCA implementations of the multiplier are considered. Since magnetic QCA has the potential for a wire crossing device while building a wire crossing with two different cell types in molecular QCA is difficult, significant differences in reliability may result.

A significant advantage of the PTM method is that it does not require specific physical parameters that other methods require. For instance, similar work has recently been completed in [23], but it utilizes a quantum mechanical model that requires values such as the size and separation of QCA cells and the temperature of the system. By avoiding these requirements, circuit reliabilities can be generated to compare different implementation technologies without having to be concerned with the actual fabrication parameters of each technology.

This paper examines the reliability of a multiplier circuit when considering both magnetic and molecular QCA implementations. When the circuit components used in the multiplier have error rates of approximately $5 \times 10^{-3}$ the magnetic version has a reliability that is nearly 50% higher than the molecular version. Additional analysis demonstrates that in both multiplier versions, the majority gate, straight wire, and a fanout component have the most significant impact on reliability. This consistency demonstrates that, independent of which technology is used to implement a QCA circuit, interconnect reliability should receive significant attention when considering component level defect tolerance.

Brief introductions to QCA and PTMs\textsuperscript{1} are in Sec. 2.

\textsuperscript{1}This section is largely similar to the same section of a companion paper [4].
2 Background Material

2.1 Introduction to QCA

The quantum-dot cellular automata (QCA) architecture is built upon a foundation of simple, identical, bistable devices that interact with one another via electromagnetic forces. The initial devices for QCA were charge based and utilized a square cell of four quantum dots with potential barriers between the dots. Within the cell are two free electrons capable of tunneling through the potential barrier, which could be clock-controlled, that settle on different quantum dots due to Coulombic interaction [13]. The energetically favorable states of these cells would have the electrons in opposing corners (along a diagonal). Since there are two diagonal configurations available, the cell is bistable. By aligning the cells in specific configurations a universal set of logic gates can be constructed. Charge based QCA devices have been extensively tested and developed using metal-dot cells [20, 1, 21] and recently, molecular QCA devices have been investigated [16, 10, 15, 14, 22].

A non-charge based QCA implementation, namely magnetic QCA, is currently being investigated and shows significant promise [8, 7]. Within magnetic QCA the magnetization state of a nanomagnet provides a stable value. A single, rectangularly shaped, nanomagnet will have its magnetization align along the long axis (longer side of the rectangle) of the nanomagnet. Depending on the external forces, the magnetization of a nanomagnet with its long axis being vertical will be either straight up or down, thus satisfying the bistable constraint required by the QCA architecture. Similar to the charge-based QCA implementations, the alignment of the nanomagnets will determine the specific function that is implemented.

Figure 1 contains a variety of basic circuit components for both Coulombic (charge-based) and magnetic QCA implementations. In part (a), two nanomagnets with opposing magnetizations are shown along with a Coulombic QCA cell. The two nanomagnets are functionally equivalent to a single four-dot Coulombic cell. In the remaining figures, the solid line boxes with arrows represent nanomagnets while the dotted line boxes represent Coulombic cells. Subfigures (b) and (c) show straight and bent wires, while (d) and (e) show two different types of fanouts. The magnetic inverter shown in (f) requires only an odd number of nanomagnets while a Coulombic inverter requires a certain cell configuration. A majority gate is shown in (g). For charge based QCA implementations a wire crossing, (h), can occur in the plane by using a wire made of normal, 90 degree, cells and a wire made of rotated, 45 degree, cells as is shown in Fig. 1 [25]. Potential magnetic QCA wire crossing devices are currently under investigation [19]. There are numerous references, not listed here, in the recent literature demonstrating a wide variety of common computing structures built using these QCA components.

One limitation of a Coulombic QCA implementation, particularly if molecular cells are used, is that in the wire crossing shown in Fig. 1 sub-Angstrom level precision is required to place each cell for the crossover to function properly [3]. However, a simple combinational circuit capable of crossing wires without using 45 degree wires can be formed [2]. Since a magnetic QCA implementation might be able to have an explicit wire crossing device, this paper will look at the reliability differences in the multiplier when using the logical crossover and the single device crossover.

2.2 PTM Framework

Probabilistic transfer matrices (PTMs) were recently described in [11] as a method for accurately computing the reliability of a combinational circuit given error prone components. Each component has its own PTM, and by computing a series of Kronecker products and matrix-matrix products using these component PTMs, a PTM for the circuit is formed. This circuit PTM is then used to calculate the circuit’s reliability.

The PTM for a gate (circuit) with \( m \) inputs and \( n \) outputs is a \( 2^m \times 2^n \) matrix that, when error-free, is the truth table for the gate. For example, the error-free PTM, also termed an ideal transfer matrix (ITM), for a majority gate is Fig. 2(a). If this majority gate produces an incorrect output with probability \( p \) (error rate), regardless of input values, the PTM is Fig. 2(b). Note that within a PTM the sum for all of the entries in a row must be \( \leq 1 \), in other words, for a given input combination, the potential outputs cannot have a probability greater than one of occurring.

Overall, specific fault models are not considered here when generating the component PTMs. For example, [5] shows inversion errors in wires and [24, 17, 18] develops a number of stuck-at and related fault models for charge-based QCA components. While these models, along with any that may be developed for magnetic QCA, may be used to refine component PTM construction in future work, the component PTMs here only consider if the output differs from its expected value.

The component PTMs used here are: AND, OR, and MAJ gates; inverters; wires; single bend wires; T-shaped fanouts; regular fanouts; and a magnetic wire crossing.
The row sum limitation mentioned above, is important in deriving the PTMs for faulty fanout and wire crossing components. The PTM used for the fanout components, with an error rate of $p$, is:

$$\begin{bmatrix} 1 - p & p/3 & p/3 & p/3 \\ p/3 & 1 - p & p/3 & p/3 \\ p/3 & p/3 & 1 - p & p/3 \\ p/3 & p/3 & p/3 & 1 - p \end{bmatrix}.$$

The PTM used for the wire crossing component, with an error rate of $p$, is:

$$\begin{bmatrix} 1 - p & p/3 & p/3 & p/3 \\ p/3 & 1 - p & p/3 & p/3 \\ p/3 & p/3 & 1 - p & p/3 \\ p/3 & p/3 & p/3 & 1 - p \end{bmatrix}.$$

For this work, the error rate for the AND and OR gates matches that of the majority gates. By assuming that the fixed input to a majority gate, which would turn it into an AND or OR gate, is error-free, the overall complexity of the PTMs are reduced.

A circuit PTM is generated by first dividing the circuit into slices that are one component level each, i.e. no level has a series of components. Within a level the components are in parallel, and the Kronecker product is calculated for the level, thus giving each level a PTM. These level PTMs are then multiplied, from circuit inputs to outputs, using matrix-matrix multiplication to generate the circuit PTM. At each stage of this process, the size of the PTM corresponds to the number of inputs and outputs as discussed above.

Consider a circuit consisting of three wire components as inputs into a majority gate with the gate’s output being the input to an inverter; this function would be $Z = NOT(MAJ(A, B, C))$. The wire PTMs are 2x2, the majority gate PTM is 8x2, and the inverter PTM is 2x2. This circuit requires three levels: one for the wires, one for the majority gate, and one for the inverter. The Kronecker product of the wire level is an 8x8 matrix; recall that this level has three inputs and three outputs, and the other two levels do not require a Kronecker product operation since there are no components in parallel. Matrix-matrix multiplication between the wire level and the majority gate level results in an 8x2 matrix, and multiplying this by the inverter matrix results in a final 8x2 matrix. This is appropriate since the circuit has three inputs, A, B, and C and a single output, Z.

To generate the reliability for a circuit from its PTM [12], the PTM is element-wise multiplied with its ITM. This causes the non-desired (erroneous) terms to be removed from the resulting matrix, called ETM here, as shown in Fig. 2(c) for the majority gate case. The ETM is then left-multiplied by an input row vector, $v$, whose values are the probability of each input combination occurring. To continue the majority gate example, assume $v$ is a 1x8 row vector with each element being 0.125, which gives each input combination an equal probability of occurrence. This leaves $v \ast ETM = [0.5(1-p) \ 0.5(1-p)]$ with each entry of $v \ast ETM$ corresponding to the probability of a specific output occurring. The total circuit reliability is the result of summing
the elements of $v \ast ETM$, $1 - p$ in this example.

3 Designs

The circuits used to build the multiplier include an XOR gate and wire crossing circuit for the molecular version, a half-adder, and a full-adder. Keep in mind that the magnetic versions of these circuits utilize a wire crossing device as opposed to a circuit. These designs are presented using an approximate layout with the components from Fig. 1. The XOR gate and wire crossing circuit presented here are similar to those developed in a companion paper [4].

3.1 XOR Gate

The base XOR gate used in this paper is shown in Fig. 3(a). This gate requires three AND gates, an OR gate, two regular fanouts, a T-fanout, two single bend wires, and seven straight wires. A separate wire component has not been used between the output of the majority gate and the input of the inverter. Additionally, the output of the OR gate has been considered error free in this circuit to avoid counting this wire as erroneous multiple times in circuits utilizing the XOR circuit.

The division of the XOR gate into gate levels, with each level being denoted by $L_X$, and the construction of the XOR gate’s PTM, $\text{XOR} \_{\text{PTM}}$, is shown in Fig. 3(b). The symbol $\otimes$ is used to denote the Kronecker product operation. $I$ is the 2x2 identity matrix and is necessary to properly size the gate level matrices for matrix-matrix multiplication. $I$ is required in gate levels 2-6 as a result of the fanouts in gate level 1.

3.2 Crossover Circuit

The crossover circuit uses the axiom that $A \oplus B = B$ (similarly, $A \oplus B \oplus B = A$). Using this principle, one can design a wire crossing circuit with three XOR gates, shown in Fig. 3(c), that requires the use of only 90 degree cells. Excluding the three XOR gates, the only components used in this circuit are the three fanouts which are not marked separately. All of the input wires into the XOR gates shown in this diagram are considered error free since they are considered erroneous in their respective XOR gates. Like the XOR gate, the output wires are considered error free to prevent counting them as erroneous multiple times.

3.3 Adder Circuits

The half-adder circuit designed for this work is shown in Fig. 4(a). This design requires an XOR gate, a fanout, a wire, a single bend wire, an inverter, and an AND gate. Since no wire crossings are required, the half-adder is implementation independent for this work. The adder circuit shown in Fig. 4(b) is based on the design in [26] and requires fewer crossovers than the adder presented in [4]. Altogether, this adder uses two crossover circuits, three majority gates, two inverters, four regular fanouts, a T-fanout, seven straight wires, and two single bend wires.

3.4 Multiplier Circuit

The multiplier designed here, shown in Fig. 5, takes a four bit unsigned binary input and a two bit unsigned binary input and generates a six bit output. It is not a generalized slice of a larger multiplier. This circuit requires ten crossovers, shown as the dotted line boxes, in its interconnection network. When including the full adder circuits, a total of fourteen wire crossings are required. In the molecular implementation, the wire crossing circuit from Sec. 3.2 is utilized and in the magnetic implementation a wire crossing device is assumed. The size of the multiplier has been limited since the component level PTMs grow larger than Matlab can handle.

4 Results and Analysis

The results in this section consider the circuit reliabilities based on constant component error rates and the multiplier reliabilities if an individual component is
Figure 3. XOR gate, the gate's PTM derivation, and the wire crossing circuit.

(a) XOR gate diagram
(b) XOR gate PTM derivation
(c) Wire crossing circuit diagram

Figure 4. Adder circuit designs used here.

(a) Half-adder circuit.
(b) Full-adder circuit.

Figure 5. The 4x2 multiplier designed for this work.
considered error free. The second analysis provides insight into which components have the largest impact on circuit reliability. Since non-CMOS nanoelectronic devices are expected to have higher defect and failure rates than CMOS, the component error rates assumed here are higher as well. Using the values given in the ITRS[9], the defect rate for CMOS technology is on the order of $10^{-10}$ defects per transistor. If it is assumed that a defect in a transistor causes a gate to fail, then the 10 transistor majority gate from [6] and 12 transistor XOR gate have error rates on the order of $10^{-9}$. Accordingly, given the anticipated higher defect and fault rates in nanoelectronic devices, error rates assumed here range from $10^{-8}$ to $10^{-2}$ for the component PTMs listed in Sec. 2.2.

4.1 Constant Defect Rates

Figure 6 shows the reliability for the crossover, adder, and multiplier circuits in both technologies as a function of the component error rate $p$, with each component having the same failure rate. The figure is divided into low (a) and high (b) error rates to exaggerate the respective reliability ranges. Additionally, since the magnetic crossover circuit is actually a component, its reliability is the same at each point in these graphs as all of the other components.

In terms of the multiplier, component error rates must be below $10^{-4}$ ($1.00E-04$) for a magnetic multiplier with greater than 99% reliability. This error rate nears $10^{-5}$ for the molecular multiplier. In the $10^{-4}$ to the $5 \times 10^{-2}$ range there is a massive difference between the magnetic and molecular reliabilities that grows to approximately 50% at $5 \times 10^{-3}$. As can be seen in the graphs, circuit reliabilities also start to fall significantly once the component failure rates reach $10^{-3}$, or 1 in 1000. For the smaller circuits, the half adder is roughly as reliable as the magnetic full adder. Both of these circuits are significantly more reliable than the molecular full adder.

4.2 Perfect Component Analysis

The previous section identified the component failure ranges necessary to achieve highly reliable circuits. In this section, the multiplier’s reliability is considered with one component being perfect. Tables 1 and 2 show the reliabilities, given a constant error rate for the components, when none of the components are perfect, Fig. 6 and the 2nd column when going from left to right, and the cases where a single component is considered perfect (3rd through the rightmost columns). The columns with perfect components are sorted by higher reliabilities on the left and lower reliabilities on the right at the $1.00E-04$ error rate line.

Of particular interest in the above tables is the ordering of the perfect components. For the magnetic multiplier, having a perfect majority gate will improve the reliability more than having a perfect wire component. This changes slightly for the molecular multiplier at error rates at and below $5.00E-03$ when a perfect wire would be better than a perfect majority gate. However, in both cases, the wire and majority gate have a more significant impact than the other components. When considering the relatively significant impact the regular fanout has as well, these trends are consistent with those observed in [4] and strongly suggests that these components, mainly interconnect, should receive the earliest focus when developing defect tolerant components.

5 Conclusions

The work and results presented here should be considered preliminary since there are a number of questions that need to be answered. In particular, can a spe-
### Table 1. Magnetic multiplier reliability with zero or one perfect component(s).

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<th>Maj. Gate</th>
<th>Wire</th>
<th>Reg. Fan.</th>
<th>Crossover</th>
<th>Single Bend</th>
<th>Inverter</th>
<th>T-Fanout</th>
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### Table 2. Molecular multiplier reliability with zero or one perfect component(s).

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cific wire crossing device be created for magnetic QCA? Additional questions such as where should the error on the wire be located, should fanouts have errors, and does wire length affect the error rate still remain. Physical simulation and experimental results will be needed to answer these questions.

This work has shown that to generate high circuit reliabilities for QCA multipliers, low component error rates are required. Additionally, this work, along with [4], has shown that improving the reliability of the wire, majority gate, and fanout components will have the greatest impact on improving the multiplier’s reliability. These results are independent of implementation technology and circuit type and strongly suggest that interconnect components should receive significant attention when considering component level defect tolerance.

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References